

American Society of Mechanical Engineers

Inspection of Electronics Components for Cryogenic Temperature Operations

¹N. Poonthottathil,¹ F. Krennrich,¹ A. Weinstein,¹ J. Eisch,² L.J. Bond,³ D. Barnard,³ Z. Zhang,³ L. Koester

¹Department of Physics and Astronomy, Iowa State University

²Department of Aerospace Engineering, Iowa State University

³Center for Non-destructive Evaluation, Iowa State University

Ames, Iowa, 50010

Email: pnav@iastate.edu

Abstract

Electronics operating at cryogenic temperatures play a critical role in future science experiments, and space exploration programs. The Deep Underground Neutrino Experiment (DUNE) uses a cold electronics system for data taking. Specifically, it utilizes custom-designed ASICs (Application Specific Integrated Circuits). The main challenge is that these circuits will be immersed in liquid Argon and that they need to function for 20+ years without any access. Ensuring quality is critical, and issues may arise due to thermal stress, packaging, and manufacturing-related defects: if undetected, these could lead to long-term reliability and performance problems. The paper reports an investigation into non-destructive evaluation techniques to assess their potential use in a comprehensive quality control process during prototyping, testing, and commissioning of the DUNE cold electronics system. Scanning Acoustic Microscopy (SAM) was used to investigate permanent structural changes in the ASICs associated with thermal cycling between room and cryogenic temperatures. Data are assessed using a correlation analysis, which can detect even minimal changes happening inside the ASICs.

Keywords: Liquid Argon, correlation, cryogenic, neutrino, DUNE, NDE, ASICs

Introduction

Next-generation neutrino physics experiments will provide precision measurements to identify neutrino induced charged particle tracks using a Liquid-Argon based time projection chamber (LAr-TPC) [1]. The Liquid- Argon detector readout has to

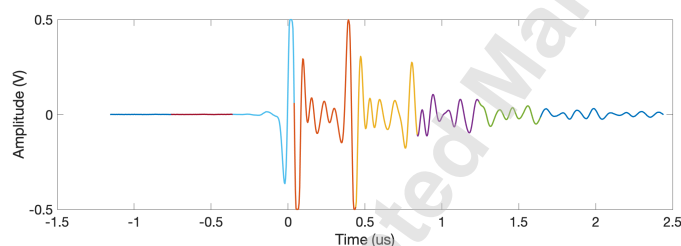
operate for many years at cryogenic temperature with stable performance. Low noise performance in the cold and proximity of the signal pick up close to detector wires favors the placement of the electronics in the liquid. A LAr-TPC contains a modular electronics system with 3,000 printed circuit Front-End Motherboards (FEMBs). Each FEMB provides the signal processing of 128-channels (wires) and may host up to 18 CMOS based ASICs, bringing the total number of ASICs to 50,000 per LAr-TPC corresponding to 10kilo-tons of liquid argon. Functionally, these chips include an amplifier, signal shaping, digitizer, and data assembly functions.

CMOS technology is well suited for operation at cryogenic temperature, due to its low power usage and minimal heating of the cryogenic liquid, thereby reducing the risk of bubbles in the detector. CMOS failure mechanisms, such as hot-carrier effect and dielectric breakdown at cryogenic temperature, can be minimized by tuning the operating voltages [2]. Detailed studies of chip lifetime were discussed in [4][5], indicating that these devices would be suitable for decades of operation. However, the reliability of the electronics components remains a major concern. Any defects associated with the manufacturing process (e.g bubbles in the thermal paste and plastic enclosure) and thermal stresses imposed during the cryo-cycling of the chips could impact the long-term performance of the system.

Scanning Acoustic Microscopy (SAM) is a highly sensitive non-destructive evaluation technique for the inspection of micro-electronics integrated circuit packages [6]. The main advantage of SAM is that it is highly sensitive to defects, including voids, cracks, and delamination inside the packaged ASICs [7]. The technique also helps to identify weak spots inside the package. The integrated circuits are made from composite materials and

In this paper, Scanning Acoustic Microscopy is utilized to probe and identify defects in the chip packaging or circuitry resulting from thermal cycling. A feature detection technique based on correlation is used to analyse the SAM data.

A SAM uses ultrasound to interrogate a material by focusing periodic sound waves onto a small region of a sample. The technique uses a transducer to generate, transmit, and detect waves reflected by the various interfaces inside the sample. Timing and amplitude of the reflected wave provide information which depends on scattering and changes in acoustic impedance. The amplitude of the reflected signal is a measure of the echoes' strength, and the position on the time axis represents the time required to travel through the sample (it is a measure of the depth). Figure 1 represents an example of a reflected wave signal. The echos correspond to reflections due to differences in acoustic impedance for the various materials. The data record is, the superposition of multiple reflections and reverberations in the chip. The frequency selected (15MHz) provided the deepest penetration depth and at the same time provided an adequate quality, in terms of lateral resolution, for the image. The use of higher frequencies, up to 25 MHz, was investigated, but attenuation was too high to allow the desired penetration depth. Measurements were performed in pulse-echo mode with a transducer with a spherical focus and the transducer focal plane was set on the top of surface of the ASICs. The measurement was taken at a sampling rate of 250 MHz and the waveform is represented in bins of time with a bin width of 4 ns.



For collecting the data presented in this paper, the scanning microscopy is set in its simplest configuration, the ‘pulse-echo mode’. With this particular configuration, a single transducer generates the pulse and receives the reflected signal at a given position of the sample. The transducer sends pulses into the material using water as a coupling medium and collects the reflected

The data from the acoustic scan can be visualized in three different modes, 1) A-Scan, showing a digital waveform from measuring the reflected signal at a given location on sample 2) B- Scan, a collection of A-Scan amplitudes along a chosen line resulting in a cross-sectional view of the sample, 3) C-Scan, a 2-D raster scan of A-Scans is performed to create a 2-D image of the inside of the chips at a given depth. A specific and depth and depth range is achieved by integrating the A-scans over a corresponding time window for each point of the raster scan. The ASICs tested here are about 1 mm thick and with dimensions of 2×2 cm. The circuit is based on 180 nm CMOS technology and each chip includes about 320,000 transistors.

A correlation analysis has been developed to study the similarities in the chips' internal structure within a group of ASICs. The signals are collected from each and every point on an ASICs, the scans yield a 150 x 150 matrix of A-Scans, containing 22,500 pixels/chip in total. In order to compare two ASICs chips for any structural differences, a cross-correlation value for each pixel based on the two corresponding A-scans by quantifying the similarity of their time traces over a given time window is calculated. Effectively two ASICs chips are compared at each position and thereby generate a 2-D image. The main advantage of this analysis technique is that the correlation can be performed by choosing any particular time gate. A particular choice of the time-gate allows a correlation analysis to be performed at any depth inside the ASICs. A low correlation value from the outside pins of ASICs is expected due to the distortions of the reflections from the edges (edge-effect) [8].

$$\Phi_{fg} = \frac{\sum_{i=1}^n f_i g_i}{\sqrt{\sum_{i=1}^n f_i^2 \sum_{i=1}^n g_i^2}} \quad (1)$$

The correlation coefficient for two different ASICs is defined according to equation (1). Here f_i, g_i refer to the reflected waveform in time bin i detected with the transducer at the location on the two different ASICs. These waveforms are in digitized format, recorded with a sampling rate of 250 MHz. The Correlation value Φ_{fg} quantifies the similarity between the two waveforms over a chosen time window, corresponding to n time samples, and a specific depth regime inside the chips. In this analysis the starting time of all the incident waveforms are synchronized, to ensure that there is no offset – as would be indicated by a time lag between the incident waves reflected off the top surface of the sample. The resulting correlation values Φ_{fg} computed yield a 2-D map/image of the chip comparison. If the reflected waveforms of the two chips are close to identical, a high correlation value close to 1 is expected. A correlation value of 0 indicates no correlation, due to substantially different waveforms. A correlation value of -1 corresponds to a phase shift between the waveforms from the two chips.

Results and Discussions

The similarity of the sample is evaluated by looking at the 2-D image formed using the correlation values. Images were created by forming the correlation values for the entire time window, and selection of a narrowed time-window to focus on a given depth inside the material. When the correlation analysis is performed in the frequency domain by using the short-time Fourier transform of the signal, the features appeared to be the same.

A more general view of a collection of 9 ASICs and their internal structural similarities can be gleaned from Figure 2. Here, a distribution of the correlation values is shown for eight chips compared to a reference chip. As can be seen, most chips show correlation value distributions clustered around 1, corresponding to a high level of similarity with the inner structure compared with the reference chip. One sample (chip identification number 1745) exhibits a broad correlation value distribution. This chip had been purposely exposed to mechanical pressure to induce delamination inside. Furthermore, ASICs chip number 1732 shows a broadened correlation value distribution compared to the other chips, indicating that the inner structure differs substantially from the reference chip. Several ASICs were immersed in liquid nitrogen and then quickly removed for an acoustic microscopy scan. The 2-D image of the ASICs, formed using the

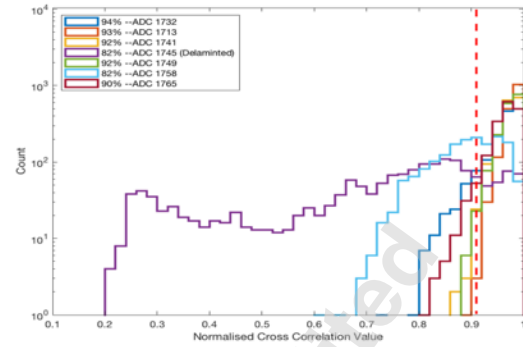


Figure 2: The distribution of the correlation values for the damaged ASICs is compared with the other ASICs, a clear shift towards the lower correlation value is noticed.

correlation values, is used to detect changes inside the ASICs before and after the liquid nitrogen treatment (multiple thermal-cycling for 20 minutes), Figure 3. There is an apparent difference in the internal structure, as indicated in the image. A small strip feature appeared at a depth of 0.4 mm inside the ASIC packaging (calculated from the time of the reflected wave, the velocity of the sound in this composite material is approximately 2800 m/s) [9]. This type of feature inside the ASIC is an indication of an anomaly that could be due to a stitch crack caused by delamination [10]. In order to confirm this hypothesis we plan correlate such anomalies with functional tests. We also plan to physically inspect the chip by chemically opening up the packaging. To gain a more detailed view of the regions of interest, Figure 5, shows the corresponding B-Scan images of the chip before (top) and after the liquid nitrogen treatment (bottom). The comparison shows a clear change in the center region. A slight multi-layer indentation was already present before the temperature cycling (top) and this is much enlarged after the cycling (bottom). The original waveforms from the defect location compared before and after the liquid nitrogen treatment, and exhibited a phase inversion in the waveforms at a particular depth inside the chip; Figure 5.

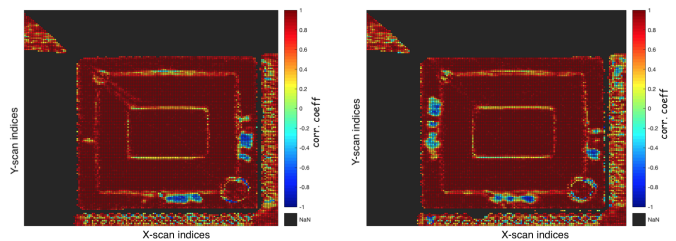


Figure 3: The C-scan image of two the ASICs formed using the correlation values of the samples before and after treated with liquid nitrogen, a clear change is observed in the sample. This image corresponds to a particular depth inside the sample. The waveform from the blue region shows a clear phase inversion.

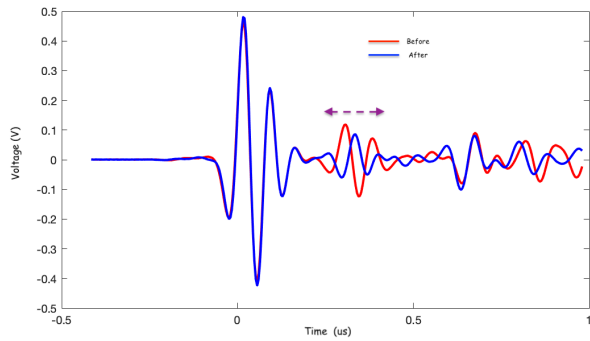


Figure 4: Waveforms recorded in the anomalous blue region in figure 3, before and after liquid nitrogen treatment are shown in here. A clear phase inversion in the waveform is seen which typically is indication of a delamination inside the chip. The time gate corresponding to the low correlation value is marked in the figure.

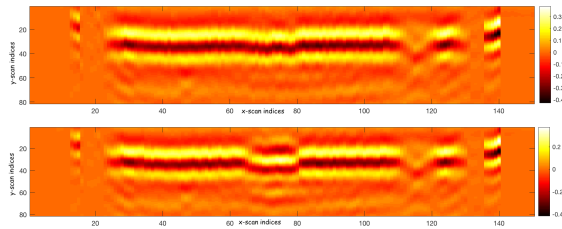


Figure 5: The B-scan image from one of the ASICs before (top) and after (bottom) treated with the liquid nitrogen. A shift in the B-scan waveform could be an indication of sensitive regions inside the chip package.

The systematic uncertainty associated with the correlation measurement has been calculated by a measurement carried out on the same chip consecutively and by computing the correlation value, and the deviation from 1 is quoted as the error in the measurement. The uncertainty in the correlation measurement is about 5%, see, Figure 6 (the outside pin region on the sample is not included due to the known effect of the scattering of the acoustic wave). The numbers corresponds to each index on the bottom plot of Figure 6 is given by,

$$\text{Syst.Error } (\Delta_i) = \left(\frac{\sum_{j=1}^{150} 1 - \phi_{ij}}{150} \right) * 100 [\%] \quad (2)$$

Conclusions

Scanning Acoustic Microscopy is used to evaluate its potential for non-destructive testing of ASICs. In this work, a cor-

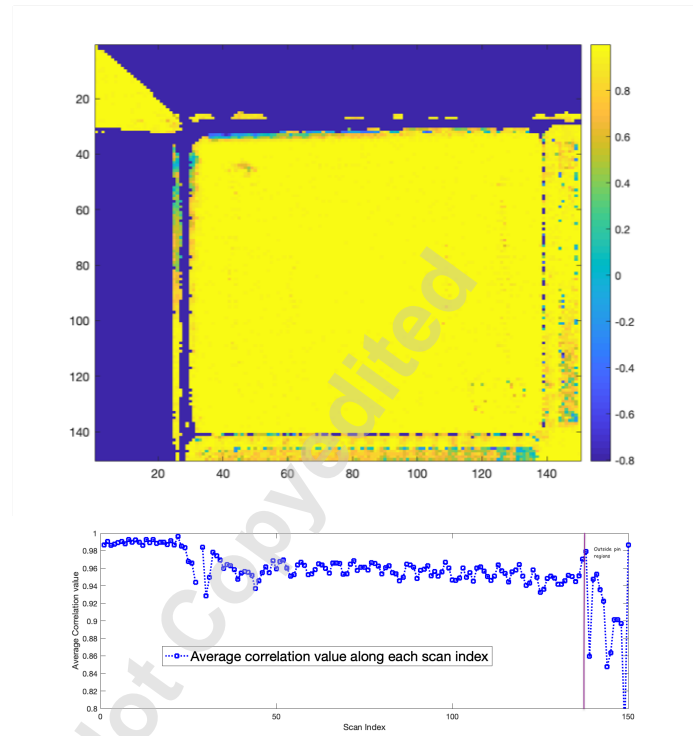


Figure 6: The top is the correlation of the same chip by taking after two consecutive measurement, and the bottom is the average value of correlation along the scan indices. The Low correlation values corresponds to the scattering from the edges are due to the scattering of the acoustic wave.

relation analysis was developed that allows one to perform a comparison between different chips. This technique was demonstrated to be highly sensitive to even small changes. For example, one can compare statistical samples of chips with different testing histories, such as failed functional tests and well-performing chips.

Furthermore, this correlation analysis was used to study the effects of temperature cycling between 87K and room temperature. Results demonstrate structural changes in several chips that occurred after cryogenic cycling. Further functional tests and destructive evaluation are needed to fully understand the origin of these structural changes. Furthermore some diagonal feature across the inner chip at the depth of the thermal paste layer was identified and we will investigate more about this feature the future studies.

Acknowledgment

This research is supported by grants from the U.S. Department of Energy Office of Science and by Iowa State University. We would like to acknowledge our colleagues Matt Worcester,

Steve Kettel and Hucheng Chen from Brookhaven National Laboratory for providing ASIC chips samples and for the fruitful discussions of this work.

J.J.M. Zaal “Delamination-induced stitch crack of copper wires” IEEE 18 th Conference on Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE) (2017). 10.1109/EuroSimE.2017.7926294

[1] B. Abi “The single phase ProtoDUNE technical review report” arXiv:1706.07081 (2017).

[2] S. Gao, “The Development of Front-End Readout Electronics for ProtoDUNE-SP LAr TPC” Proceedings of Science Vol 313 (2017).

[3] B. Abi “DUNE TDR Deep Underground Neutrino Experiment (DUNE)” arXiv:1807.10334v1 (2017).

[4] T. Chen “CMOS reliability issues for emerging cryogenic lunar electronics applications,” Solid-State Electron., vol. 50, pp. 959–963 (2006).

[5] C. Hu “Hot-electron-induced MOSFET degradation-model, monitor, and improvement,” IEEE J. Solid-State Circuits, vol. SSC-20, no. 1, pp. 295–305, Feb. (1985).

[6] J. Yang. “Non-destructive identification of defects in integrated circuit package by scanning acoustic microscopy” Microelectron.Reliab.Vol.36, N0.9. pp.1291-1295 (1996).

[7] Poonthottathil N., Krennrich F., Eisch J., Weinstein A., Bond L. J., Barnard D., Zhang Z., & Koester L. “Reliability studies of application specific integrated circuits operated at cryogenic temperature”, 46th Annual Review of Progress in Quantitative Nondestructive Evaluation QNDE 2019-7089 (2019). <https://www.iastatedigitalpress.com/qnde/article/id/8744/>

[8] Sandeep Kumar Diwendi, “Advances and Researches on Non-Destructive Testing: A Review” Materials Today: Proceedings 5 (2018) 3690–3698 (2018).

[9] Pouria Aryan, “An Overview of Non-Destructive Testing Methods for Integrated Circuit Packaging Inspection” Sensors 2018, 18, 1981 (2019).

[10] Toshio Kondo and Mituyoshi Kitatuji “Composite Materials and Measurement of Their Acoustic Properties” Japanese Journal of Applied Physics Vol. 43, No. 5B, 2004, pp. 2914–2915 (2004).

[11] M. van Soestbergen, A. Mavinkurve, S. Shantaram,