Environ-stabilized voltage references

by

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ABSTRACT

A new design approach for high performance voltage references has been developed. This approach exploits the inflection point property of a first-order voltage reference where the temperature derivative is zero at a temperature in the range of interest. By creating an ordered family of these references with the corresponding inflection points distributed across a wide temperature range and using a temperature trigger to continuously transition between these references, a highly accurate wide temperature range voltage reference is realizable. The resultant voltage references that have an output voltage that has been stabilized to temperature changes in the environment are termed "environ-stabilized" voltage reference. The implementation of an environ-stabilized voltage reference using this approach is verified through both transistor level and behavioral simulations. The implementation of a 3-family reference predicts an error voltage of less than 180μV for a temperature between -40°C and 100°C. This is equivalent to a temperature coefficient of 1.06ppm/°C. Further reductions in the equivalent temperature coefficient are possible if the number of members in the family is increased.

The performance degradation of the environ-stabilized voltage references due to process variations was also studied. A self-calibration scheme has been introduced to correct errors introduced by process variations. The result suggests the environ-stabilized reference approach can be used for the realization of highly accurate voltage references that operate over a wide temperature range throughout a wide range of the process variations.

1. INTRODUCTION

Many electrical systems require voltage references to maintain acceptable performance. Ideally, a voltage reference should have no variation in the output voltage over all operating conditions. Environmental factors such as power supply fluctuation and temperature variations invariably cause output perturbations with virtually all known voltage references. Ideal references are not necessary provided the error introduced in the reference can be bounded to a level defined by a given application. The performance requirements imposed on a reference circuits varies widely with the specifications of a system. For example, an 8-bit analog-to-digital converter (ADC) has substantially lower accuracy requirements on the voltage reference than is required for a 12-bit ADC. The accuracy requirements for the reference in an ADC are generally a fixed fraction of a Least Significant Bit (LSB) independent of the resolution of the ADC. If V_{REF} for both an 8-bit and a 12-bit ADC is 1V, than the corresponding LSB are 3.91mV and 0.244mV respectively. Thus, a 12-bit ADC would require a much more accurate voltage reference than what is required in an 8-bit ADC.

The effects of temperature changes in a reference are determined primarily by two factors, the intended temperature range of a system and the sensitivity of the reference to a system and the sensitivity of the reference to temperature. The temperature coefficient (TC) is often used to characterize the sensitivity of a reference with respect to temperature and is defined by

$$TC(T_0) = \frac{1}{V_{REF}} \cdot \frac{\partial V_{REF}}{\partial T}\bigg|_{T = T_0} \tag{1.1}$$

where T_0 is any temperature.

Often the TC is expressed in parts per million and can be obtained from (1.1) by multiplying by 10^6, that is

$$TC_{ppm}(T_0) = \frac{10^6}{V_{REF}} \cdot \frac{\partial V_{REF}}{\partial T}\bigg|_{T=T_0} \tag{1.2}$$

Throughout this thesis we will use the term TC to denote either the definition in (1) or (1.2), the distinction in the units of the expression with the latter being ppm/°C.

In general, the temperature coefficient is a function of temperature and if TC (T_0) is known, (1.2) represents a differential equation that can be solved to obtain $V_{REF}(T)$. If TC (T_0) is independent of temperature and the partial derivative is small, then the change in V_{REF} to a change in temperature from T_1 to T_2 can be approximated by the expression

$$V_{REF}(T_2) - V_{REF}(T_1) = \Delta V_{REF} \approx TC \cdot V_{REF}(T_2 - T_1) \cdot 10^6 \; ppm \tag{1.3}$$

From (1.3), an approximate expression for the equivalent temperature coefficient needed to maintain a change of ΔV over a temperature range T_2-T_1 can be obtained. This expression is simply

$$TC_{eq} = \frac{\Delta V \cdot 10^6 \; ppm}{T_2 - T_1} \tag{1.4}$$

It must be emphasized, however, that this equivalent temperature coefficient would represent the actual temperature coefficient only if TC is independent of temperature and T_2-T_1 is small.

The equivalent temperature coefficient corresponding to 1LSB for the 8-bit and 12-bit examples give some insight into the temperature stability that will be required for voltage references in data converters. For example, it follows from (1.4) that a 12-bit ADC with a nominal reference voltage of 1V that must operate over the -30°C to 80°C range would have a TC_{eq} for a 1LSB change of

$$TC_{eq} = \frac{\frac{1V}{2^{12}} \times 10^6}{80-(-30)} = 2.22 ppm/°C$$

where the same converter which must operate only over the 0°C to 50°C range would have a TC_{eq} of

$$TC_{eq} = \frac{\frac{1V}{2^{12}} \times 10^6}{50-0} = 4.88 ppm/°C$$

It should be emphasized, however, that the required temperature coefficient for a 12-bit data converter may be somewhat more stringent than this numerical example suggests for two reasons. First, the assumption that the TC is independent of temperature may not be justifiable over the reasonably wide temperature ranges considered in these examples but more importantly, the data converter application would likely not justify allocating a full LSB error to the temperature dependence of the reference voltage. These two examples do show, however, that the performance requirements on the reference circuits are strict for highly accurate systems and even stricter if the systems are required to operate over a wide temperature range. Current state-of-the-art reference circuits design techniques can readily achieve temperature stability of less than 10ppm/°C [2]. At the present time, it is challenging to design references 12-bit ADC applications that operate over a 50°C range. References for

16-bit ADC that operate over a 100°C range are well beyond the state-of-the-art in voltage references design. Designing references that have high accuracy over a wide temperature range is not an easy task, with state-of-the-art approaches not providing the performance desired in many high-end systems.

A lot of researchers have been attempting to design high performance references by proposing various techniques and approaches [5-15]. Although considerable effort has been focused upon developing circuit architectures that provide high accuracy over a wide temperature range and these efforts have resulted in reasonable success, the research community has not had much success at maintaining good process over process variations. Most, if not all, solutions to the process variation related problems rely heavily on post-process trimming [7-13] which is expensive. The current state-of-the-art can be succinctly summarized by observing that existing approaches to voltage references design provide reasonable temperature stability with expensive post-fabrication trimming but still much less than what is required for many applications; meanwhile, researchers have had little success at designing references that are robust to process variations without post-fabrication trimming. I believe it is necessary to simultaneously address both temperature stability and process variation issues of designing high performance reference circuits. The work reported here not only presents a new reference circuit design technique that offers high accuracy over a wide operating temperature range but it also proposes a self-calibration scheme to provide robustness to process variations without the need for post-fabrication trimming. Table 1.1 shows a comparison between the state-of-the-art approaches and the proposed approach.

Table 1.1 Comparison between the state-of-the-art and the proposed approach

Approach	Nominal V_{REF} (V)	Temperature range (°C)	TC (ppm/°C)
Nonlinear correction [8]	0.199	0~125	3
Exponential compensation [9]	1.264	-55~125	6.65
Piecewise-linear [6]	0.595	-15~90	6.5
Environ-stabilized (proposed)	1.212	-40~100	1

2. VOLTAGE REFERENCE CIRCUITS

The most popular approach to realizing temperature compensated voltage references is to cancel the temperature dependence of a generated voltage by summing it with appropriately weighted voltages that have the opposite temperature dependence [1,2]. If the positive temperature dependence perfectly cancels the negative temperature dependence at a given temperature, a zero temperature coefficient can be obtained at that temperature. If the temperature dependence remains small in the region of the zero temperature coefficient, a reasonable voltage reference is obtained. For example, a first-order temperature compensated voltage reference is realized by canceling the linear negative temperature dependence of a p-n junction diode voltage with a positive temperature dependent voltage generated by a PTAT (proportional-to-absolute-temperature) circuit. Ultimately, precision references can be realized by removing the nonlinear temperature dependence of the diode voltage. Current state-of-the-art precision references are mostly based upon circuit structures that remove the higher-order temperature dependence of a diode voltage. Since diodes are the nucleus of voltage reference circuits, it is important to understand the temperature dependence of the diode voltage.

2.1 – Temperature dependence of diodes

The collector current and the base-emitter voltage of a BJT can be related by the following expression:

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \tag{2.1}$$

or

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right), \tag{2.2}$$

where I_C is the collector current, I_S is the forward-active saturation current, V_{BE} is the base-emitter voltage, and V_T is the thermal voltage,

$$V_T = \frac{kT}{q} \tag{2.2a}$$

where k is the Boltzmann's constant: 8.62×10^{-5} eV/°K, T denotes temperature, q is the electron charge: 1.6×10^{-19} Coulomb. I_S can be expressed by [1-4]

$$I_S = \frac{q\left[AT^3 \exp\left(\frac{-V_{go}}{V_T}\right)\right](V_T B T^{-n})A_e}{Q_B}, \tag{2.3}$$

where A is a constant with a typical value of 5.4×10^{31} and B is the scaling factor for mobility. Q_B is the number of doping atoms in the base per unit emitter area, A_e is the cross-sectional area of the emitter, n is a process dependent constant, and V_{go} is the extrapolated base-emitter voltage at 0 °K. The base-emitter voltage can be rewritten as a function of an arbitrary reference temperature, T_o, by manipulating equation (2.2) with (2.3) and assuming an x-order temperature dependence of the collector current. Refer to Appendix F for derivation.

$$V_{BE} = V_{go} - \frac{T}{T_o}\left[V_{go} - V_{BE}(T_o)\right] - \left[(4-n)-x\right]V_T \ln\left(\frac{T}{T_o}\right). \tag{2.4}$$

Equation (2.4) can be rewritten in a more designer-friendly form which gives yield to another V_{BE} expression. Refer to Appendix G for derivation.

$$V_{BE} = \left[V_{g0} + (\eta - x)V_{T_o}\right] - \left[\frac{V_{g0} - V_{BE}(T_o) + (\eta - x)V_{T_o}}{T_o}\right]T - \left\{\frac{(\eta - x)V_{T_o}}{T_o}\left[T\ln\left(\frac{T}{T_o}\right) - T + T_o\right]\right\} \quad (2.5)$$

where η denotes the constant *4-n*, and has a value between 3.6 and 4. Note that the first term in equation (2.5) is independent of temperature, the second term has first-order temperature dependence, and the last term has higher-order temperature dependence.

2.2 – First-Order Voltage References

First-order voltage references are commonly known as the bandgap voltage references. The basic idea is to compensate the first-order negative temperature dependence of the diode with a PTAT voltage. The resultant reference voltage is the sum of the diode voltage and the PTAT voltage. By appropriately weighting the two components, an inflection point in the sum can be obtained. The temperature variation of the reference in the vicinity of the inflection point is small. Refer to Figure 2.1 for a graphical illustration on this compensation approach. The resulting references are capable of achieving temperature accuracy ranging from 20ppm/°C to 100ppm/°C [2].

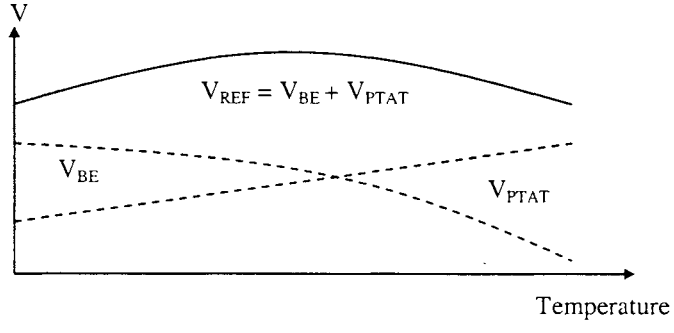


Figure 2.1 Temperature compensation of first-order voltage references

PTAT voltages can be generated by taking the difference in the junction voltages of two base-emitter junctions biased at currents I_1 and I_2. To see this, it can be observed from equation (2.2) that for any bipolar device, the base-emitter voltage relates to the collector current by the relationship

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) \tag{2.5a}$$

Thus it follows from (2.5a) and (2.3) that the difference of the two base-emitter voltages is given by

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = \frac{kT}{q} \ln\left(\frac{I_{C2}}{I_{C1}} \cdot \frac{A_{E1}}{A_{E2}}\right) \tag{2.6}$$

where A_E denotes the base-emitter junction area. First-order references are realized by a weighted sum of equation (2.5) and (2.6), which yields to the following expression:

$$V_{REF} = V_{BE2} + \beta \cdot \Delta V_{BE} \tag{2.7}$$

where β is a design parameter that controls the relative weighting of the PTAT voltage and the diode voltage. Substituting from (2.5) and (2.6) into (2.7), this may be expressed as

$$V_{REF} = \left[V_{go} + (\eta - x)V_{T_o}\right] + \left[\beta \cdot \frac{kT}{q} \ln\left(\frac{I_{C2}}{I_{C1}} \cdot \frac{A_{E1}}{A_{E2}}\right) - \frac{V_{go} - V_{BE2}(T_o) + (\eta - x)V_{T_o}}{T_o}\right] T$$
$$- \left\{\frac{(\eta - x)V_{T_o}}{T_o}\left[T \ln\left(\frac{T}{T_o}\right) - T + T_o\right]\right\} \tag{2.7a}$$

Taking the derivative of V_{REF} with respect to temperature, we obtain

$$\frac{\partial V_{REF}}{\partial T} = \beta \cdot \frac{kT}{q} \ln\left(\frac{I_{C2}}{I_{C1}} \cdot \frac{A_{E1}}{A_{E2}}\right) - \frac{V_{go} - V_{BE2}(T_o) + (\eta - x)V_{T_o}}{T_o} - \frac{(\eta - x)V_{T_o}}{T_o} \ln\left(\frac{T}{T_o}\right)$$

(2.8)

This derivative will become 0 at $T=T_0$ if

$$\beta \cdot \frac{k}{q} \ln\left(\frac{I_{C2}}{I_{C1}} \cdot \frac{A_{E1}}{A_{E2}}\right) = \left[\frac{V_{go} - V_{BE2}(T_o) + (\eta - x)V_{T_o}}{T_o}\right] \tag{2.8.1}$$

Thus, if (2.8.1) is satisfied, the reference will have an inflection point at $T=T_0$ and the temperature variation of the reference at temperatures in the vicinity of $T=T_0$ will be small. These references are often termed first-order references since if (2.8.1) is satisfied, the first-order temperature dependent term in (2.7a) will be cancelled. Solving for β in (2.8.1), we obtain

$$\beta = \frac{V_{go} - V_{BE2}(T_o) + (\eta - x)V_{T_o}}{T_o \cdot \frac{k}{q} \ln\left(\frac{I_{C2}}{I_{C1}} \cdot \frac{A_{E1}}{A_{E2}}\right)} \tag{2.9}$$

With the inflection point being placed at $T= T_0$, it follows from (2.7a) that

$$V_{REF} = \left[V_{go} + (\eta - x)V_{T_o}\right] - \left\{\frac{(\eta - x)V_{T_o}}{T_o}\left[T \ln\left(\frac{T}{T_o}\right) - T + T_o\right]\right\} \tag{2.10}$$

A plot of V_{REF} vs. temperature is depicted in Figure 2.2. Note that the nonlinear temperature dependence is still present and deteriorates performance at temperatures away from T_0. If the performance of the first-order reference is not adequate, the nonlinear error still needs to be accounted for. A circuit implementation of the first-order reference, often termed the bandgap reference, will be given in the next section.

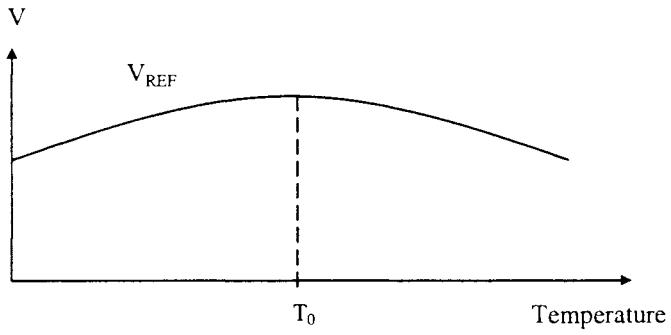


Figure 2.2 First-order voltage references

2.2.1 – Circuit Implementation of First-Order Voltage References

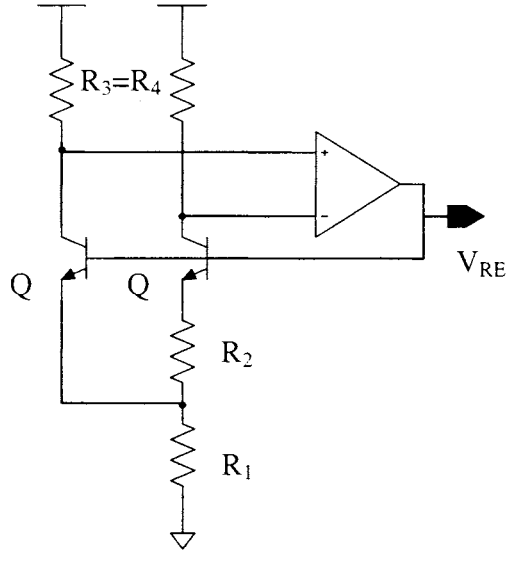


Figure 2.3 Bandgap voltage reference

It follows that the voltage V_{REF} can be expressed as

$$V_{REF}=V_{BE2}+V_{R1} \tag{2.11}$$

If R_3=R_4 it follows that I_{C1}=I_{C2} and hence I_{R1}=2I_{R2}. But I_{R2} can be expressed as

$$I_{R2} = \frac{V_{BE2} - V_{BE1}}{R_2} = \frac{\Delta V_{BE}}{R_2} \tag{2.12}$$

Substituting (2.12) into (2.11), we obtain

$$V_{REF} = V_{BE2} + \frac{2R_1}{R_2}\Delta V_{BE} \tag{2.13}$$

This is precisely of the form of a first-order voltage reference as given in (2.7) where

$$\beta = \frac{2R_1}{R_2} \tag{2.13a}$$

It follows from (2.9) that an inflection point in V_{REF} can be placed at T_0 provided

$$\beta = \frac{2R_1}{R_2} = \frac{V_{go} - V_{BE2}(T_o) + (\eta - x)V_{T_o}}{T_o \cdot \frac{k}{q}\ln\left(\frac{I_{C2}}{I_{C1}} \cdot \frac{A_{E1}}{A_{E2}}\right)} \tag{2.14}$$

Recall x is a parameter that denotes the temperature dependence of the collector currents in the circuit. The circuit in which a diode is embedded will determine the current that flows in the device. Thus, for the circuit of Fig 2.3, the resultant value of x can be determined. Since I_{R2}= I_{E2} =αI_{C2}, it follows from (2.6) that

$$I_{R2} = \alpha_F I_{C2} = \frac{V_{BE2} - V_{BE1}}{R_2} = \frac{\Delta V_{BE}}{R_2} = \frac{1}{R_2} \cdot \frac{kT}{q}\ln\left(\frac{A_{E1}}{A_{E2}}\right) \tag{2.15}$$

where α_F related to the "beta" of the transistor by the relationship

$$\alpha_F = \frac{\beta_F}{1 + \beta_F} \tag{2.15a}$$

Reorganizing (2.15) to form an expression of the collector current as a function of temperature yields

$$I_{C2} = \left[\frac{k}{\alpha_F R_2 q}\ln\left(\frac{A_{E1}}{A_{E2}}\right)\right]T \qquad (2.16)$$

Equation (2.16) indicates that the collector current has a first-order temperature dependence. Upon comparison with (X.7) in Appendix F, it follows that the variable x in (2.14) is simply x=1. It thus follows from (2.10) that

$$V_{REF} = \left[V_{go} + (\eta - 1)V_{T_o}\right] - \left\{\frac{(\eta - 1)V_{T_o}}{T_o}\left[T\ln\left(\frac{T}{T_o}\right) - T + T_o\right]\right\} \qquad (2.16a)$$

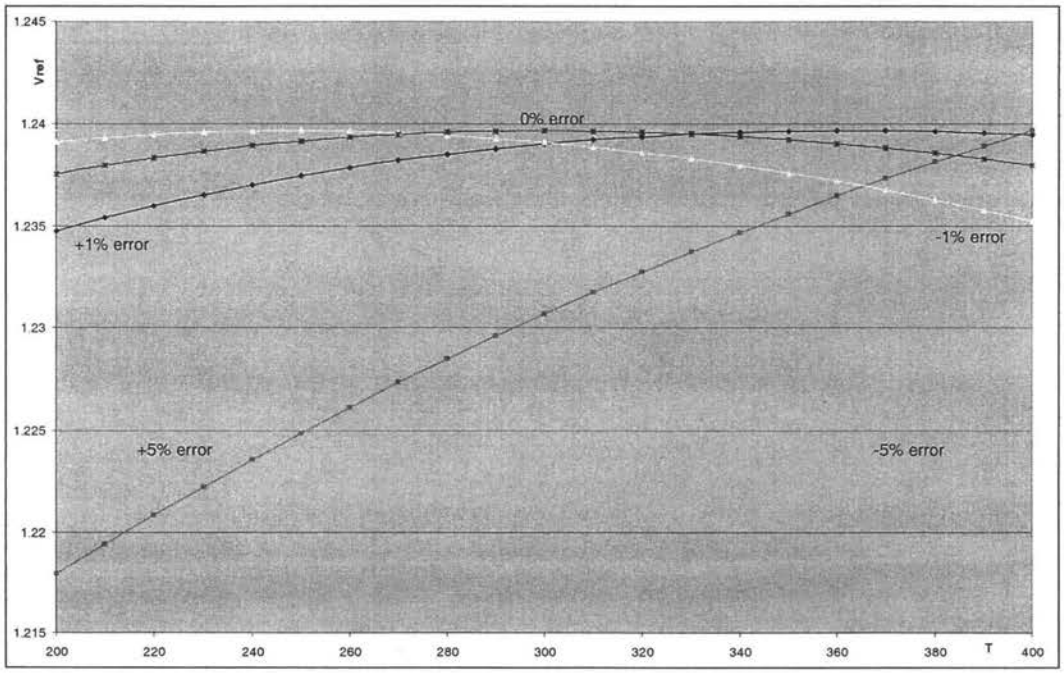


Figure 2.3.1 Effects of process variations on first-order references. (a) Ideal first-order reference. (b) and (c) Effects of inflection point shift with process

From a practical viewpoint, there are limitations in the first-order temperature compensation technique. These are depicted in Figure 2.3.1. When designing a voltage reference, the requirements generally stipulate a maximum deviation in the reference voltage over a

temperature interval depicted as $T_{min}<T<T_{max}$ in Figure 2.3.1. The strategy in designing this reference will then be to select T_0 so that $V_{REF}(T_{min}) = V_{REF}(T_{max})$ so that the total deviation in voltage over the specified operating range, given in this case by

$$\Delta V_{REF} = V_{REF}(T_o) - V_{REF}(T_{\min})$$

will be minimized. If the inflection point drifts to the left or the right as depicted in Figure 2.3.1, the total deviation in voltage given by

$$\Delta V_{REF} = V_{REF}(T_o) - \min\{V_{REF}(T_{\min}), V_{REF}(T_{\max})\} \qquad (2.16.2)$$

will increase and since the derivative of the $V_{REF}(T)$ curve becomes quite large away from T_0, even a modest change in T_0 can result in a significant degradation in performance of V_{REF}. To put it in perspective, a 1% error in the gain factor β would increase the total voltage deviation by 100%. A 5% error would cause a 900% increase in the voltage deviation!

Thus one major limitation in the first-order reference is the deviation of the inflection point T_0 with process. A second limitation is associated with the dramatic increase in slope of the $V_{REF}(T)$ curves away from the inflection point. In many applications, even if the inflection point is trimmed so that (2.16.1) is satisfied, the value of ΔV_{REF} may still be unacceptably large. A plot of ΔV_{REF} and TC_{eq} versus $\Delta T=T_{max}-T_{min}$ for first-order references can be obtained from (2.16a) and (1.4) and is shown in Figure 2.3.2. In this plot it was assumed that no process variations were present and that the geometric mean of T_{max} and T_{min} was fixed at 30°C. Also shown in the figure is the corresponding inflection point. From this plot, it is apparent that first-order references offer potential, if process variations can be appropriately compensated, for obtaining 20~100 ppm/°C performance range [2,10-13]. Table 2.1 shows a comparison between several published and commercial available first-order voltage references.

Table 2.1 Comparison between several first-order voltage references

Published work / Commercial parts	TC (ppm/°C)	Temperature range (°C)	Trim
A. Buck et al [10]	112	0~70	Yes
R. Stair et al [11]	92	0~100	Yes
Maxim MAX6006A	30	-40~85	Yes
Maxim MAX6006B	75	-40~85	Yes
Analog Devices ADR280	20	-40~85	Yes

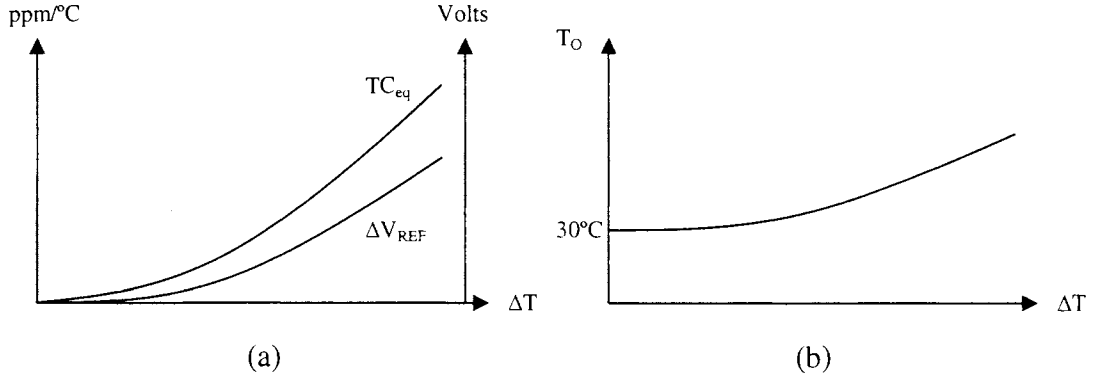


Figure 2.3.2 (a) & (b) TC_{eq} and ΔV_{REF} vs. ΔT for first-order voltage references

If better accuracy than is attainable with first-order references is required, alternate strategies for realizing the reference voltage must be developed. References that attempt to go beyond the concept of establishing a single inflection point are termed curvature compensated references. Curvature compensated references will be discussed in the next session.

2.3 – Curvature-Corrected Voltage References

In order to achieve precision voltage references, the nonlinear temperature components can be compensated in addition to the first-order terms. Several techniques had

been developed and reported [5-15] that provide higher-order temperature compensation. These techniques are found on one common ground, which is to introduce higher-order temperature dependent terms to offset the nonlinear components of the diode voltage. Invariably they depend upon the introduction of additional inflection points in the V_{REF} (T) relationship. A typical approach for such compensation is through the addition of a squared PTAT ($PTAT^2$) voltage that is second-order temperature dependent to a first-order effect free reference voltage, thus leaving only third and higher order effects present in the reference. The second-order approach can potentially achieve temperature stability of 1 to 20ppm/°C [2]. A typical second-order compensation operation is depicted in Figure 2.4.

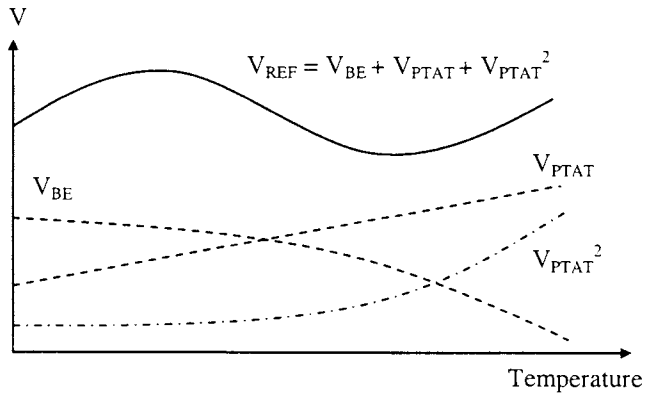


Figure 2.4 Second order temperature compensation

2.3.1 – Second-Order Temperature Compensations

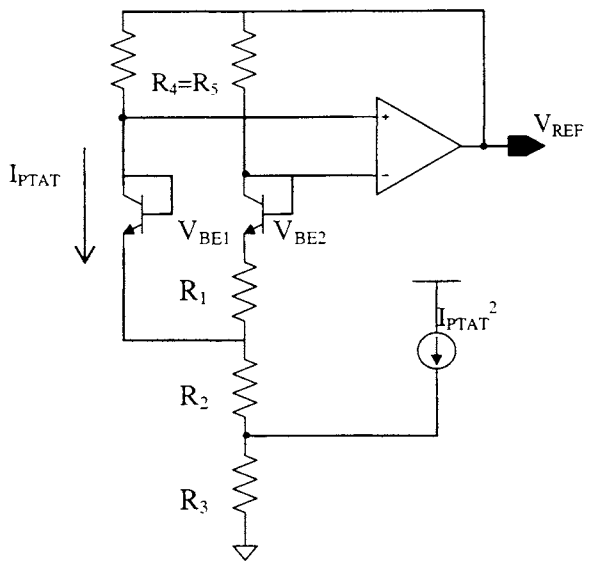


Figure 2.5 Second-order voltage reference

The output voltage of the circuit depicted in Figure 2.5 has the following expression [2]:

$$V_{REF} = V_{BE2} + 2I_{PTAT}\left(\frac{R_4}{2} + R_2 + R_3\right) + I_{PTAT}{}^2 R_3 \qquad (2.17)$$

where

$$I_{PTAT} = \frac{V_{BE2} - V_{BE1}}{R_1} = \frac{\Delta V_{BE}}{R_1} = \frac{1}{R_1} \cdot \frac{kT}{q} \ln\left(\frac{A_{E1}}{A_{E2}}\right) \qquad (2.18)$$

It follows from (2.5), (2.17) and (2.18) that

$$V_{REF} = V_{go} + (\eta - x)V_{To} + T\left\{\left[R_4 + 2(R_2 + R_3)\right]\frac{k}{qR_1}\ln\left(\frac{A_{E2}}{A_{E1}}\right) - \frac{V_{go} - V_{BE}(T_o) + (\eta - x)V_{To}}{T_o}\right\}$$
$$+ \left\{R_3\left(\frac{k\ln\left(\frac{A_{E1}}{A_{E2}}\right)}{qR_1}\right)^2 T^2 - \frac{(\eta - x)V_{To}}{T_o}\left[T\ln\left(\frac{T}{T_o}\right) - T + T_o\right]\right\} \qquad (2.18a)$$

It again follows from (2.15) and (2.16) that x=1 so this equation simplifies to

$$V_{REF} = V_{go} + (\eta - 1)V_{To} + T\left\{[R_4 + 2(R_2 + R_3)]\frac{k}{qR_1}\ln\left(\frac{A_{E2}}{A_{E1}}\right) - \frac{V_{go} - V_{BE}(T_o) + (\eta - 1)V_{To}}{T_o}\right\}$$
$$+\left\{R_3\left(\frac{k\ln\left(\frac{A_{E1}}{A_{E2}}\right)}{qR_1}\right)^2 T^2 - \frac{(\eta - 1)V_{To}}{T_o}\left[T\ln\left(\frac{T}{T_o}\right) - T + T_o\right]\right\} \qquad (2.18b)$$

Therefore, R_2, R_3, R_4 and the base-emitter area ratio of the diodes pair, A_{E1}/A_{E2}, are chosen to cancel the first-order temperature dependence of V_{BE2}. Meanwhile, I_{PTAT}^2 and R_3 are chosen to cancel the second-order component of the temperature dependence of V_{BE2} as indicated in the last term of (2.18b). It remains to implant an I_{PTAT}^2 generator. An I_{PTAT}^2 generator can be implemented with the circuit depicted in Figure 2.6 [2].

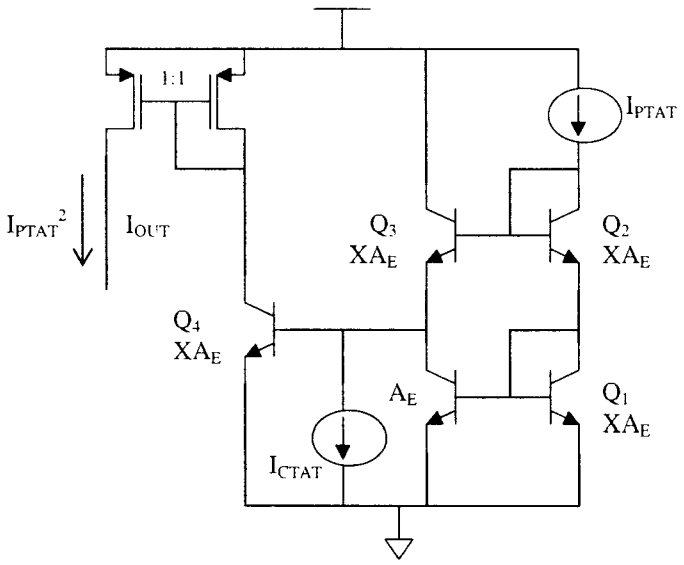


Figure 2.6 I_{PTAT}^2 generator

Applying Kirchoffs Voltage Law to the voltage loop formed by transistors Q_1-Q_4 yields to the following expression:

$$V_{BE4} + V_{BE3} - V_{BE2} - V_{BE1} = 0 \qquad (2.19)$$

Since Q_1-Q_4 have the same base-emitter area and it follows from (2.2) and (2.2a) that (2.19) can be rewritten as

$$0 = \frac{kT}{q}\ln\left(\frac{I_{C4}}{I_{S4}}\cdot\frac{I_{C3}}{I_{S3}}\cdot\frac{I_{S2}}{I_{C2}}\cdot\frac{I_{S1}}{I_{C1}}\right) = \frac{kT}{q}\ln\left(\frac{I_{C4}}{I_{C2}}\cdot\frac{I_{C3}}{I_{C1}}\right) \qquad (2.19a)$$

If the transistors have infinite beta it follows that $I_{C1}=I_{C2}=I_{PTAT}$ and hence

$$I_{C3} = I_{CTAT} + \frac{I_{PTAT}}{X} \qquad (2.19b)$$

It also follows that $I_{C4}=I_{OUT}$ thus (2.19a) can be expressed as

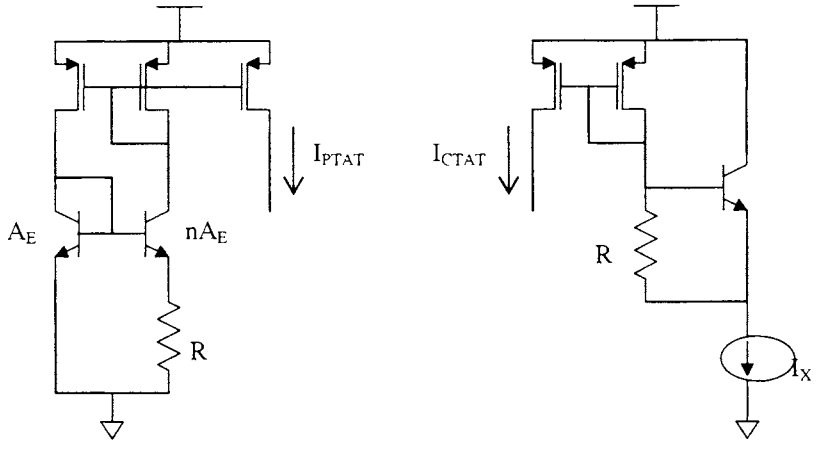
$$0 = \frac{kT}{q}\ln\left[\frac{I_{OUT}\left(\frac{I_{PTAT}}{X} + I_{CTAT}\right)}{I^2_{PTAT}}\right] \qquad (2.19c)$$

Therefore,

$$I_{OUT} = \frac{I^2_{PTAT}}{\left(\frac{I_{PTAT}}{X} + I_{CTAT}\right)} \qquad (2.20)$$

where *CTAT* stands for complementary-to-absolute-temperature. If the area factor, X, I_{PTAT} and I_{CTAT} are designed appropriately such that the sum of $\frac{I_{PTAT}}{X} + I_{CTAT}$ is temperature independent, then the output current of the I_{PTAT}^2 generator, I_{OUT}, realizes a second-order

temperature component. The circuit realizations of I_{PTAT} and I_{CTAT} generators are depicted in Figure 2.7a and 2.7b.



$$I_{PTAT} = \frac{kT}{Rq}\ln(n) \qquad I_{CTAT} = \frac{V_{BE}}{R}$$

(a) (b)

Figure 2.6(a) I_{PTAT} generator (b) I_{CTAT} generator

Generating I_{PTAT} is rather straightforward while generating I_{CTAT} may require some attention. The sink current I_X has to be greater than I_{CTAT} such that the transistor always operates in the forward-active region. To further improve the linearity of the I_{CTAT} source, a PTAT current source can be used as I_X to reduce the nonlinear effects associated with the logarithmic behavior of V_{BE} [2].

The I_{PTAT}^2 generator depicted in Figure 2.6 has major limitations because the denominator term in (2.20), $\frac{I_{PTAT}}{X} + I_{CTAT}$, is only temperature compensated to the first-order; therefore the output current of the I_{PTAT}^2 generator is not entirely second-order but instead consists of other higher-order components as well. If the I_{PTAT}^2 term is not handled

carefully, it may end up injecting nonlinear error into the reference voltage instead of compensating it.

There exist other design approaches to generate better nonlinear temperature components that attempt to achieve high order temperature compensation, for example, the piecewise-linear technique.

2.3.2 – Piecewise-Linear Technique

This technique is also based on the idea of creating nonlinear components for curvature correction. However, the nonlinear components are generated in a piecewise-linear fashion [6]. Refer to Figure 2.7a for the circuit implementation of this technique. Transistor M_1 is sourcing current that is proportional to base-emitter voltage, K_2I_{VBE}. During the lower half of the temperature range, transistor M_2 is cutoff as long as the sourcing current K_2I_{VBE} is larger than the sinking current K_1I_{PTAT}. During the upper half of the temperature range, M_2 turns on and supplies the nonlinear current, I_{NL}, when K_1I_{PTAT} exceeds K_2I_{VBE}. Figure 2.7b depicts the operation of generating the nonlinear current, I_{NL}.

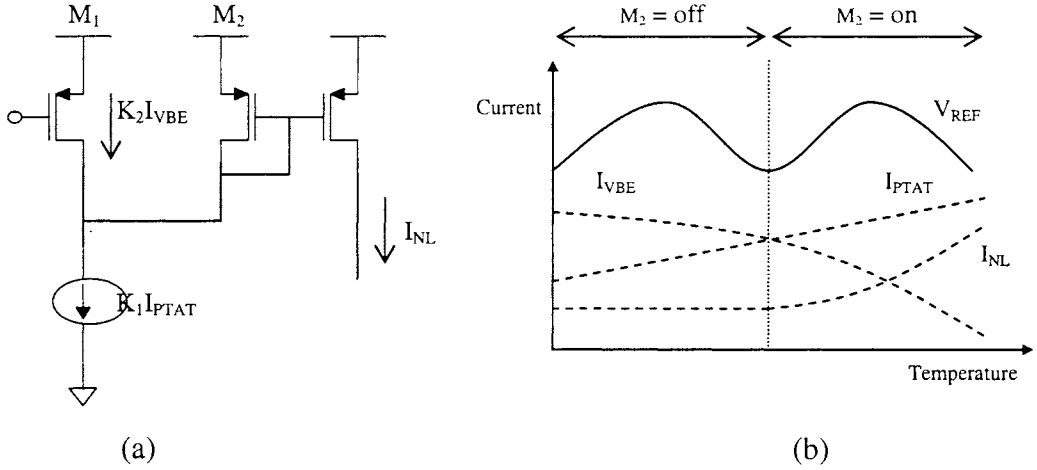


Figure 2.7 (a) Circuit that generates I_{NL} (b) realization of V_{REF} by summing I_{VBE}, I_{PTAT} and I_{NL} through resistor

The resulting nonlinear current has a piece-wise linear expression.

$$I_{NL} = \begin{cases} 0 & K_2 I_{VBE} > K_1 I_{PTAT} \\ K_1 I_{PTAT} - K_2 I_{VBE} & K_2 I_{VBE} < K_1 I_{PTAT} \end{cases} \qquad (2.21)$$

where K_1 and K_2 are the current mirror gains. To realize a voltage reference, all three components are combined with a summing resistor. The resulting voltage reference has a temperature response as depicted in Figure 2.7b.

With the three inflection points, the total variation of the reference voltage over a reasonable temperature range can be much less than is achievable with the second-order or first-order compensation techniques discussed previously. This concept can be extended to achieve higher-order compensation with even more inflection points throughout the temperature range of interest thus decreasing the total variation in the reference voltage over the range of interest to arbitrarily low levels. With this observation, one might be tempted to conclude that the field of voltage reference design has matured since the multiple inflection point approaches will yield references with arbitrarily small deviations in the output voltage over an arbitrarily large temperature range. Indeed, using models such as given by (2.5) one can readily design circuits that have simulated performance that is arbitrarily good. Reality is, however, that the industry still struggles to practically achieve performance that is even a small fraction of what is achievable with the theoretical results obtainable with the multiple inflection point approaches. For example, Analog Devices Inc., one of the industry leaders in high precision voltage references, have, at the top their live, one part, the AD588, with a temperature coefficient of ±1.5ppm/°C over a 70°C temperature range and a second part, the AD778, with a 3ppm/°C temperature coefficient over a 125°C temperature range. Both circuits require dedicated processes that include temperature stable thin film resistors which

must be individually trimmed as part of the manufacturing operation. Both parts have two inflection points. This can be contrasted to the performance of a simple trimmed first-order reference which would have approximately a 7ppm/°C temperature coefficient over the same 70°C range and approximately 13ppm/°C over the corresponding 125°C range. Without trimming, the first-order references could have temperature coefficient of 50ppm/°C to 200ppm/°C or worse.

From these observations, it should be apparent that there are some fundamental challenges associated with practically exploiting the multi-inflection point approaches and even the practical implementation of a two-inflection point approach requires expensive special-purpose processes and post-fabrication trimming.

Refer to Table 2.2 for a comparison of several state-of-the-art precision references among which include published works and commercial parts. Commercial parts that deliver state-of-the-art performance such as AD558 could cost up to US$14 per part. This is due to their exorbitant development cost which includes precision thin film resistors and laser trimming.

Table 2.2 Comparison of state-of-the-art precision references

Approach / Commercial parts	Nominal V_{REF} (V)	Temperature range (°C)	TC (ppm/°C)
Nonlinear correction [8]	0.199	0~125	3
Exponential compensation [9]	1.264	-55~125	6.65
Piecewise-linear [6]	0.595	-15~90	6.5
Analog Devices AD780	2.5	-40~85	3
Analog Devices AD588	5	0~70	±1.5

In general, almost all existing curvature correction schemes for realizing precision references have the same foundation, which is to create nonlinear temperature components to offset higher order temperature dependence of the diode voltage. However, it is a challenge itself to generate decent nonlinear temperature components. Although many circuit structures had been proposed to generate such nonlinear temperature components, most of them, if not all, are unpromising for practical high performance applications. For example, the I_{PTAT}^2 approach fails to account for the second-order effects within the I_{PTAT}^2 source itself. Furthermore, none of the schemes that were reported addresses the problems with the sensitivity to process variations.

Though often neglected, process related issues are becoming more and more important when designing high precision references. Most of the curvature correction schemes reported are extremely susceptible to process variations because the coefficients of the nonlinear terms are designed with tight margin for optimal compensation. For example, the piecewise-linear technique is based on proper selection for the coefficients of I_{VBE}, I_{PTAT} and I_{NL} in terms of circuit parameters such as current mirror gain and resistors values; nonetheless, these circuit parameters are heavily affected by process variations. For that reason, designers have to introduce trim networks in the circuits and rely on post-process

trimming in order to resolve the error caused by process variations [7-9]. Although post-process trimming is an effective way to correct process variations, it is expensive and time-consuming and often requires iterative thermo-cycling of the circuit during trim.

With the concerns mentioned above in mind, an alternative design approach is proposed in the next chapter to address both performance and process related issues for designing high performance precision references.

3. PROPOSED CURVATURE CORRECTION APPROACH

Some observations and insights on the first-order references need to be mentioned before the proposed approach is discussed.

3.1 – First-Order Voltage References (Review)

For first-order references, equation 2.10 can be simplified to the following form by substituting x=1:

$$V_{REF} = V_{go} + (\eta - 1)\frac{kT}{q}\left[1 + \ln\left(\frac{T_o}{T}\right)\right] \tag{3.1}$$

The derivative of V_{REF} is obtained to examine its temperature discrepancy

$$\frac{\partial V_{REF}}{\partial T} = (\eta - 1)\frac{k}{q}\ln\left(\frac{T_0}{T}\right) \tag{3.2}$$

By construction, V_{REF} has an inflection point at T=T_0 and $\frac{\partial V_{REF}}{\partial T}\Big|_{T=T_0} = 0$, and $\frac{\partial V_{REF}}{\partial T}$ is small for T near the inflection point. The temperature discrepancy increases significantly for T that is appreciably away from T_0 because the reference error ΔV_{REF} grows exponentially. Table 3.1 shows a comparison of ΔV_{REF} for a ±100°C window around T_0.

Table 3.1 A comparison of $\frac{\partial V_{REF}}{\partial T}$ for several T-T_0 values (η=2.3, T_0=300°K)

T-T_0, °C	$\partial V_{REF}/\partial T$	ΔV_{REF}, μV	TEMPCO, ppm/°C
0	0	0	0
10	3.80E-06	19	1.85
20	7.74E-06	73	3.66
50	2.05E-05	444	8.87
100	4.55E-05	1690	16.92

Although the ΔV_{REF} value is a close approximation to the actual change in V_{REF} in the neighborhood or T_0, the approximations are somewhat pessimistic for $T\text{-}T_0$=50°C and 100°K. Figure 3.1 shows a plot of (3.1) over a ±100°C temperature range and explicitly shows the deviations in V_{REF}.

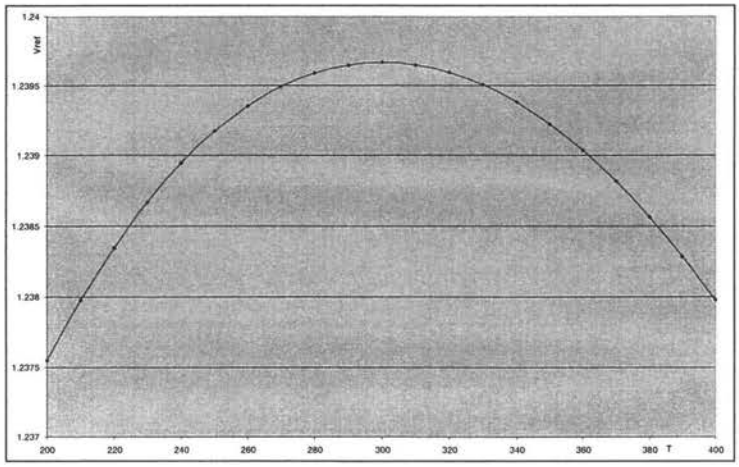


Figure 3.1 V_{REF} vs. temperature

Observe from Figure 3.1 that ΔV_{REF} is 73μV for a temperature range of T_0+20°C, and the error increases to .444mV as the temperature range grows to T_0+50°C and to 1.69mV at T_0+100°C. The deviation of 1.69mV at T_0+100°C represents a change in the reference voltage of approximately 0.14%. This is equivalent to an error of 1LSB in a 9.5 bit data converter. To put this in perspective, if this reference were used in a data converter, many applications will require that the total error due to all error mechanisms be at most ±½ LSB. If 25% of this error budget were allocated to errors in V_{REF}, the total acceptable error in V_{REF} would be $\pm{}^1/_8$ LSB. The error of 0.14% in the first-order reference would correspond to an error of $^1/_8$ LSB of a 5.5 bit data converter. It can be concluded that the error in reference voltage for the first order reference is much too large to make this reference useful in even

moderate performance applications with considerable demand for references that have a deviation with temperature from a factor of 10 to a factor of 100 better than what is achievable with the first-order references.

Based on the observations presented above, a design approach for building very stable references that operate over a wide temperature range is proposed. This approach will take advantage of the property of the first-order references at T near the inflection point ($T=T_0$) and places multiple inflection points ($\frac{\partial V_{REF}}{\partial T}\Big|_{T=T_0}=0$) across the temperature range of interest. Corresponding to each inflection point is a narrow temperature window over which the reference must operate and since the temperature window is narrow, the reference error will be low [15].

3.2 – Multiple Inflection Points Approach

Recall that the first-order references compensate the negative temperature dependence of the diode voltage, V_{BE}, with a positively temperature dependent PTAT voltage (Refer to Chapter 2 for detail). The PTAT voltage is designed to provide the inflection point at $T=T_0$. A plot of the temperature coefficient of a first-order references as a function of the deviation from T_0 can be obtained from (1.4) and (2.10) and is shown Figure 3.1.1. From this figure it is apparent that first-order reference performs quite well provided T_0 can be precisely determined and provided the temperature range around T_0 does not get too large. With this in mind, consider the design of a first-order reference with multiple inflection points obtained by discretely altering the PTAT voltage as the temperature changes

[15]. With this approach, the temperature coefficient of the resultant reference should be small in the neighborhood of each inflection point.

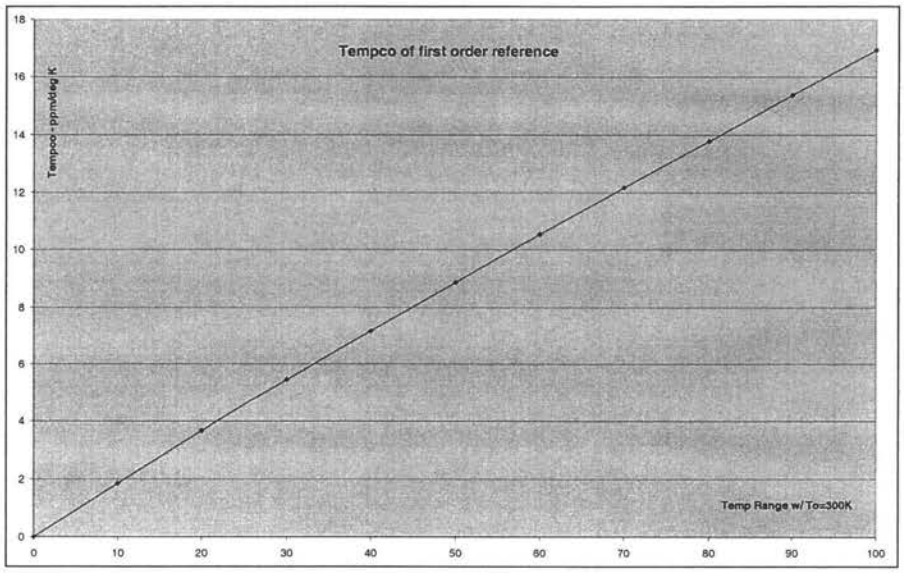


Figure 3.1.1 TEMPCO of first-order reference

Figure 3.1 depicts a circuit that has discretely configurable PTAT that can generate two PTAT voltage references. This circuit is derived from the circuit depicted in Figure 2.3 by replacing R_1 with two switched-resistors, R_{1A} and R_{1B}.

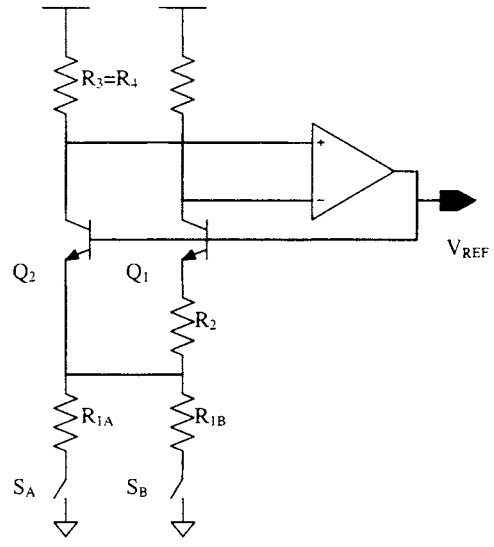


Figure 3.1.1 Bandgap voltage reference circuit with switch-able PTAT

The design equation for the switch-able bandgap circuit depicted in Figure 3.1.a is:

$$V_{REF} = V_{BE2} + \underbrace{\frac{2(S_A R_{1A} + S_B R_{1B})}{R_2} \Delta V_{BE}}_{V_{PTAT}} \qquad (3.3)$$

The V_{PTAT} term is configured to provide $V_{PTAT\text{-}A}$ when S_A is on and $V_{PTAT\text{-}B}$ when S_B is on. A graphical illustration on how the configurable V_{PTAT} alters the temperature response of V_{REF} is depicted in Figure 3.2. The resistors R_{1A} and R_{1B} are chosen such that when S_A is on (S_A=1), V_{REF} has an inflection point at $T_{0\text{-}A}$ and so that the inflection point moves to $T_{0\text{-}B}$ when S_B is on (S_B=1).

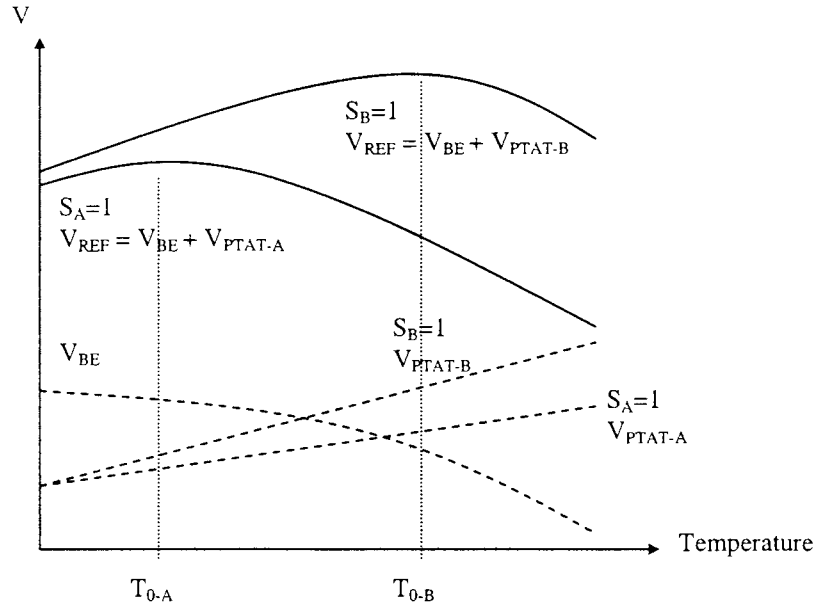


Figure 3.2 Configurable V_{PTAT} and the resulting V_{REF}

A temperature trigger point in the middle of the desired operating temperature range, T_{middle}, is selected such that S_A is turned on for all temperatures lower than T_{middle} and S_B is turned on for all temperature greater than T_{middle}. The resulting V_{REF} is characterized by a piecewise continuous function that has two inflection points, one at T_{0-A} and the other one at T_{0-B}. A graphical illustration is depicted in Figure 3.3. Although the local temperature coefficients and small, the overall temperature coefficient of this circuit as defined by (1.4) will be quite large because of the discontinuity at T_{middle}.

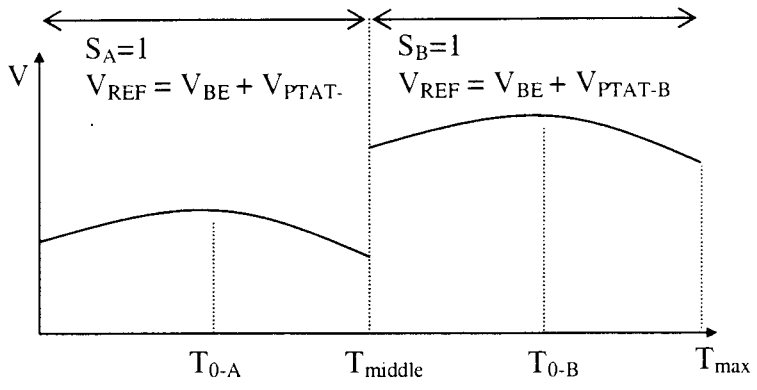


Figure 3.3 V_{REF} with multiple inflection points

3.3 – Determining shift level for removing discontinuity

To achieve good performance over a wide temperature range, it is necessary to remove the discontinuity of V_{REF} at $T=T_{middle}$. One way to remove the discontinuity is to add a resistor string level-shifter at the output of the reference circuit as depicted in Figure 3.4. By appropriately choosing R_5 and R_6, continuity at the temperature trigger point, T_{middle}, can be obtained. The adjusted response is depicted in Figure 3.5. A dramatic reduction in the temperature coefficient over the temperature range T_{max} - T_{min} can be obtained by using two inflection points and of continuity is maintained at the trigger temperature.

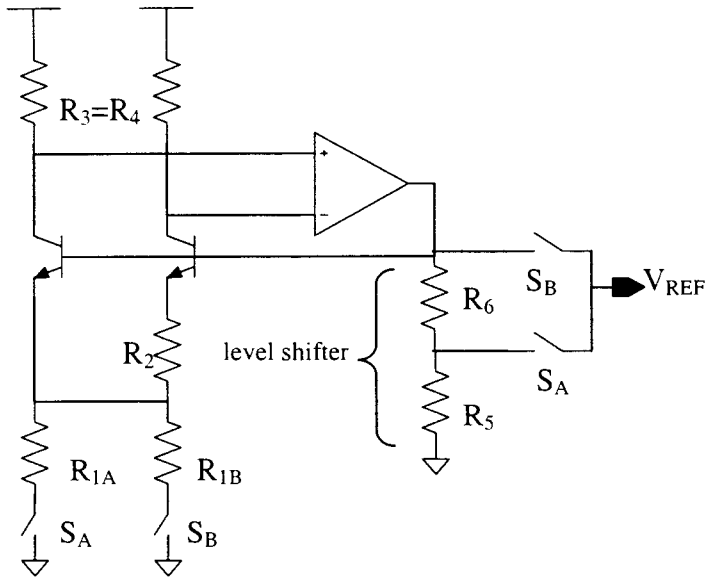


Figure 3.4 Level shifted added to remove discontinuity

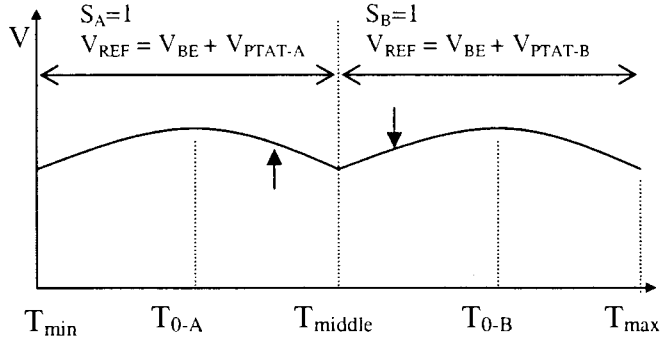


Figure 3.5 V_{REF} with multiple inflection points and adjusted DC level

Precise positioning of the two inflection points, $T_{0\text{-}A}$ and $T_{0\text{-}B}$, and removing the discontinuity at the T_{middle} does require some effort. Procedures for trimming a standard first-order bandgap reference by adjusting R_{1A} or R_{1B} to obtain an inflection point at a desired operating temperature, $T_{0\text{-}A}$ and $T_{0\text{-}B}$, are tedious but well known. Additional comments about

trimming a standard first-order bandgap reference will be discussed later. Thus, it will be assumed that first R_{1A} and R_{1B} have been trimmed with S_A and S_B closed respectively to obtain inflection points at $T_{0\text{-}A}$ and $T_{0\text{-}B}$ respectively. It will now be assured that a temperature sensor circuit exists that has a digital output that increases monotonically with temperature and that the resolution can be set at any desired level. Practically, a resolution of 1bit/°K should be adequate. A block diagram of such a circuit is shown in Figure 3.5.1.

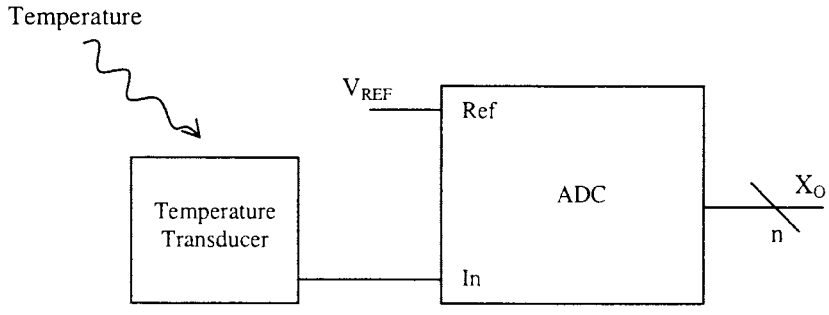


Figure 3.5.1 Monotone Digital Temperature Sensor

Although details of the digital temperature sensor will not be provided, some properties of the temperature sensor will be described. If the ADC has infinite resolution, the ADC has an input/output relationship

$$V_O = \theta_K \frac{V_i}{V_{REF}} \tag{3.3a}$$

where θ_K is a constant dependent upon the architecture of the ADC. If the resolution is finite, the signal $\theta_K \frac{V_i}{V_{REF}}$ is passed through a quantizer. To guarantee the output is monotone with respect to temperature, we must have

$$\frac{dV_O(T)}{dT} = \theta_K \cdot \frac{V_{REF}(T)\frac{dV_i(T)}{dT} - V_i\frac{dV_{REF}(T)}{dT}}{V_{REF}^{\ 2}(T)} > 0 \qquad (3.3b)$$

for all T in the temperature range of interest. This implies

$$\frac{dV_i(T)}{dT} > \frac{V_i(T)}{V_{REF}(T)} \cdot \frac{dV_{REF}(T)}{dT} \qquad (3.3c)$$

This inequality can be practically maintained over an operating range of interest in many ways one of which entails using a first-order bandgap for V_{REF} (T) and a PTAT voltage reference for V_i (T).

Assume now the temperature of the circuit is adjusted to T_{middle} and the corresponding digital output of the temperature sensor is stored in memory. The output of the Digital Temperature Sensor can then be monitored and if the output exceeds that stored in memory, the switch S_B is closed and if it is less than or equal to that stored in memory, S_A is closed.

Two procedures for maintaining continuity at the trigger temperature T_{middle} will now be described. In the first, during calibration at manufacturing, temperature will be increased from below T_{middle} until the output code of the digital temperature sensor increases to 1LSB above the value stored in the digital memory. During this temperature adjustment, the output of V_{REF} will be monitored with a digital volt meter and at the time the 1LSB increase occurs, the value on the volt meter will be stored in tester memory. After this value is stored, S_A will be opened and S_B will be closed and R_5 or R_6 will be trimmed so that the output, V_{REF}, equals the value just before the transition. The trimming of R_5 or R_6 should be done quickly enough so that no significant change in temperature occurs during the trimming.

A second calibration algorithm will now be described. Assume the trigger temperature is set at manufacturing. At power up of the references, either S_A or S_B will be

closed depending upon whether the output of the Digital Temperature Sensor indicates the temperature is below or above $T_{TRIGGER}$ respectively. Without loss of generality, assume that the temperature was below $T_{TRIGGER}$ at startup. The temperature is simply monitored with the digital temperature sensor and if the temperature never exceeds $T_{TRIGGER}$, no further action is necessary. However, if at any point in time the temperature exceeds $T_{TRIGGER}$, as evidenced by a 1LSB increase above the stored trigger value, the circuit will be field-trimmed for continuity. The trigger condition will start the following chain of events which will be completed in a sufficiently short time frame that no substantial change in temperature occurs during this even sequence.

Upon receiving the trigger signal, the output of the reference will be input into the ADC of the Digital Temperature Sensor and the output will be stored in local RAM. The switch S_A will remain closed while this voltage is measure. Then S_A will be opened and S_B closed and the voltage V_{REF} will again be input into the ADC of the Digital Temperature Sensor. R_5 or R_6 will be electrically adjusted until the output of the ADC agrees with that stored in RAM. The trim coefficients for R_5 or R_6 will be stored in RAM. The trimming is now complete. On subsequent crossing of the trigger temperature, the stored values for the trimmed values of R_5 or R_6 will be used and no additional trimming will be required. Refer to Figure 3.6 for the operation flow graph of this second trimming algorithm.

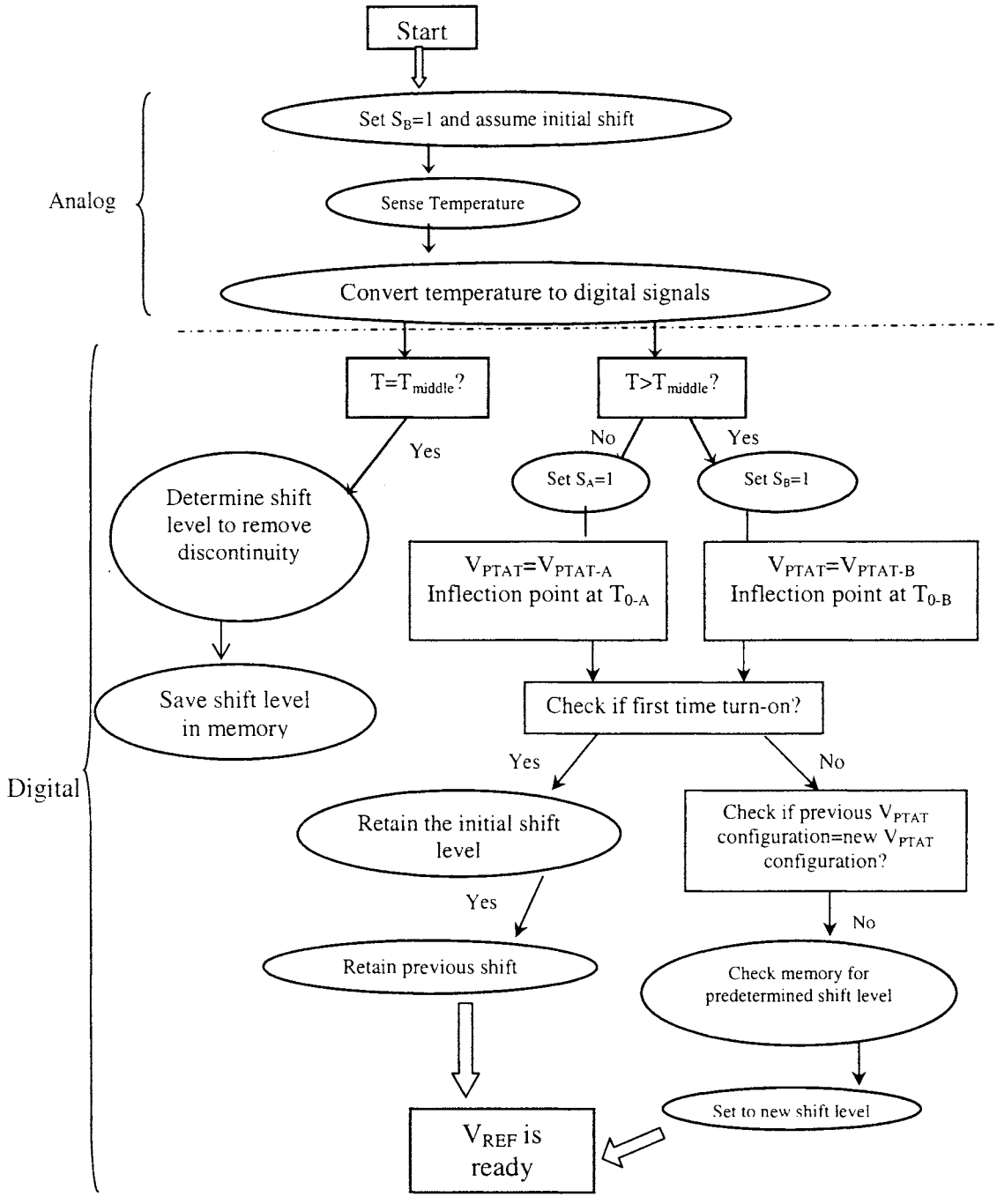


Figure 3.6 Operation flow graph of the multiple inflection points voltage reference system

The circuit of Figure 3.4 and the subsequent trimming algorithms can be readily extended to include 3 or more inflection points with the corresponding reduction in the overall TEMPCO.

An approximate expression for the number of inflection points needed and the resulting temperature coefficient for a given temperature range will now be derived. The TEMPCO curve of Figure 3.1.1 was derived under the assumption that the inflection point was at T_0=300°K. The TEMPCO is approximately given by the expression

$$TEMPCO \approx m(T_O) \cdot T_{range} \tag{3.4}$$

where

$$m(T_O) \approx \begin{cases} .06\,ppm/(^\circ K)^2 & T_O = 250^\circ K \\ .05\,ppm/(^\circ K)^2 & T_O = 300^\circ K \\ .04\,ppm/(^\circ K)^2 & T_O = 350^\circ K \end{cases} \tag{3.5}$$

If we assume $m(T_O) \approx .05$, then it follows from (3.4) for a k-segment approximation with uniform inflection points that the equivalent TEMPCO is approximately given by

$$TEMPCO \approx \frac{(.05)T_{range}}{k^2}\, ppm/(^\circ K)^2 \tag{3.6}$$

Thus, the equivalent temperature coefficient decreases approximately with the square of the number of segments. For example, it follows from (3.6) that a voltage reference with a TEMPCO of 1ppm/°C over a temperature range from 0°C to 80°C is realizable by placing an inflection point at 20°C, and another inflection point at 60°C. The temperature response for this voltage reference is depicted in Figure 3.7b and compared with a single inflection point reference in Figure 3.7a. If four inflection points instead of two are placed over the same temperature range as depicted in Figure 3.7c, ΔV_{REF} can be driven down to 20μV. On the

other hand, if the four inflection points are used to extend the temperature range as depicted in Figure 3.7d, the same accuracy performance is retained but the operating temperature range has been doubled. In Figure 3.7e, eight inflection points are inserted to drive down ΔV_{REF} and extend the operating temperature range.

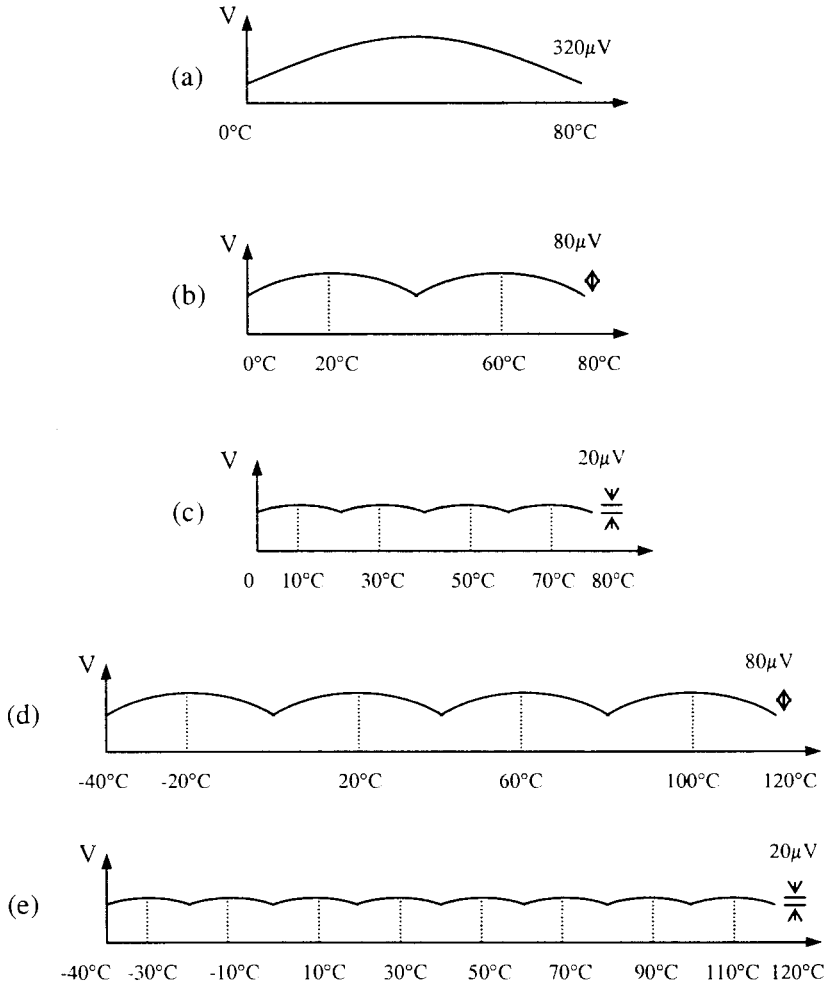


Figure 3.7 (a) single inflection point (b) two inflection points (c) improved accuracy (d) extended temperature range (e) improved accuracy and extended temperature range

The performance potential of the multiple inflection point compensation should be apparent from these examples. It should also be observed, however, that the performance predicted in Figure 3.7 far exceeds anything reported in the literature or anything available commercially. The TEMPCO of 1ppm/°C over the 80°C range for the example of Figure 3.7 is better than that of the Analog Devices AD558 discussed previously. The 4-segment and 8-segment structures have even lower TEMPCOs!

4. PROCESS VARIATIONS

Like all other approaches for designing precision references, the performance of the multiple inflection point approach introduced in the previous chapter is sensitive to process variations. Two tuning algorithms were described in the precious chapter but both were dependent upon having already established the inflection points at the desired temperature. In most precision reference circuits, trimming is done at manufacturing to locate the inflection points at the desired values. This trimming operation is costly. In this section, the sensitivity of the inflection points to process variations will be considered. This discussion will show that trimming is necessary to obtain precision performance. In the next section a new strategy for doing self-trimming of the inflection points will be introduced.

If we define the temperature independent variables H and θ by

$$H = \frac{\beta k}{q}\ln(\gamma\upsilon) - \left[\frac{V_{go} - V_{BE}(T_0) + (\eta - x)V_{T0}}{T_0}\right] \tag{4.1}$$

and

$$\theta = \frac{(\eta - x)V_{T0}}{T_0} \tag{4.2}$$

$$\beta = 2\frac{R_1}{R_2} \tag{4.2a}$$

where

$$\gamma = \frac{I_{C2}}{I_{C1}} \tag{4.2b}$$

$$\upsilon = \frac{A_{E2}}{A_{E1}} \tag{4.2c}$$

then it follows from (2.3) that the reference voltage of the bandgap reference can be expressed as

$$V_{REF} = V_{go} + (\eta - x)V_{T0} + HT + \theta\left[T\ln\left(\frac{T}{T_0}\right) - T + T_0\right] \tag{4.3}$$

Taking the partial of V_{REF} with respect to T and setting this to 0 we obtain an expression for the inflection point, T_{INF}

$$T_{INF} = T_0 e^{H/\theta} \tag{4.4}$$

The sensitivity of T_{INF} with respect to β, γ and υ at $T=T_0$ will now be obtained. These sensitivities are defined respectively by

$$S_{\beta}^{T_{INF}} = \frac{\partial T_{INF}}{\partial \beta} \cdot \frac{\beta}{T_{INF}}\bigg|_{T=T_0} \tag{4.5}$$

$$S_{\gamma}^{T_{INF}} = \frac{\partial T_{INF}}{\partial \gamma} \cdot \frac{\gamma}{T_{INF}}\bigg|_{T=T_0} \tag{4.6}$$

$$S_{\upsilon}^{T_{INF}} = \frac{\partial T_{INF}}{\partial \upsilon} \cdot \frac{\upsilon}{T_{INF}}\bigg|_{T=T_0} \tag{4.7}$$

A routine analysis gives the following results:

$$S_{\beta}^{T_{INF}} = \frac{V_{go} - V_{BE}(T_0) + (\eta - x)V_{T0}}{(\eta - x)V_{T0}} \tag{4.8}$$

and

$$S_{\gamma}^{T_{INF}} = S_{\upsilon}^{T_{INF}} = \frac{\beta}{\eta - x}\bigg|_{T=T_0} \tag{4.9}$$

Substituting in typical values for V_{go}=1.206V, $V_{BE}(T_0)$ =0.6V, η=2.3, x=1, and V_{T0} =25mV at T_0=300°K gives

$$S_{\beta}^{T_{INF}} \approx 19 \tag{4.10}$$

and for $\frac{I_{C2}}{I_{C1}} \cdot \frac{A_{E2}}{A_{E1}} = 4$,

$$S_{\gamma}^{T_{INF}} = S_{\upsilon}^{T_{INF}} = 13 \tag{4.11}$$

If we now approximate the change in the inflection point due to a variable X change of ΔX

$$\Delta T_{INF} \approx \left(S_X^{T_{INF}}\right) T_{INF} \frac{\Delta X}{X} \tag{4.12}$$

then a ±1% error in β would cause about a ±19% change in T_{INF} and if T_{INF}=300°K, $|\Delta T_{INF}|$ would be approximately 60°K! Likewise, a 1% error in the emitter area ratios or the collector currents would cause around a 14% change in T_{INF} which would be about 40°K change in T_{INF}. Since the sensitivities of these circuits are so large, the accuracy of (4.12) in predicting the change in the inflection point, even for reasonably small $\frac{\Delta X}{X}$ is of concern. A computer simulation of (4.3) with υ=1, γ=4, T_0=300°K and η=2.3 was run. The value of β needed to achieve T_{INF}=300°K is that needed to make H in (4.1) 0, which is

$$\beta = \frac{V_{go} - V_{BE}(T_0) + (\eta - x)V_{T0}}{V_{T0} \ln(\gamma\upsilon)} \tag{4.13}$$

With the values specified for υ, γ, η and T_0, we obtain β=16.4574. Simulations for a +1% error and a -1% error in β show inflection points at 358.4°K and 251.8°K respectively which is reasonably close to the 360°K and 240°K predicted by the sensitivity analysis.

From the material presented in the previous chapter, it is apparent that the inflection points must be controlled to a few °K for the two inflection point scheme to work properly and even somewhat tighter for the 4 inflection point strategy to be useful. This would require

control of β, current ratios, and emitter area ratios to around .01% which is not practically achievable without trimming in existing processes. It can be concluded that the deviation of the inflection points from their ideal location has a profound impact on the performance of the multiple inflection point approach. Figure 4.1a and 4.1b depict graphically how process variations impact the performance of the multiple inflection point approach if the continuity algorithm is used but if the inflection points are not correctly placed.

(a) Inflection points moved to lower temperature due to insufficient PTAT

(b) Inflection points moved to higher temperature due to excessive PTAT

Figure 4.1 The performance of the multiple inflection points approach suffers due to process variations.

Two algorithms for maintaining continuity at the trigger temperatures were discussed in the previous chapter. Two strategies for locating the inflection points at the desired values are discussed in the next section.

4.1 – Inflection Point Correction Strategies

In this section, two methods for adjusting the inflection points are discussed. The first is a review of a standard strategy used during the manufacturing process for trimming bandgap references on a production tester. Techniques such as this are widely used in industry. The second is a new approach that does not require a production tester thus offering potential for dramatic reduction in cost and compatibility with standard high-volume semiconductor processes.

In high-volume semiconductor production, the voltage reference circuits are characterized by measuring a large number of samples of the circuits. The measurement is done by thermo-cycling each circuit and determining the trim bit to set the trim networks in the circuit for optimum performance. The characterization results are then averaged to obtain a standard trim bit. This trim bit will be used to trim all circuits in the same production without having to characterize the circuits. This approach is sometimes termed batch trimming. The advantage of this approach is that the time consuming and expensive characterization procedures are performed only once. However, this approach relies heavily on the correlation between wafers for the trimming to be effective. Variants of the bandgap trimming operation and of bandgap circuits have appeared recently in the literature [7-13].

The post-process trimming method has proven effective for correcting process variations. However, employing the post-process trimming method on reference circuits is expensive and time consuming because it requires thermo-cycle process on a tester and often expensive laser trimming systems that are suitable for wafer level trimming but not well-suited for post-packaging trims. The ambient temperature is controlled in order to measure and trim the temperature response of the reference circuits under test. Often, the

measurement and trimming procedures are performed iteratively to optimize the trimming results but iterative trimming algorithms require even more tester time. An on-chip self-calibration scheme has been developed as part of this work to correct the inflection point error caused by process variations in a low cost manner while avoiding the post-process trimming procedures. It is introduced in the next section.

4.2 – On-chip Correction Scheme

Consider the temperature responses depicted in Figure 4.2 which belong to three first-order voltage references with different inflection points. A family of curves such as this would be obtained from either of the circuit of Figure 4.2.1 if k=3 and exactly one of the switches are closed. If a measurement is made on each reference at temperature T_1 and temperature T_2, where $T_2>T_1$, some information about the location of the inflection point can be obtained.

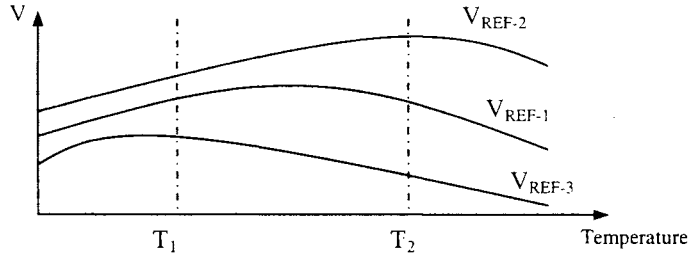
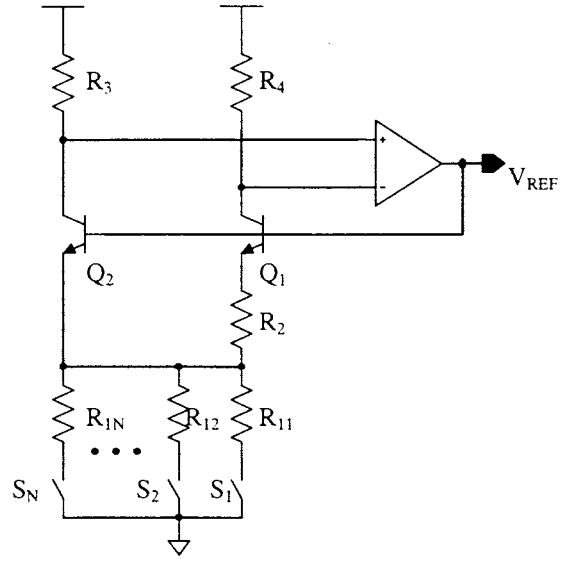
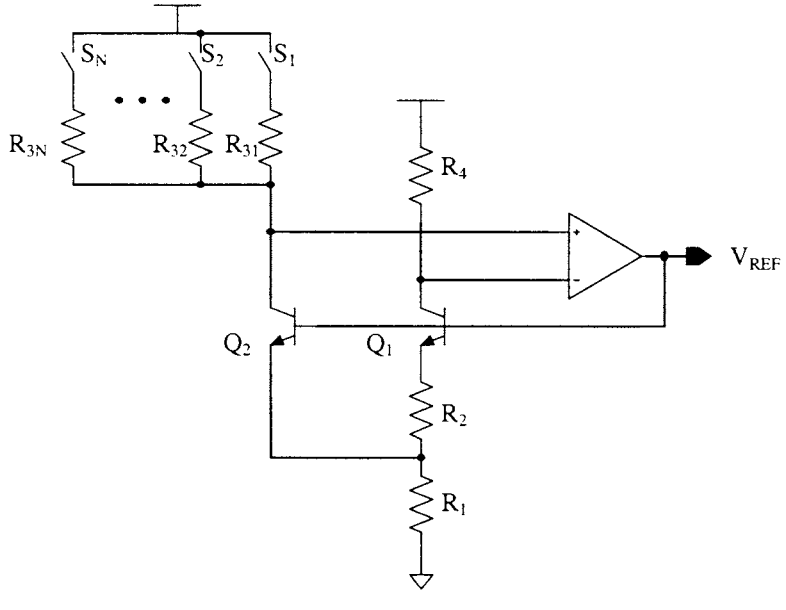


Figure 4.2 Temperature responses of three reference circuits with different inflection point's locations



(a)



(b)

Figure 4.2.1 Multiple inflection point circuits

If the measurement at T_2 is less than the measurement at T_1, the inflection point must be to the left of T_2 and if the measurement at T_2 is greater than the measurement at T_1 it must be to the right of T_1. If the measurement at T_1 and T_2 were precisely the same, the inflection point must be between T_1 and T_2. If the resistors R_{1k} or the resistors R_{3k} are monotonically increasing or decreasing in value, it can be shown that the corresponding inflection point are also monotone increasing or decreasing with k. For notational convenience, it will be assumed that the inflection points are monotone increasing with the index k. It thus follows that there exists an index k_1 such that the inflection points are larger than T_1 for $k \geq k_1$ and less than T_2 for $k < k_1$. Furthermore, this index k_1 can be obtained by the measurement of the reference voltages at T_1 and T_2. There also exists a $k_2 \geq k_1$ and a $k_3 < k_1$ such that the inflection point is larger than T_2 for $k > k_2$ and it is less than T_1 for $k < k_3$. These conditions are depicted in Figure 4.2.2. For any k in the interval $[k_3, k_2]$, the inflection points will be between the temperature T_1 and T_2.

Our goal is to determine a value of an index *k* so that the voltage reference has an inflection point in the interval $[T_1, T_2]$. If N is small, the value of k_1 may equal k_2 and there would be no inflection points in the interval $[T_1, T_2]$. If the circuit is, however, designed to guarantee that there is always at least one inflection point in any interval of length T_2-T_1, then it follows that the reference corresponding to index k_1 has an inflection point between T_1 and T_2. From a practical viewpoint, it is easy to design a circuit that is guaranteed to have several inflection points in an interval of length T_2-T_1 even in the presence of typical process variations.

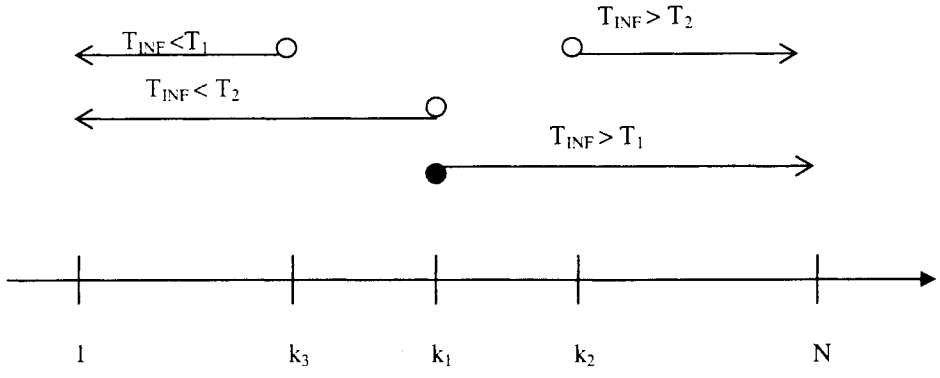


Figure 4.2.2 Relation between index k and inflection point

4.2.1 – Calibration Strategy

Consider the bandgap voltage reference circuit of Figure 4.2.1b redrawn in Figure 4.3. The switched-resistor array is a trim network that can compensate for deviations of the circuit parameters due to process variations.

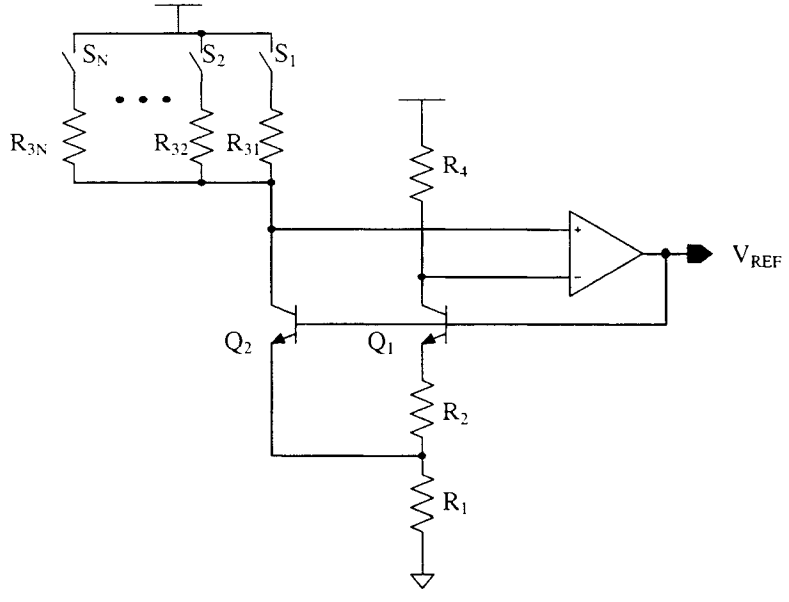


Figure 4.3 Bandgap voltage reference circuit with trim network

It follows from (4.13) that the following equation must be satisfied to place an inflection point at a temperature T_0.

$$\frac{2R_1}{R_2} = \frac{V_{go} - V_{BE2}(T_o) + (\eta - x)V_{T_o}}{T_o \cdot \frac{k}{q} \ln\left(\frac{I_{C2}}{I_{C1}} \cdot \frac{A_{E1}}{A_{E2}}\right)} \tag{4.13}$$

With the trim strategy of Figure 4.3, R_3 can be adjusted to trim the current ratio $\frac{I_{C2}}{I_{C1}}$ to the value needed to satisfy (4.13). Figure 4.4 depicts how R_3 changes the inflection point. The size of the trim network needs to be large enough to account for worst-case variations of process parameters around each desired inflection point.

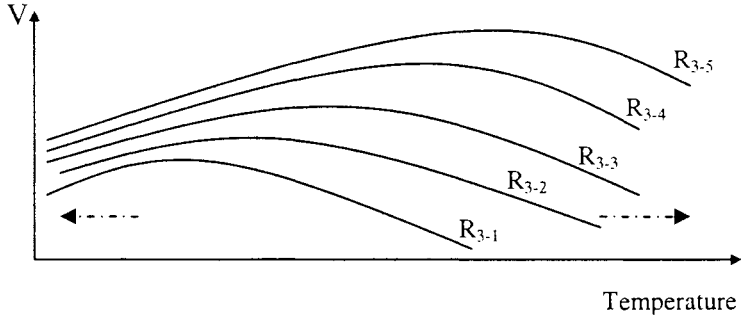


Figure 4.4 Inflection point is altered by R_3 configuration

A strategy for establishing inflection points at M_1 trigger temperatures, $T_1 \ldots T_{M1}$ will now be established. This will be based upon the assumption that V_{REF} measurement can be made at a temperature T_X and $T_X+\Delta T$, where ΔT is greater than the median of two adjacent inflection points. A method for on-chip measurements at two temperatures separated by a temperature ΔT will be discussed later in this section.

Assume the inflection temperatures $T_1 \ldots T_{M1}$ are stored in memory and the temperature of the voltage reference is sensed by the Digital Temperature Sensor of Figure 3.5.1. The exact value of the trigger temperatures is not critical but the separation between the trigger temperatures is of more concern. The latter, however, is not highly process sensitive. In the discussion that follows, three inflection points ($M1$=3) was assumed to facilitate the narration. However, the idea can be generalized to any number of inflection points. First, create a set of trigger temperatures, $\{T_{T1} \ldots T_{TM1}\}$, where

$$T_{TK} = \frac{T_k + T_{k-1}}{2} \tag{4.13a}$$

The trigger temperatures set defines the temperatures at which transitions are made between adjacent inflection points. Then, create a set of alternate trigger temperatures, $\{T_{1a} \ldots T_{ka}\}$, where

$$T_{ia} = T_i - \frac{\Delta T}{2} \tag{4.13b}$$

The alternate trigger temperatures set defines the temperatures at which inflection point measurements are performed and captured. On power up, the initial temperature which the reference first operates at is called T_{init}. There are two conditions of T_{init} to be considered.

In case one, T_{init} is less than T_{2a} but is greater than T_1. The ADC of the Digital Temperature Sensor will be used to measure the output of the reference at temperatures T_{init} and $T_{init}+\Delta T$ for values of R_{3k}, k=1 … N and the value of R_{3k} that places an inflection point of the reference at T= $T_{init}+\Delta T/2$ will be determined. From this value of k and the nominal resolution of the inflection point with temperature, an estimate of the value of R_{3k} that has an inflection point closest to T_{init} will be made. Call this R_{3kinit}. The switch corresponding to R_{3kinit} will be closed, the output of the reference will now be available and the output of the

Digital Temperature Sensor will be between two trigger temperatures in the alternate temperature trigger set. At this point, the Digital Temperature Sensor will enter a watch mode waiting for the output of the Digital Temperature Sensor to cross one of the alternate temperature trigger points. If that never occurs, the output of the reference will be operating near the inflection point corresponding to R_{3kinit} and the reference voltage will deviate little from the initial value. Without loss of generality, assume the operating temperature increases so that an alternate temperature trigger is crossed, say T_{2a}. At the time this temperature crossing occurs, measurements of the reference output will be made at this alternate trigger temperature and at the alternate trigger temperature $+\Delta T$ to determine which value of R_{3k} has an inflection point near trigger temperature T_2. This is essentially the same procedure that was depicted in Figure 4.2.2. The corresponding reference outputs are depicted in Figure 4.5. The digital code that controls the corresponding switch for R_{3k} will be stored in memory and the alternate trigger point corresponding to k=2 will be removed from the alternate trigger point set. If the temperature increases further and temperature T_{T2} is reached, the output of the reference will be measured with the ADC of the Digital Temperature Sensor and this value will be temporarily stored in digital memory. The switch corresponding to R_{32} will then be closed and a digitally controlled level shift of the reference output will be made until the output of the ADC agrees with the value stored in the temporary memory. The level shift may be similar to that used in Figure 3.4. This will provide continuity between the reference with R_{3init} and with R_{32} and the digital signal that provides the appropriate offset for k=2 will be stored in memory. If the temperature decreases from T_2 to T_{T2}, the reference will switch to the temperature curve that has inflection point at T_{init}. Until the temperature reaches T_{1a}, the reference will determine the inflection point closest to T1, and the digital code that controls

the switch for R31 is stored in memory and the alternate trigger point corresponding to k=1 will be removed from the alternate trigger point set. This procedure will be continued with further increases in temperature sequentially either determining an inflection point near a trigger point or establishing continuity in the transfer characteristics at the trigger points.

In case two, T_{init} is greater than T_{T3}. The reference will first place an inflection point near T_{init} on power up. Assume the temperature decreases until it reaches T_{3a}. At the time T_{3a} is crossed, an inflection point near T_3 will be determined. However, the reference stays on the T_{init} curve and does not switch to the T_3 curve until later. As the temperature decreases further and T_{T2} is crossed, an inflection point near T_{T2} is determined and the corresponding curve is called T_{init1} curve. A transition is made from the T_{init} curve to the T_{init1} curve by first removing the offset between the two curves. When the temperature reaches T_{2a}, an inflection point near T_2 is determined. Likewise, an inflection point near T_1 is determined when the temperature reaches T_{1a}. If the temperature increases, the reference will stay on T_{init1} curve and then switch to T_{init} curve at temperature T_{T2}. When T_{T3} is crossed, the reference will switch to T_3 curve with the offset between T_{init} curve and T_3 curve removed. Then, the offset between T_3 curve and T_2 curve is also removed. Likewise, the offset between T_2 curve and T_1 curve is removed at temperature T_{T1}.

Of course, anytime a trigger temperature is subsequently crossed in either direction, the corresponding R_{3k} will be changed so that the reference is always operating near an inflection point. A similar procedure can be used to determine the resistor settings and the offset settings if the temperature decreases below T_{init}. It should be apparent that the determination of the values of R_{3k} needed for each inflection point need only be done once since the digital signal that controls the corresponding switches is stored in memory. If the

circuit ever traverses its entire thermal operating range in the field, no further measurements of resistor values or determination of inflection points would need to be made. It should also be apparent that this calibration strategy is done in the field so it does not require any test equipment and it is not subject to either packaging or mounting stresses that may shift the trim performance of parts that were trimmed at the wafer level.

A discussion of the resolution needed for the adjustment of the R_3 resistor and the trim resistors may be of some use. In what follows we will attempt to give a simple qualitative discussion that should provide a good estimate for the number of bits of resolution needed in the R_1 resistor. Assume that we are interested in obtaining thermal stabilization over a 200°C temperature range and that our goal is to place inflection points with a nominal resolution of 5°C. It will also be assumed that the sensitivity of the inflection point to β, υ, and γ as defined in (4.2a), (4.2b), and (4.2c) are all 20. This is nominally larger than the value of the sensitivity calculated earlier and will provide a modestly pessimistic estimate for the resolution.

First, the adjustment range in β, υ, or γ needed to compensate for process variations in β, υ, and γ will be determined along with that needed to provide operation over a 200°C operating range. If ΔT is the total adjustment range required, it follows from (4.12) that

$$\Delta T_{INF} \approx T_{INF}\left(S_{\beta}^{T_{INF}} \frac{\Delta\beta}{\beta} + S_{\gamma}^{T_{INF}} \frac{\Delta\gamma}{\gamma} + S_{\upsilon}^{T_{INF}} \frac{\Delta\upsilon}{\upsilon} \right) + 200 \qquad (4.14)$$

Substituting $S_X^{T_{INF}} = 20$, $X \in \{\beta, \upsilon, \gamma\}$, assuming $\left|\frac{\Delta X}{X}\right| < .02$, $X \in \{\beta, \upsilon, \gamma\}$, and observing $T_{INF}<400°K$, it follows that $|\Delta T|< (400)\ (20)\ (.02)\ (3) + 200=680°K$. To provide this adjustment with β (or γ), it follows from (4.12) that

$$\frac{\Delta\beta}{\beta} = \frac{680}{(20)(200)} = .17$$

Thus an upper bound on the variation in β is 20%. For a resolution of 5°C, it follows again from (4.12) that

$$\frac{\Delta\beta}{\beta} = \frac{5}{(20)(400)} = 6.25E-4 \approx .06\%$$

Thus, $\frac{\Delta\beta}{\beta}$ must be quantized into $\frac{20}{.06} \approx 330$ levels. This will require approximately 9 bits of resolution fro the adjustment of β. This simple analysis was quite conservative and it is likely that 5 or 6 bits of resolution would be adequate.

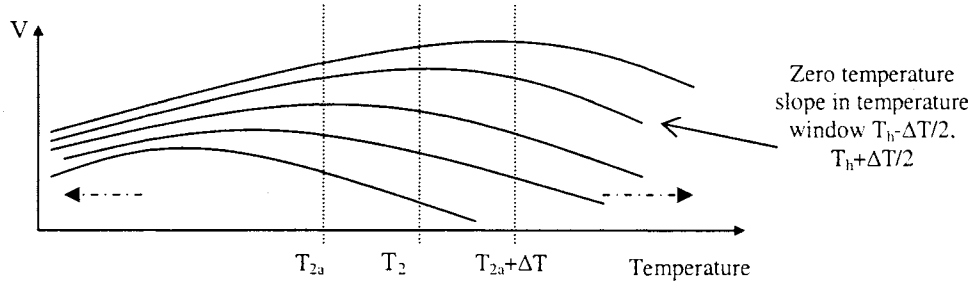


Figure 4.5 Calibration strategy that identifies R_3 that yields to an inflection point at T_h

The calibration strategy described above requires the ability of taking measurements at two temperatures, T_h and T_h+ΔT. If T_h is the ambient temperature, an on-chip heating mechanism can be used to generate temperature T_h+ΔT. This technique is described in the next section.

4.3 – On-chip Heater

Consider the bandgap voltage reference circuit depicted in Figure 4.3. The performance of this circuit is dependent upon the thermal environment of the Bipolar Junction Transistors (BJT) Q_1 and Q_2. Therefore, heating of the BJT pair has the effect of increasing the operating temperature of the reference circuit. This can be done by placing some high current resistors, or diodes, or BJTs as heaters in close proximity to Q_1 and Q_2. Similar work has been reported in [14] in which special processing was used to thermally isolate the reference circuit from the surrounding. In contrast to the earlier work, the strategy here is to change the temperature of Q_1 and Q_2 when they are part of a standard bulk CMOS process. Upon turning on the heaters, the heat dissipated by the heaters will heat up the temperature core of the reference circuit. When the power to the heaters is turned off, the circuit returns to ambient temperature. Several issues associated with using the "heaters" to increase the temperature deserve mention and all are critical to the practical use of the proposed technique. First, it is critical that the reference voltage for the ADC in the Digital Temperature Sensor not change when the temperature of the reference circuit is increased from T_1 to $T_1+\Delta T$ since this ADC is used to measure the slope of the reference circuit and to do the offset adjustment need to maintain continuity. This can be achieved if either the distance between the Digital Temperature Sensor (and including its own reference) and Q_1 and Q_2 of the temperature reference is sufficiently large that the heating of Q_1 and Q_2 will not adversely affect the operating temperature of the Digital Temperature Sensor (DTS). Alternatively, we could require that the measurement be made fast enough with the DTS so that the measurements are complete before any heating effects in Q_1 and Q_2 affect the temperature of the DTS. In what follows, it will be shown that sufficient physical separation

is readily obtainable on a die to provide the required thermal isolation. A second concern is the power dissipation associated with the heater. In what follows it will be shown that this also is not of concern since the time required to increase the temperature of Q_1 and Q_2 by ΔT is a few microseconds and since these heaters need only be turned on once for each trigger point throughout the life of the reference. A third concern is process complexity. As mentioned earlier, the proposed approach uses a standard bulk CMOS process and does not require any specialized processing steps. To investigate the lattice heating effects of semiconductors, two bulk CMOS BJTs were used as heaters and the thermal properties were simulated using a simulation tool called Silvaco-Atlas. The simulation script can be found in the appendices.

Two vertical NPN transistors on a bulk silicon wafer were modeled in the simulation. Their axis of symmetry were placed 20μm apart. Refer to Figure 4.6 for the cross-sectional diagram of the NPN transistors. The width of the emitter diffusions were 1.6μ. Two base contacts were made for each device, one to the left of the emitter region and one to the right. Both base contacts were 0.5μ wide. The collector contacts were 1μ wide. In Figure 4.6, the second base contact, the one to the left of the emitter, is designated as node Xxx. The one base contact was set at 1.8V and the other at 0V to create a large current flow in the base. This strategy was to use the base diffusion as the heater. This resulted in a large lateral gradient in the base-emitter and base-collector voltages and created some large lateral gradients in collector and emitter currents. There were some anomalies in the resultant collector and emitter currents obtained by the simulator but since we were interested primarily in thermal gradients in the silicon wafer, we did not resolve the anomalies in the electrical properties of the device model. The default thickness of the layer simulated (into

the paper in Figure 4.6) in Silvaco-Atlas is 1μ and that dimension was not changed. The heater was turned on by running up the voltage at the one base node to 1.8V while connecting the other base node (Xxx) to ground. The resultant port electrical variables (which show some anomalies) after the 1.8V is reached and after thermal equilibrium is established appear in Table 4.1. The power dissipation in equilibrium is around 14mW.

In the following simulations, the ambient temperature of the simulation environment was set to 300°K. A 1.8V step base voltage with 2μ sec linear ramp was applied to the base terminals of both BJT at time=0. In the simulator, this 2μ sec is termed the "step time". The structure reached thermal equilibrium at time=500μ sec. The thermal response of the structure at equilibrium is shown in Figure 4.7a. The region where the transistors reside is enlarged in Figure 4.7b.

Table 4.1 Operating points of the NPN transistors at equilibrium

Operating Points	BJT1	BJT2
Emitter voltage	0 V	0 V
Emitter current	-0.6mA	-0.51mA
Base voltage	1.8 V	1.8 V
Base current	8mA	6mA
Xxx voltage	0 V	0 V
Xxx current	-0.28mA	-0.29mA
Collector voltage	0.2 V	0.2 V
Collector current	-5.2mA	-7.1mA

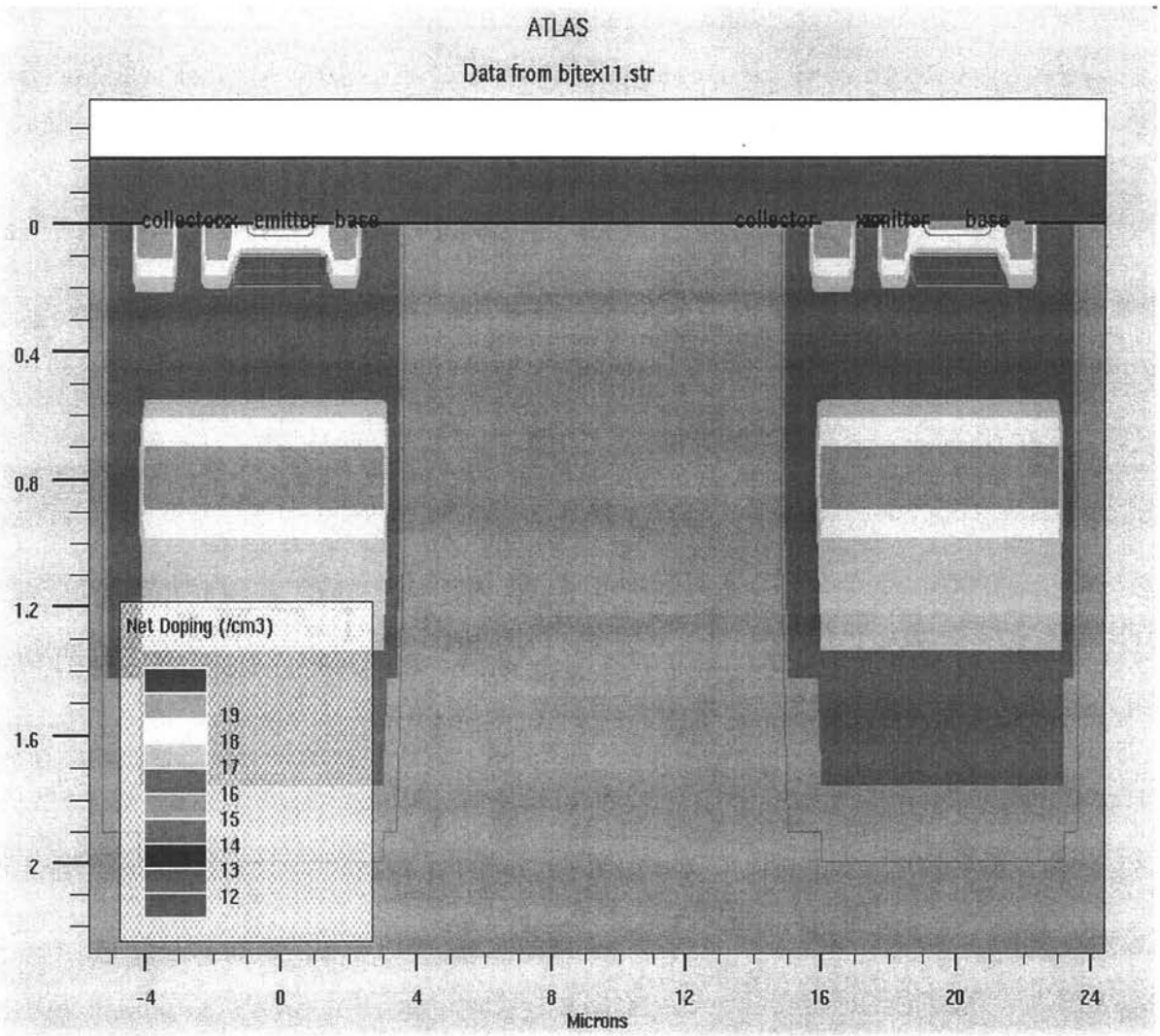


Figure 4.6 Cross-sectional diagram of two NPN transistors

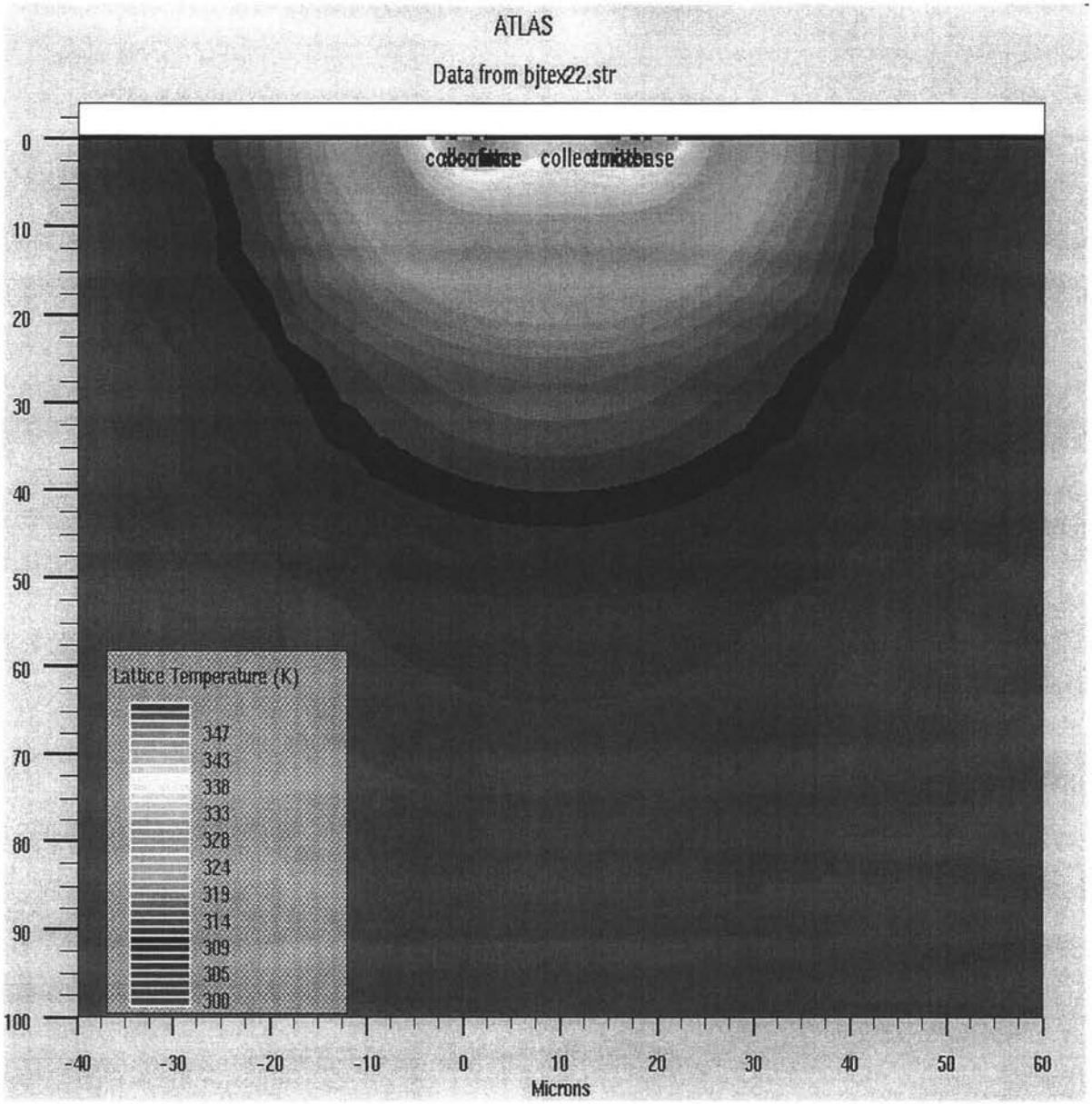


Figure 4.7a Thermal response of the NPN transistors at equilibrium

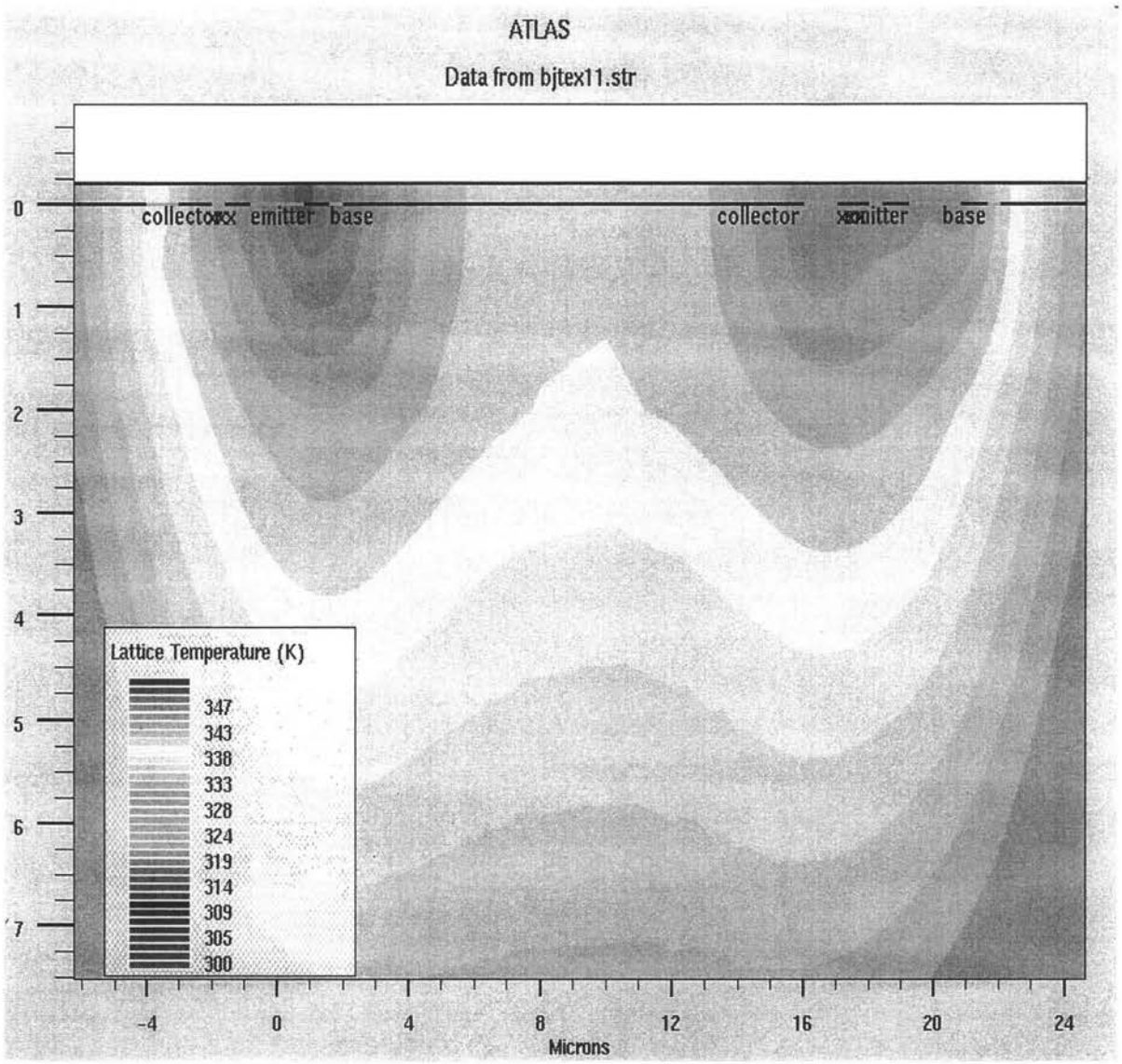


Figure 4.7b Thermal response of the NPN transistors with enlargement on the transistors region

It can be seen from Figure 4.7a and 4.7b that the temperature drops as the distance from the transistors increases. Therefore, if the NPN transistors are to be used as heaters to heat up the reference circuit, the temperature core of the reference circuit, which consists of the BJT pair, needs to be placed close to the heaters. Observe that the temperature at the region between the NPN transistors reaches 343°K at equilibrium, as depicted in Figure 4.7b. Thus it is reasonable to place the transistors Q_1 and Q_2 of the reference in between the NPN transistors used as heaters. Refer to Figure 4.8 for graphical illustration. The heating mechanism is quite localized and is effective for local heating. At distance 40μ away from the heaters, the rise in temperature is less than 5°C at equilibrium and, although not shown in the figure, it appears that at distance more than 60μ away, there will be no appreciable change in temperature. This is important because the reference in the DTS must not change when the heater is turned on.

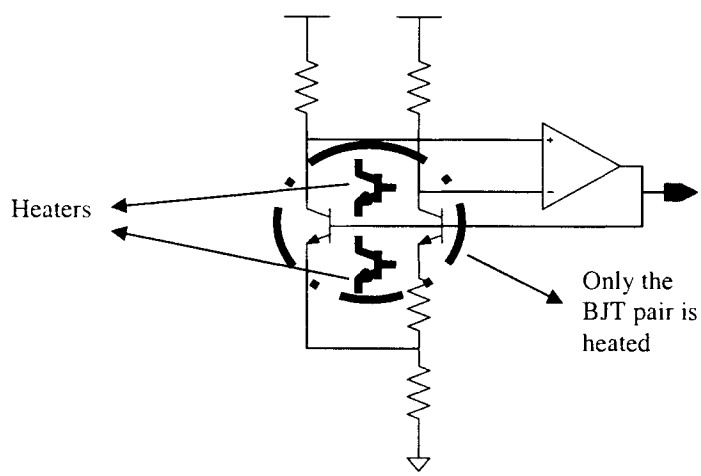


Figure 4.8 The temperature core of the reference circuit is placed closely to the heaters. Only the BJT pair is heated by the heaters.

The cool down process of the heaters was also simulated. For this simulation, the heater was initially on and in thermal equilibrium. The base voltage was then ramped down to 0 V starting at time=0 with a "step time" of 2μ sec. The thermal response of one the structures at times=2μ sec, 5μ sec and 20μ sec are depicted in Figure 4.9a, 4.9b and 4.9c respectively. The operating points of the NPN transistors at time=2μ sec are listed in Table 4.2. From Figure 4.9c it is apparent that the temperature of the heater drops rapidly once the heater is turned off and that after 20μ sec, the peak rise in temperature in the heater is only 2°C above ambient.

Table 4.2 Operating points of the NPN transistors at cooling down

Operating Points	Values
Emitter voltage	0 V
Emitter current	2.3nA
Base voltage	0 V
Base current	9.6nA
Xxx voltage	0 V
Xxx current	-13nA
Collector voltage	0.2 V
Collector current	1nA

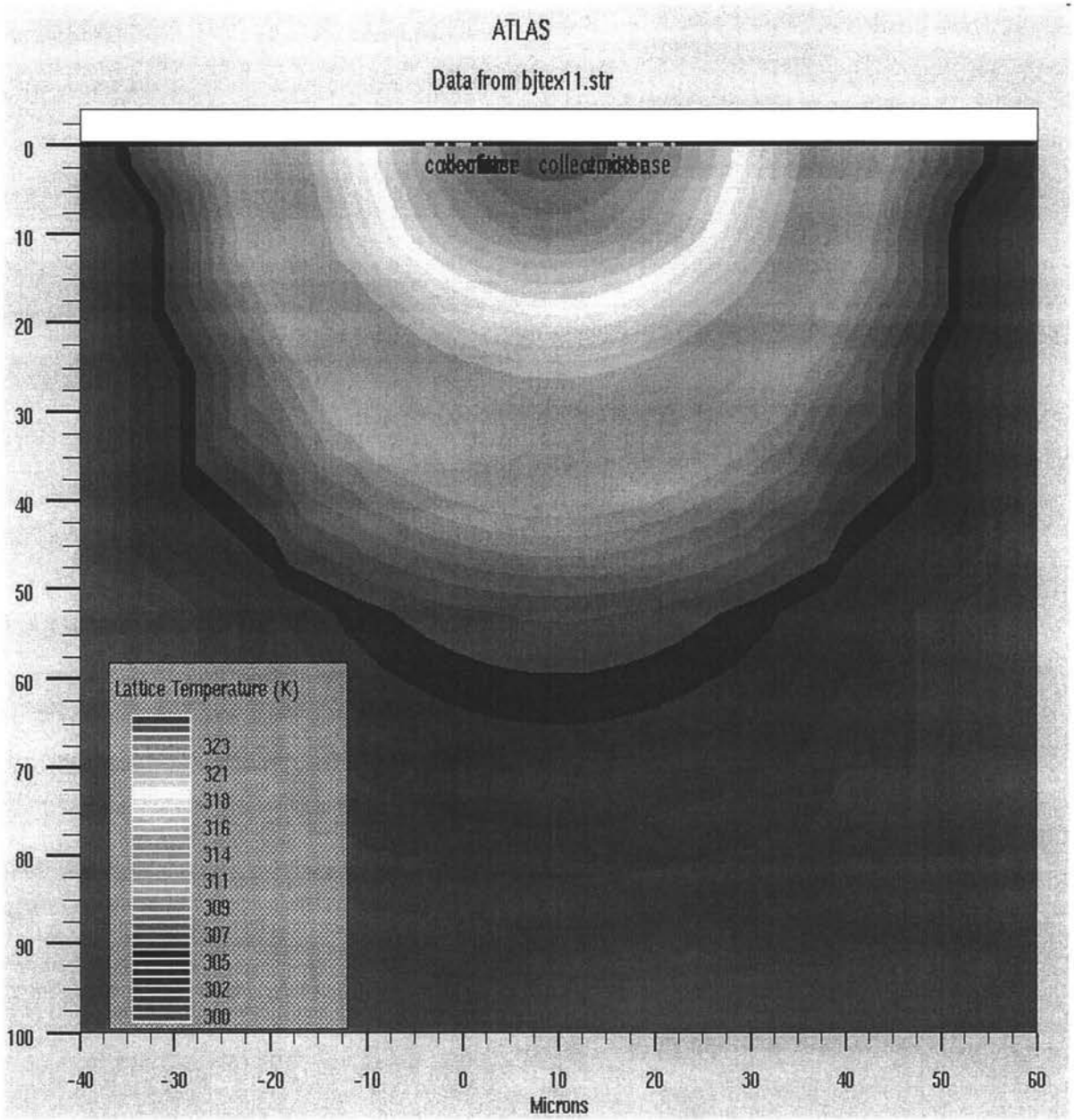


Figure 4.9a Thermal response of the NPN transistors at cooling down, time=2μ sec

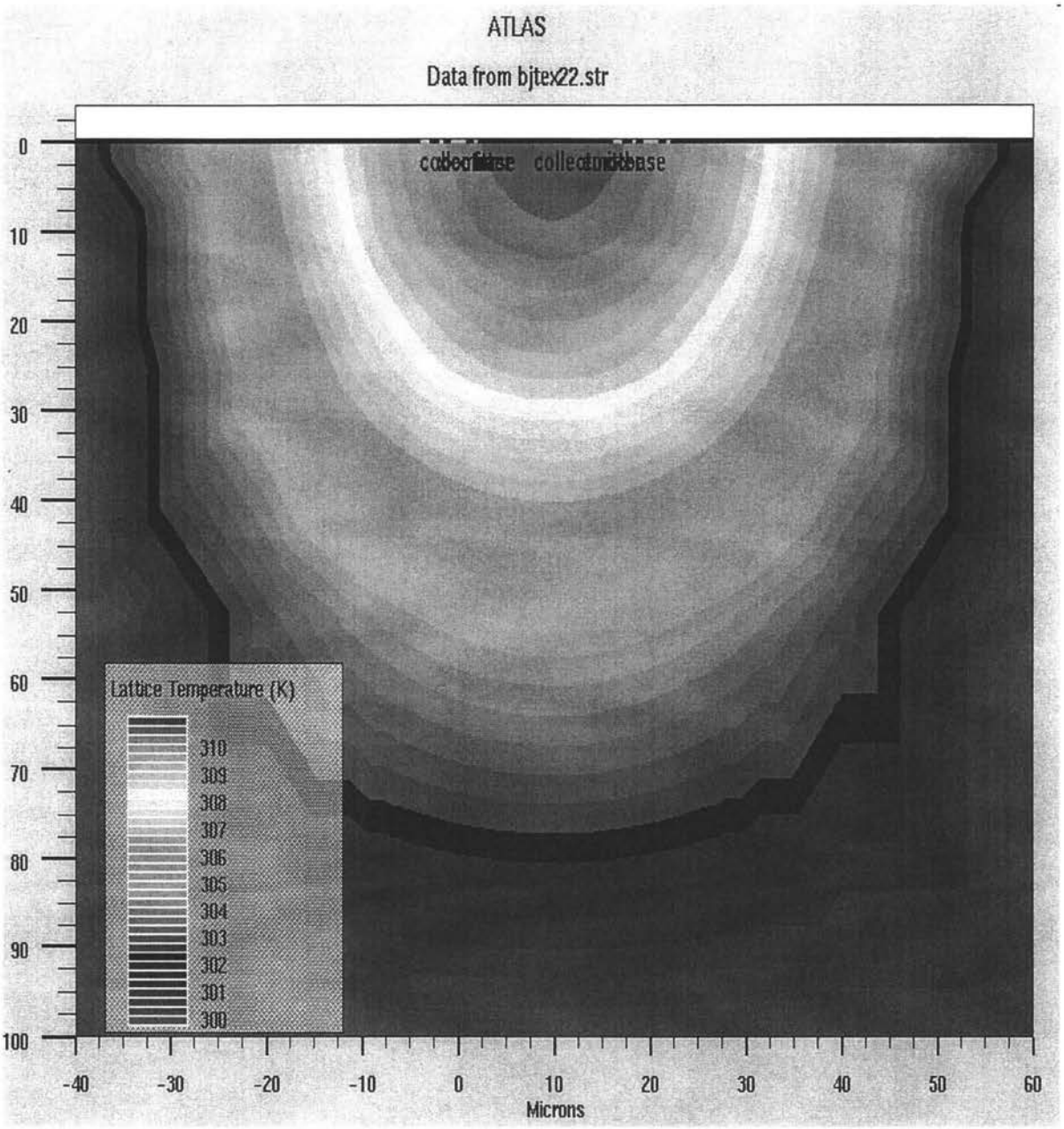


Figure 4.9b Thermal response of the NPN transistors at cooling down, time=5μ sec

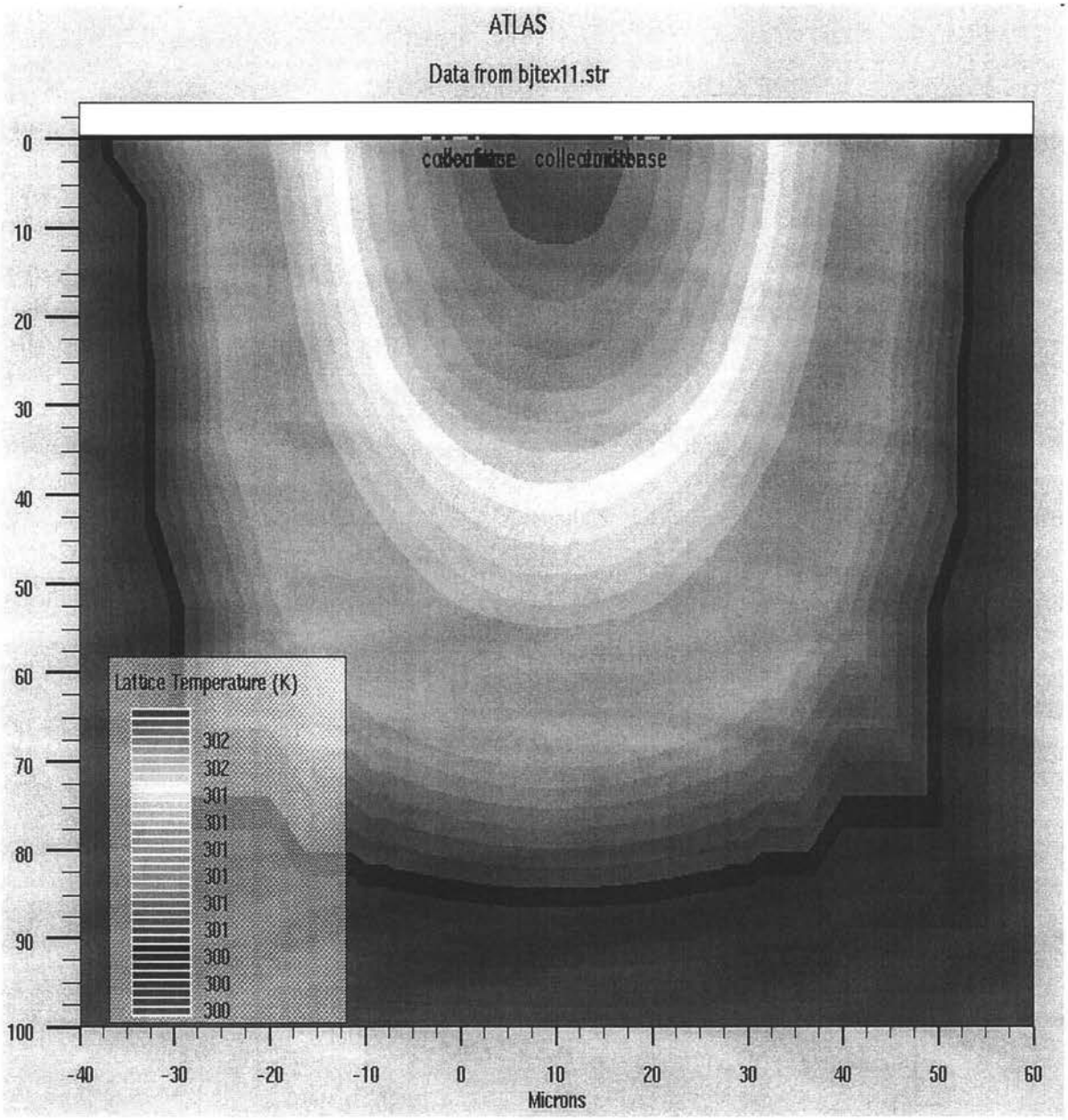


Figure 4.9c Thermal response of the NPN transistors at cooling down, time=20μ sec

In summary, it can be observed that a localized heater can be used to increase the temperature very rapidly with thermal equilibrium being established in 500μ sec but with near equilibrium being reached much faster. The effects of a localized heater on circuits 50μ away from the heater are negligible. Thermal equilibrium is re-established very quickly as well during the cool-down process with less than 3°C residual rise after 20μ sec. In this example, a 40°C temperature raise was obtained in the heater. The actual temperature raise needed for a two inflection point reference circuit would likely be in the 10°C range so either a reduction in heater power or a wider separation of the heater elements would be appropriate. If 4 inflection points were used in the reference, even a lower temperature rise would likely be preferred. It is believed that the position and geometries of the heaters can easily be modified to provide any desired temperature rise in transistors Q_1 and Q_2 of the reference.

4.4 – Self-Calibration Algorithm

The self-calibration algorithm will be reviewed in this section. The algorithm is designed with the capability of heating up the temperature core of the reference circuit without affecting the temperature of other circuitries. The definition of temperature core can be found in the previous discussion. When the calibration routine is invoked, the system will position the inflection point in the middle of the temperature window T_2-T_1, where T_1 is the ambient temperature, and T_2 is a temperature that is higher than ambient temperature. The geometry and power dissipation of the heater can be engineered to create any desired temperature increase. The definition of T_1 and T_2 can be found in the previous discussion.

The calibration routine starts with the first set of measurements described in the calibration strategy. The measurements are done by performing a series of analog-to-digital conversions with the ADC in the Digital Temperature Sensor (DTS) on the output voltage of the temperature sensor at T_1 (T_1=ambient temperature) for all R_{3k} configurations. Refer to Figure 4.3 for the definition of R_{3k}. The conversion results are then saved in the memory for future references. Next, the on-chip heaters are turned on to heat up the reference circuit. It is important to keep the reference in the DTS far enough away from the heaters so that it is not affected when the heaters are turned on. When the temperature of the reference circuit reaches equilibrium at T_2, the second set of measurements described in the calibration strategy is performed to predict the temperature slope in the temperature window T_2-T_1. The procedure can be terminated when the system detects a zero temperature slope or a transition of the temperature slope from positive to negative. The corresponding R_{3k} configuration is saved in the memory. A simplified summary of the calibration algorithm appears in the flow chart of Figure 4.6.

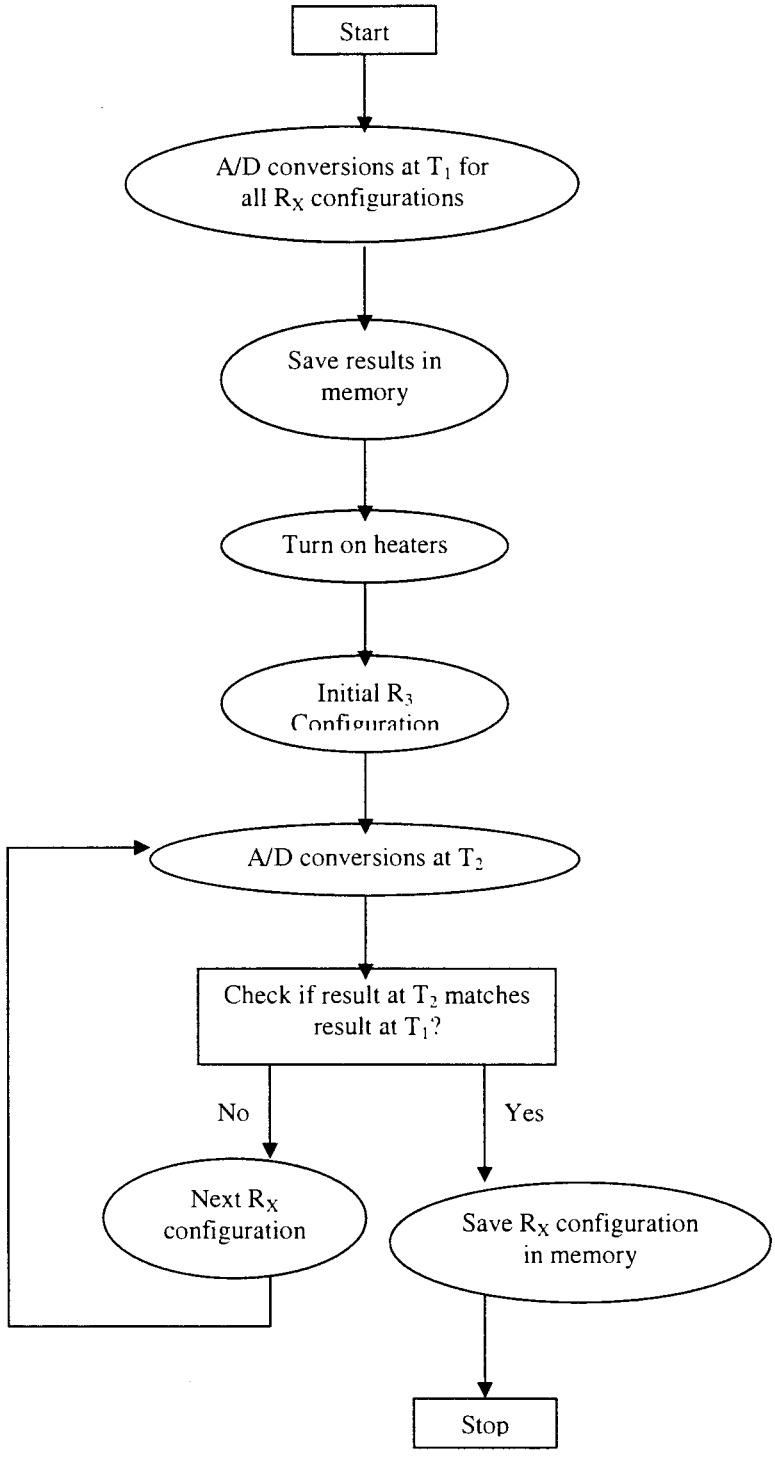


Figure 4.6 Flow graph of the self-calibration algorithm

5. IMPLEMENTATION AND SIMULATION RESULTS

A voltage reference system was implemented using the multiple inflection points approach and the self-calibration scheme for correcting inflection point error. The self-calibration scheme had been simplified in this implementation to compromise between the algorithmic complexity and accuracy with the intent of facilitating the process of simulations and verification. There are two adaptations made to simplify the algorithm. The first adaptation is to predetermine the first time power up at room temperature. The second adaptation is the measurement of the inflection point only at T_{init} on power up. The inflection points at other temperatures, instead of being measured, are estimated based on resistor matching. Therefore, the precision of the inflection point temperatures rests on the resistor matching accuracy of the technology and typical semiconductor technology can readily achieve resistor matching accuracy of 1% or better. From the data depicted in Figure 2.3.1, 1% matching error between R_1 and R_2 results in a shift of 60°K on the inflection point temperature, or 2× increase in the reference voltage error. The compromise is justifiable because it totally eliminates the alternate trigger temperatures set mentioned in the previous chapter by taking the inflection point measurement only at power up given the error of the reference voltage near inflection point is very small to start with.

The implementation was designed to operate from –40°C to 100°C with the inflection point temperatures set being {-20°C, 30°C, 75°C}. T_{init} was predetermined to be 20°C and the trigger temperatures set is {0°C, 40°C}. The implementation was simulated and verified using Spectre. The bandgap voltage reference circuit and the temperature sensor were realized in an AMI1.5m process. The digitally controlled level shifter, the control and

arithmetic unit, and the calibration unit were implemented behaviorally with AHDL (Analog Hardware Description Language). The AHDL scripts for all the behavioral building blocks in this implementation can be found in the appendices. The schematic diagram for the overall system is depicted in Figure 5.1.

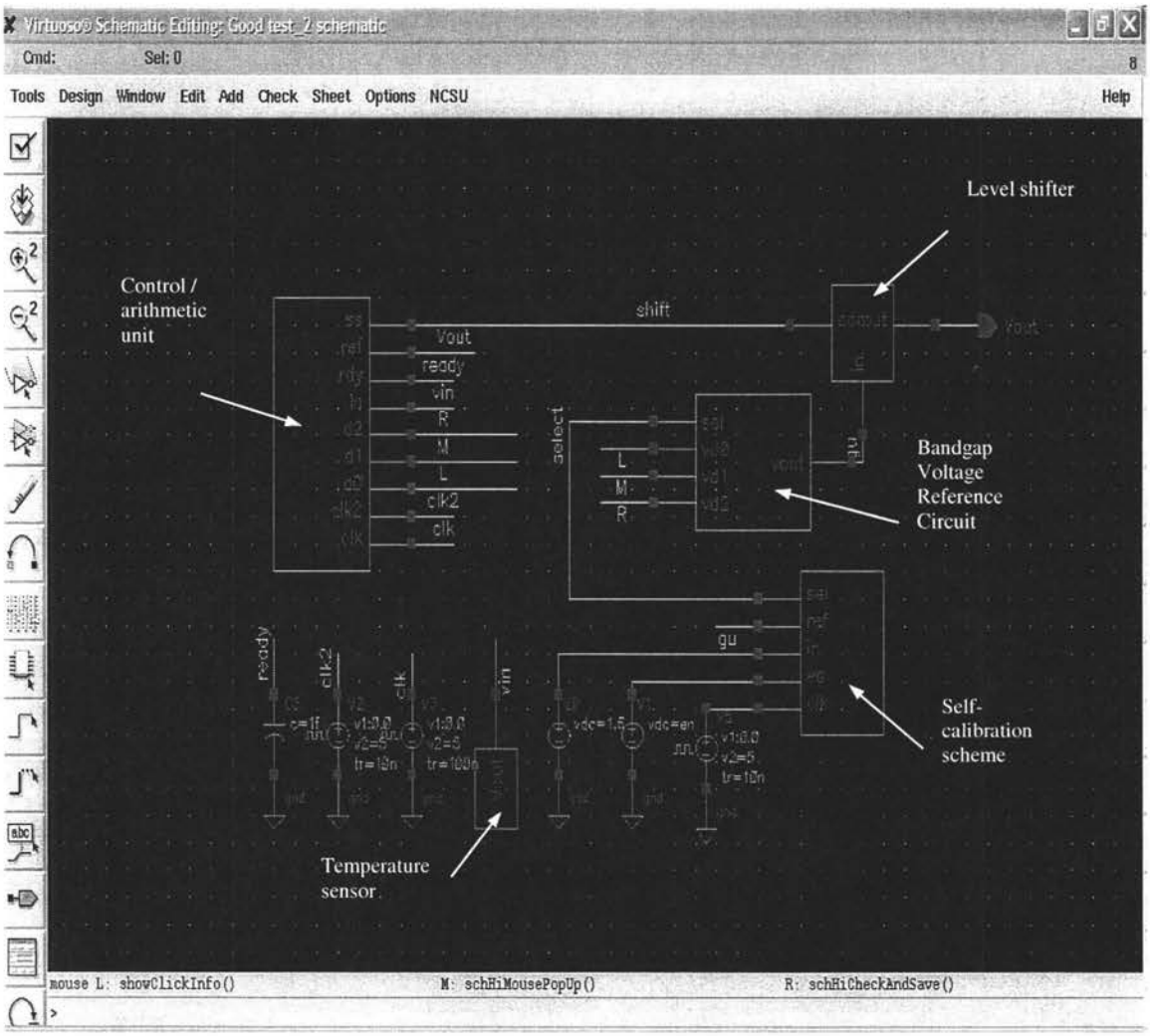


Figure 5.1 Schematic diagram of the overall system

5.1 – Multiple Inflection Points Bandgap Voltage Reference Circuit

The schematic diagram of the bandgap voltage reference circuit is shown in Figure 5.2. It was designed using the multiple inflection points approach with generalization of the circuits of Figure 4.2.1 in which the R_3 trim network was used for fine adjust and the R_1 trim network was used for coarse adjust of the inflection points. The coarse adjust circuit was not trimmed and all trimming was accomplished with the 4-bit control of the R_3 network. A switch that is always "on" was placed in series with the R_4 resistor in an attempt to obtain partial process compensation between the R_4 resistor and the R_3 resistors which inherently include a series switch impedance.

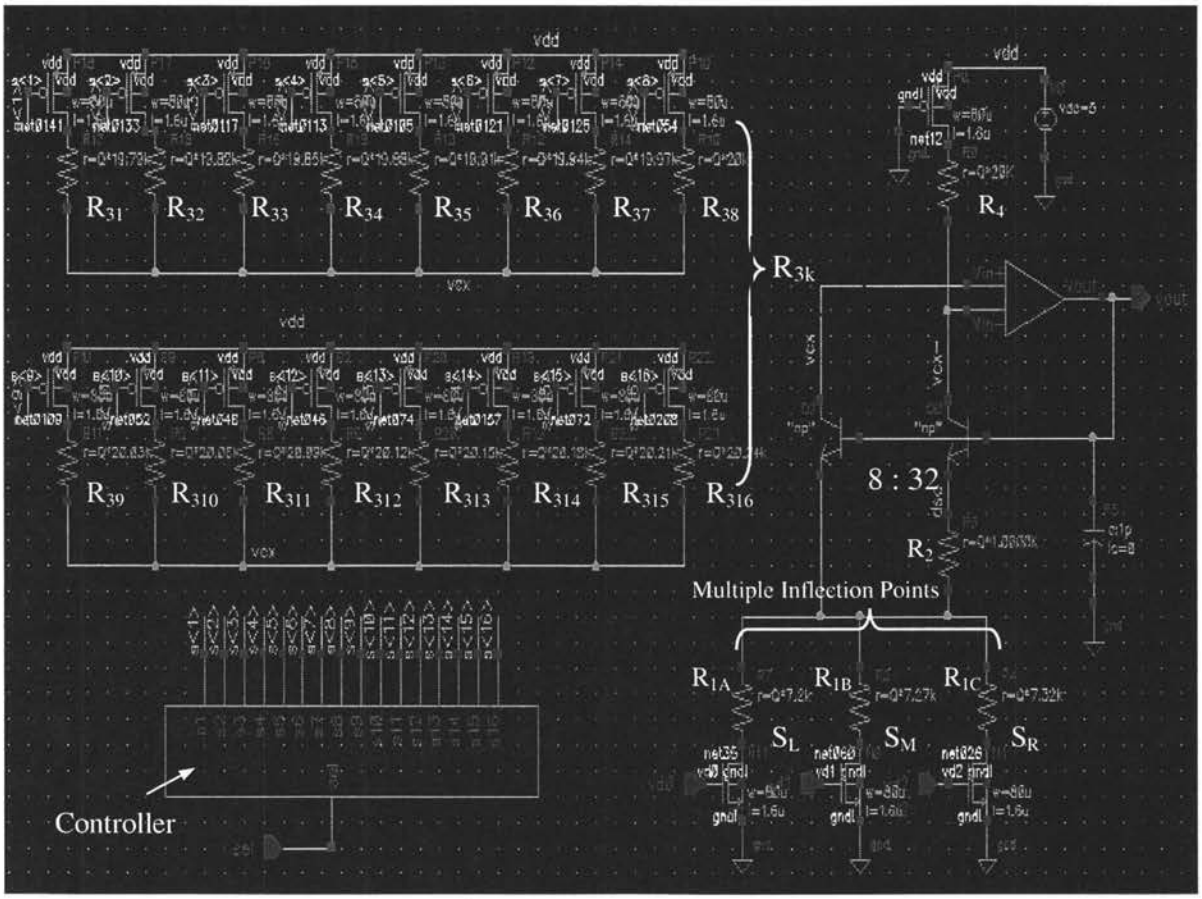


Figure 5.2 Schematic diagram of the bandgap voltage reference circuit

The components value of the circuit in Figure 5.2 can be found in Table 5.1. The simulated temperature response of the reference circuit that corresponds to S_L, S_M or S_R closed is depicted in Figure 5.3. In these simulations, the BJTs were modeled as part of the AMI process. The temperature response of the reference circuit for S_M closed and R_{3k} taking the values of R_{35} ... R_{38} is depicted in Figure 5.4. The inflection point moves from 40°C to 10°C with 10°C decrements when the R_3 configuration changes from R_{35} to R_{38}.

Component	Value	Component	Value
R_{1A}	7.2k	R_{38}	20k
R_{1B}	7.27k	R_{39}	20.03k
R_{1C}	7.32k	R_{310}	20.06k
R_2	1k	R_{311}	20.09k
R_{31}	19.79k	R_{312}	20.12k
R_{32}	19.82k	R_{313}	20.15k
R_{33}	19.85k	R_{314}	20.18k
R_{34}	19.88k	R_{315}	20.21k
R_{35}	19.91k	R_{316}	20.24k
R_{36}	19.94k	R_4	20k
R_{37}	19.97k		

Table 5.1 Components value in circuit of Figure 5.2

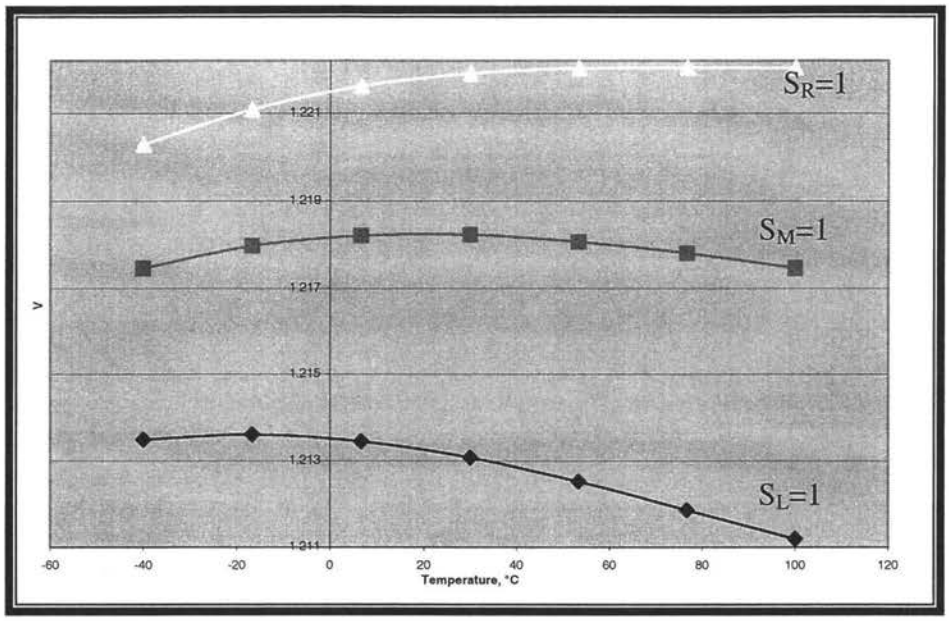


Figure 5.3 Temperature response of the reference circuit with multiple inflection points

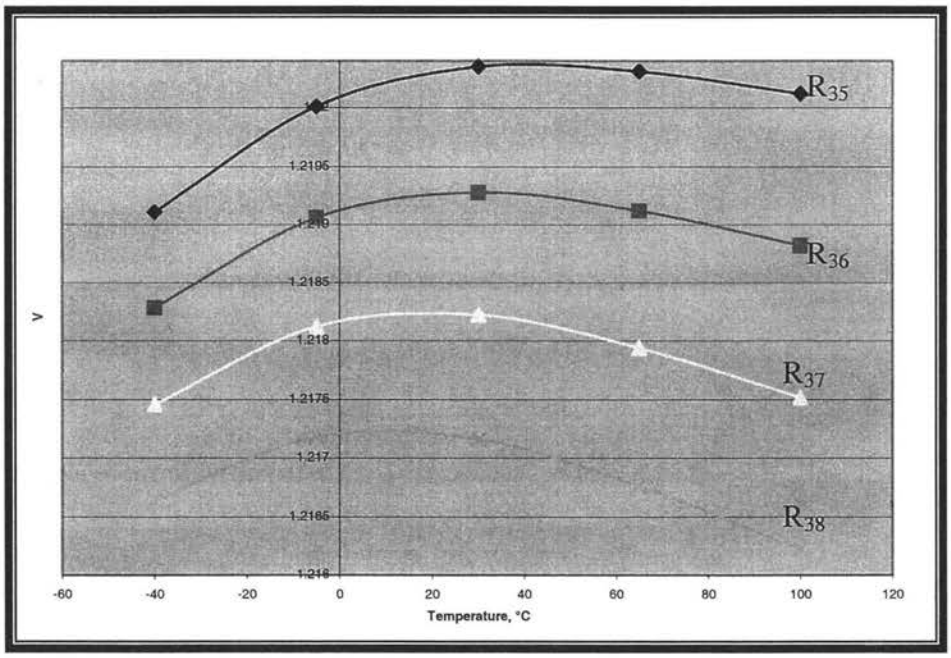


Figure 5.4 Temperature response of the reference circuit with different R_3 values

5.2 – Temperature Sensor

The schematic diagram of the temperature sensor is depicted in Figure 5.5. The circuit is derived from the PTAT current generator [2]. A resistor is used to convert the current signal into voltage. The temperature response of the circuit is depicted in Figure 5.6. This circuit will be used in the Digital Temperature Sensor for temperature to digital conversion.

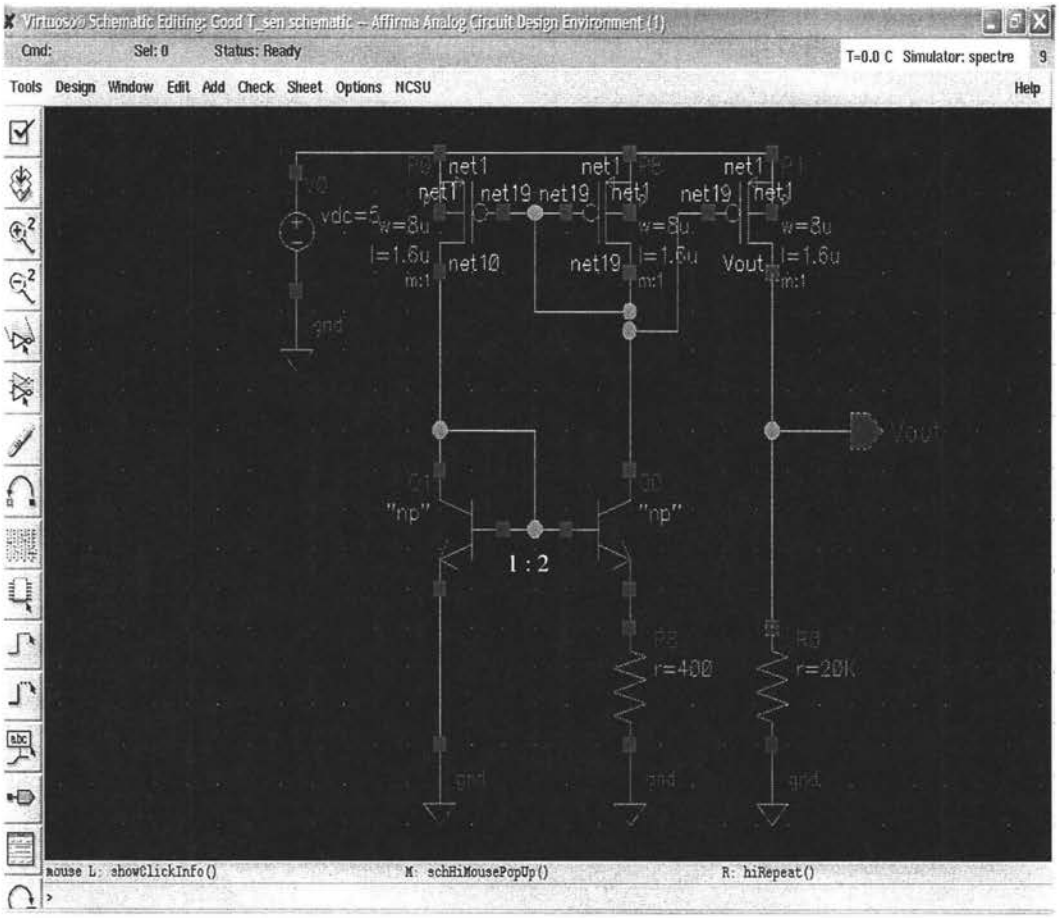


Figure 5.5 Schematic diagram of the temperature sensor

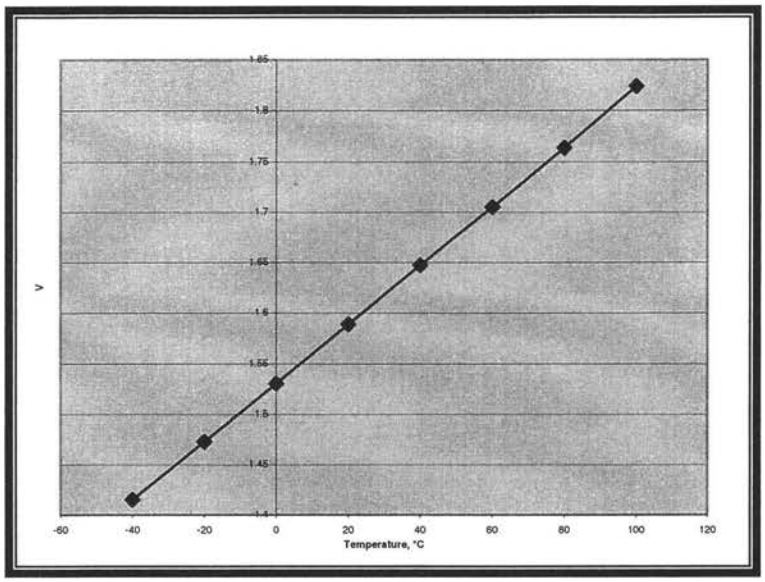


Figure 5.6 Temperature response of temperature sensor

5.3 – Control of Multiple Inflection Point Circuit

A control circuit is needed to control the switching between the three segments and a tuning algorithm is needed to establish continuity at the transition points. The circuit of Figure 5.2 was designed for nominal inflection points at -20°C, 30°C and 75°C and transition points at 0°C and 40°C. The control and arithmetic unit needed to monitor the bandgap circuit depicted in Figure 5.2 was modeled with AHDL. The ADHL scripts can be found in the appendices. The functions of the control unit include the selection of the proper R_1 to configure V_{PTAT} according to the temperature drift and the removal of discontinuity at the transition between two temperature curves. Detailed discussion on the control algorithm for multiple inflection points reference circuits can be found in Chapter 3.

The voltage reference system was simulated with the first time turn on at room temperature of T=20°C. In this implementation the self-calibration scheme was designed to work at room temperature and it was assumed that the self-calibration scheme would be applied upon power up. In a practical implementation, the control algorithm would need to accommodate initial turn on at any temperature in the specified operating range of the device. The transient response of the reference output voltage and other control signals for the simulation at T=20°C are depicted in Figure 5.7a, 5.7b and 5.7c. The frequency of the "clk" signal determines how frequently the system samples the temperature and possibly updates the reference voltage. At turn on, an initial level shift was selected and the inflection point measurement was made to determine an inflection point at T=30°C. The resulting temperature curve is called T_2 curve. The reference will follow the T_2 curve as long as the temperature does not cross any trigger temperatures in either direction.

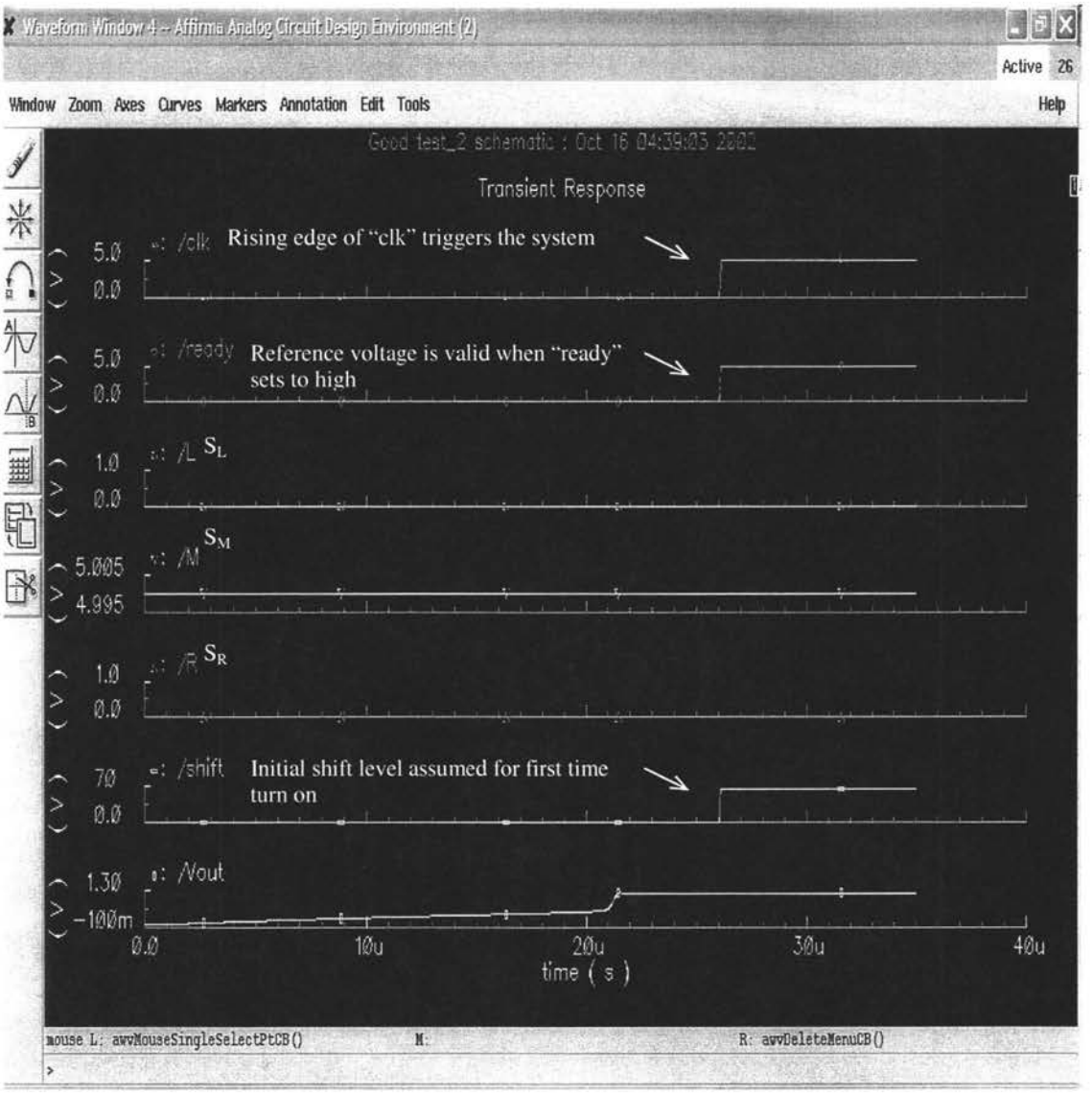


Figure 5.7a Transient response of the reference output voltage and other control signals at T=20°C

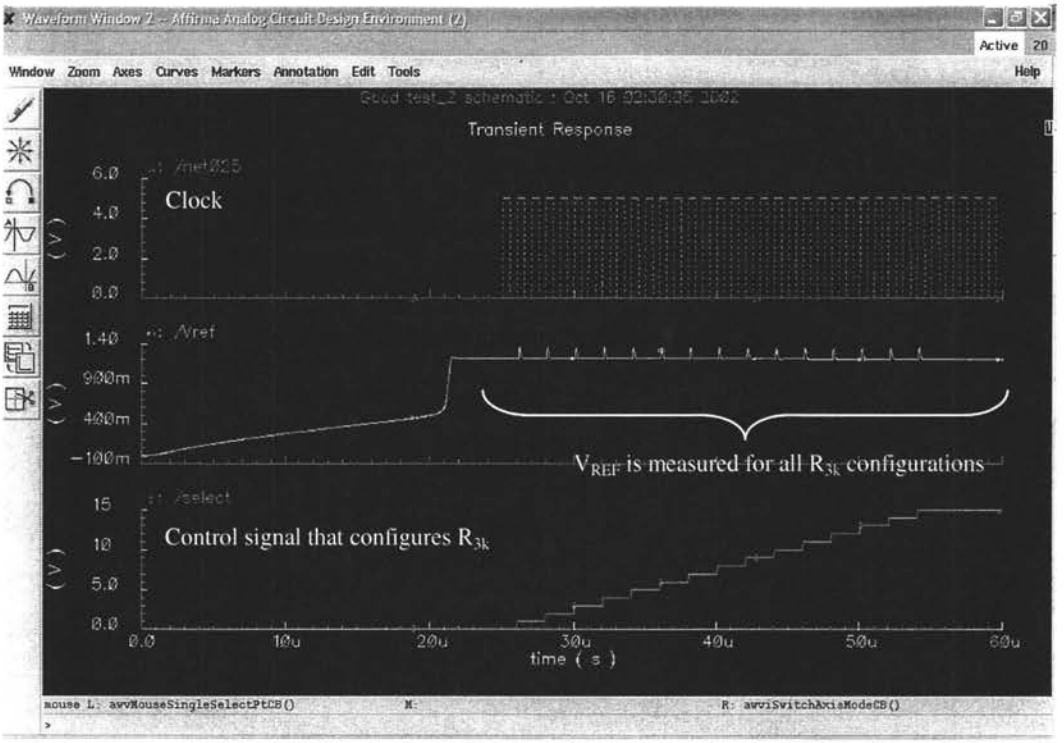


Figure 5.7b Applying calibration scheme at temperature T_{init}=20°C

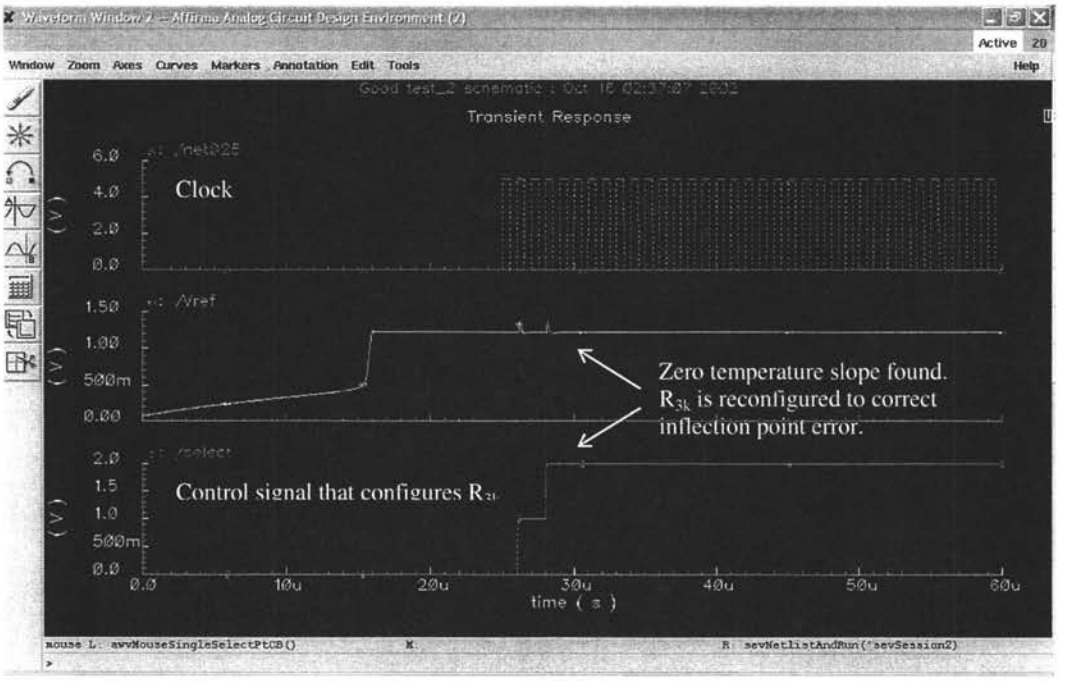


Figure 5.7c Calibration continues at T_{init}+20°C

Assume dropping temperature, another simulation was performed at T=10°C. The result is depicted in Figure 5.8. The R_1 setting remained unchanged because no trigger temperature was crossed.

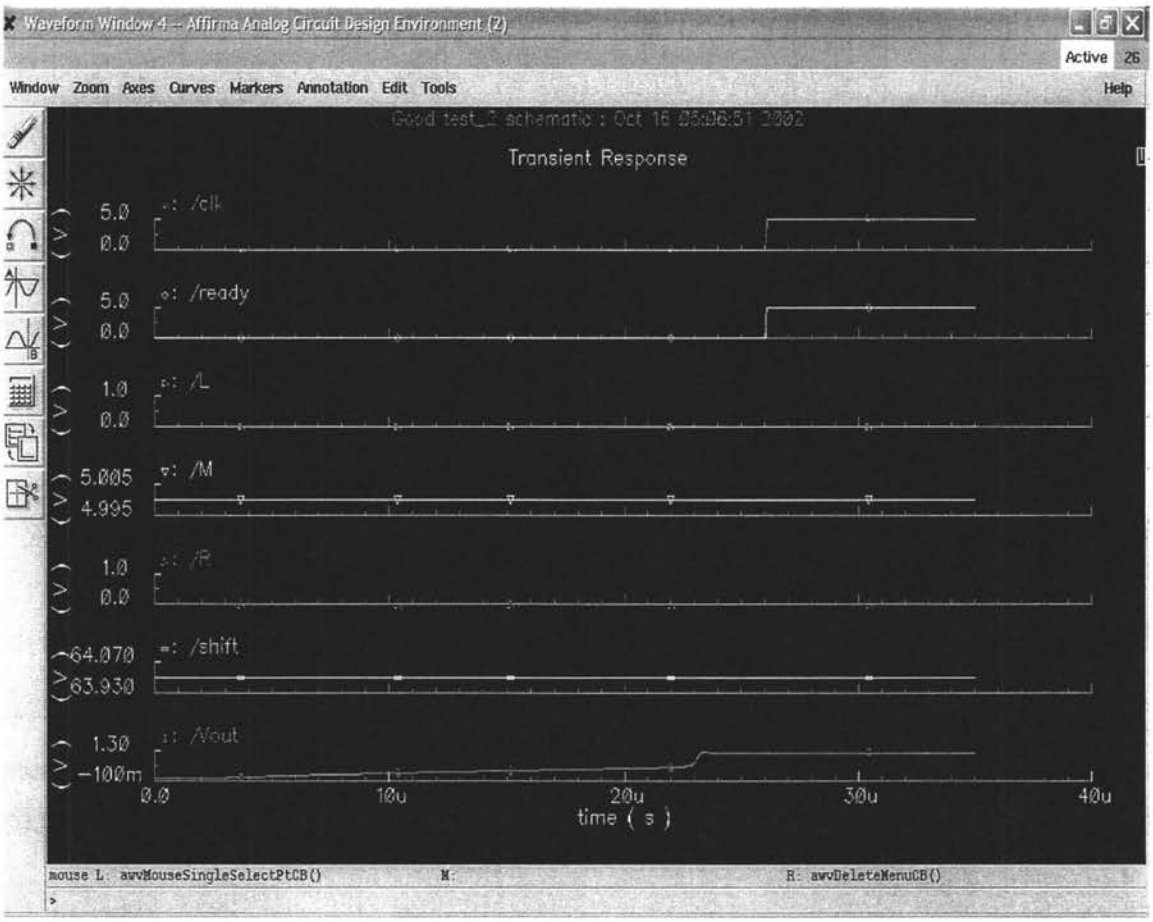


Figure 5.8 Transient response of the reference output voltage and other control signals at T=10°C

The temperature continued to decrease until it reached the trigger temperature T=-1°C. A transition would be made on the reference from the T_2 curve to a new temperature curve with an inflection point at T=-20°C, call it the T_1 curve. The offset at the transition was

removed at the crossing of T=-1°C. The transient response of the simulation is depicted in Figure 5.9. The digital code that removed the offset was stored in memory.

The reference was simulated at T=41°C. At this temperature, the reference would switch from the T_2 curve to a new temperature curve that nominally has an inflection point at T=75°C, call it theT_3 curve. The offset of the transition was removed and the corresponding digital code was stored in memory. The simulation result is depicted in Figure 5.10. Again, the new shift level was saved in the memory and it will be used to associate with all outputs where S_R=1. By now, the voltage reference system has gathered all necessary information for removing the discontinuity at the transition points, and the system is capable of providing a highly accurate reference voltage across the entire temperature range, which is from -40°C to 100°C.

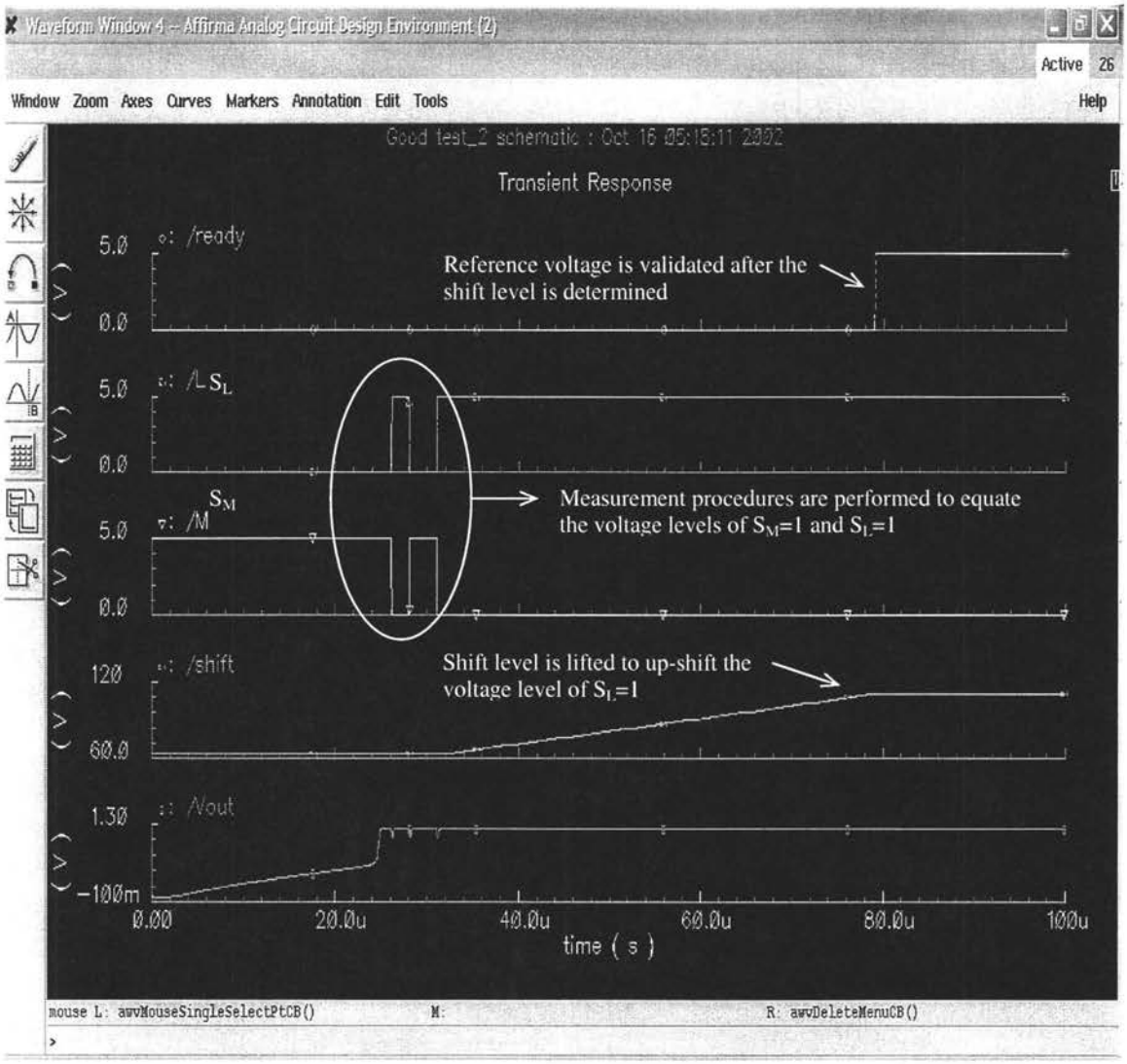


Figure 5.9 Transient response of the reference output voltage and other control signals at T=-1°C

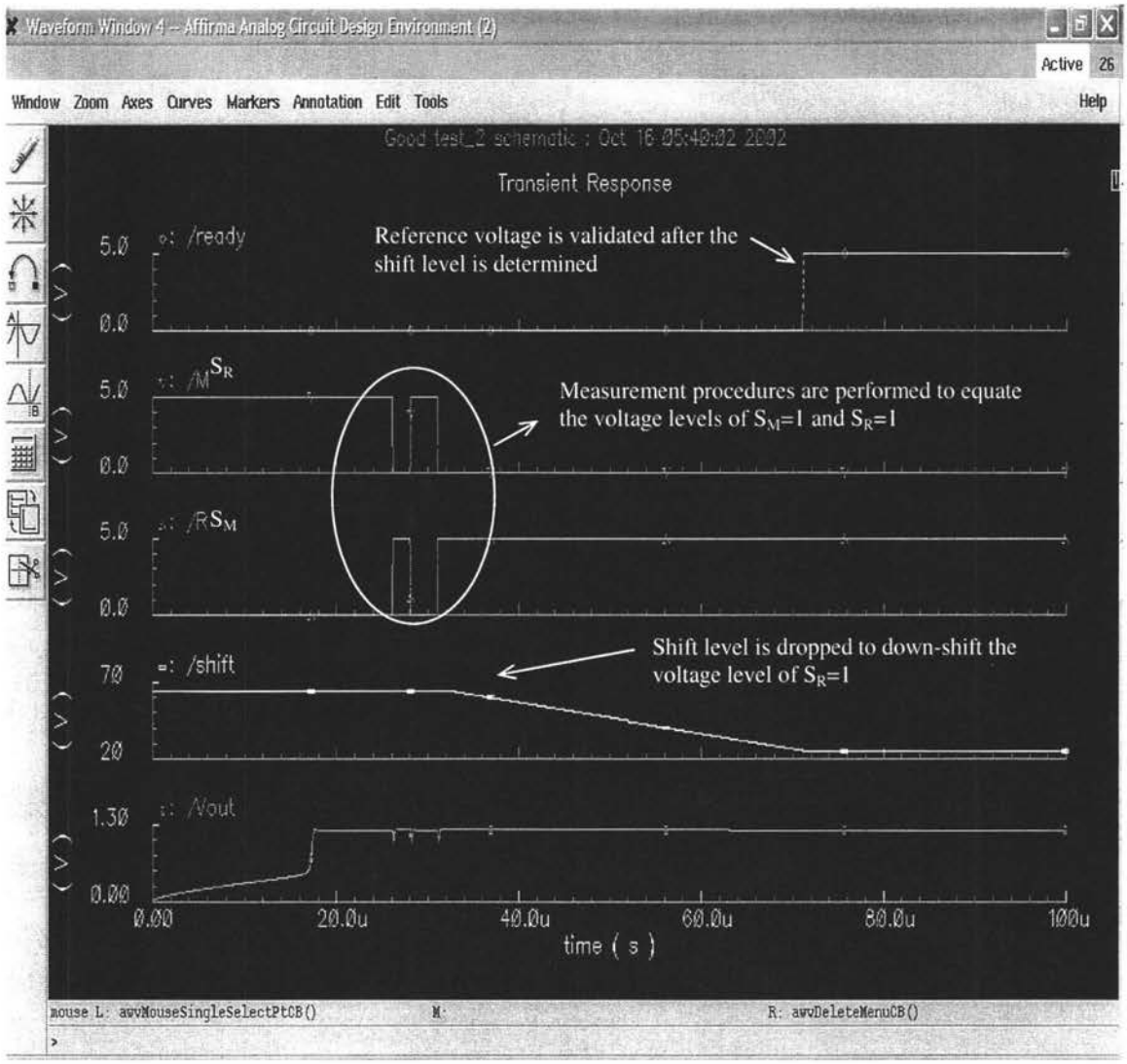


Figure 5.10 Transient response of the reference output voltage and other control signals at T=41°C

The overall temperature response of the reference voltage after being environ-stabilized is depicted in Figure 5.11a. The total error voltage is 230μV and this is equivalent to a temperature coefficient of 1.36 ppm/°C. The nominal overall temperature response of the reference voltage is depicted in Figure 5.11b. The nominal error voltage is less than 180μV. This is equivalent to a temperature coefficient of 1.06ppm/°C.

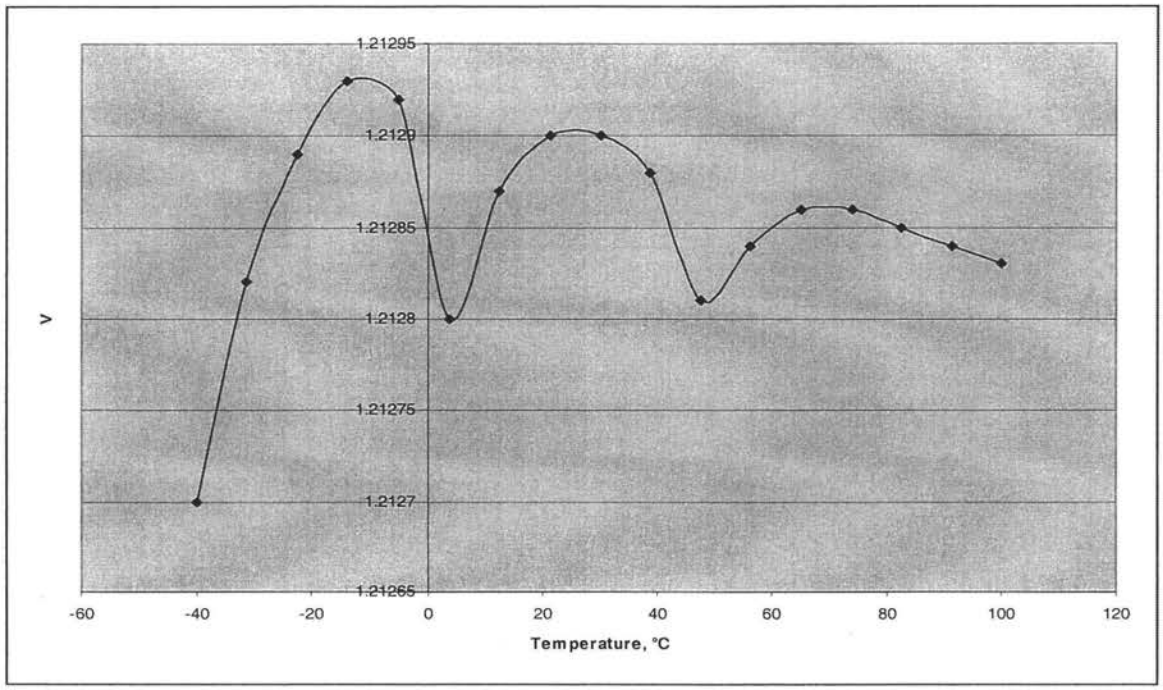


Figure 5.11a Temperature response of the multiple inflection points voltage reference system

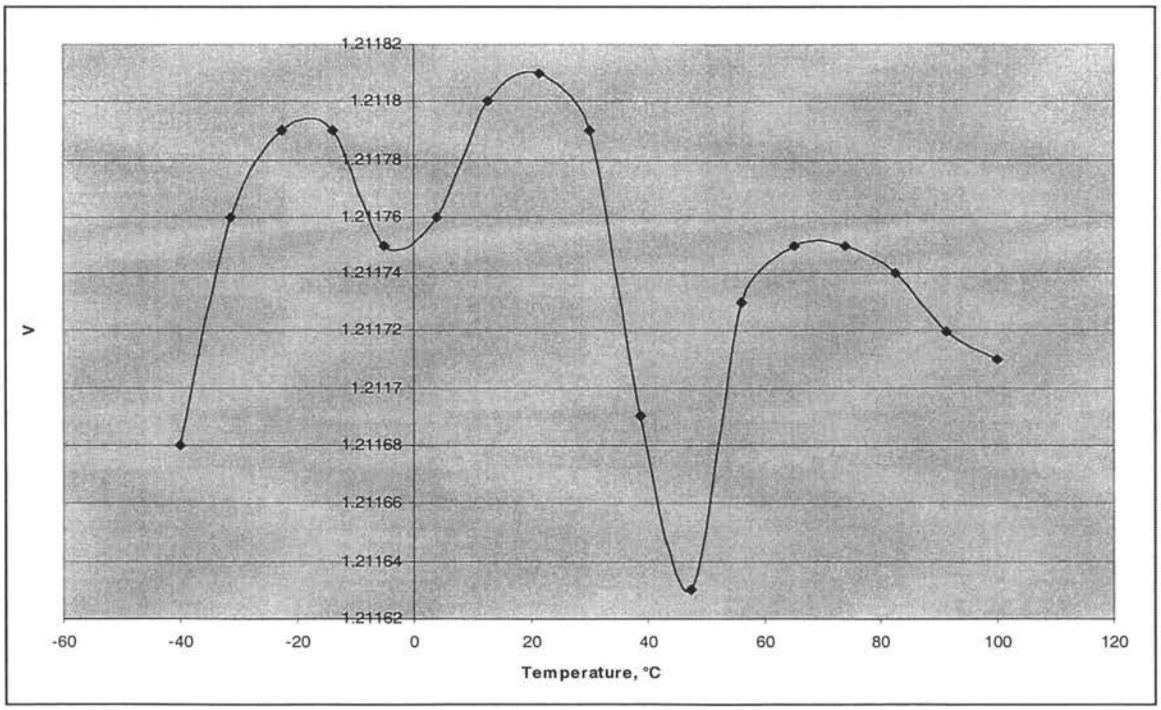


Figure 5.11b Nominal temperature response of the multiple inflection points voltage reference system

Recall from the discussion at the beginning of Chapter 5 that the performance of this implementation had been compromised for simplicity and simulation efficiency. Therefore, the performance of the reference voltage could deteriorate by a factor of two if there is a 1% resistor matching error.

6. DISCUSSION

The calibration scheme described in this work relies on on-chip heating to create a temperature window which enables the measurements on the reference voltage at different temperature points. Mathematically, these two temperature measurements provide information about the sign of the deviation of the reference voltage with respect to temperature. However, this approach can only approximately position the inflection point in the temperature window created by the calibration scheme. A minor modification on the calibration scheme would allow a precise correction on the inflection point and this variant is similar to what was actually used in the initial calibration at temperature T_{init} discussed in Chapter 4. The concept of the modified version of the calibration scheme is only discussed theoretically.

The on-chip heating mechanism is first modified with a two-step heating capability which will allow the heating mechanism to heat up the circuit to two different temperatures. The circuit is first heated to the intermediate temperature and the temperature slope from ambient temperature to the intermediate temperature is measured. Then, the circuit is heated to a higher temperature. The temperature slope from the intermediate temperature to the higher temperature is also measured. If the temperature slopes changes sign from up-slope to down-slope, then it is inferred that there is an inflection point near intermediate temperature. Refer to Figure 6.1 for an illustration of the modified calibration scheme. This two-step heating approach mathematically provides for estimates of the sign of both first and second derivatives of the reference with respect to temperature.

The algorithms discussed to this point are dependent only upon estimating the sign of the first and second derivatives. Considerable information about accurately locating the inflection points is carried in the magnitude of the derivatives as well. Although no attempt has been made in this thesis to include magnitude information, it is believed that the algorithms described in this thesis can be improved if relative magnitude information is also used.

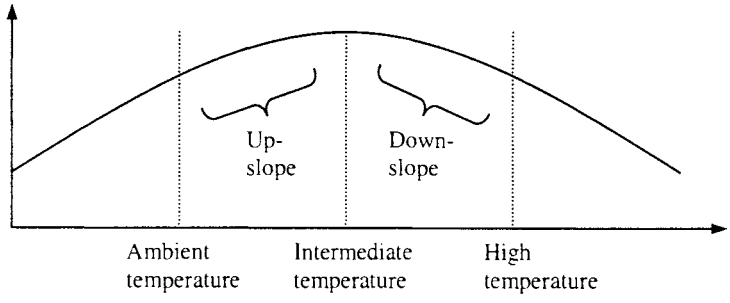


Figure 6.1 Modified calibration scheme with two-step heating

7. CONCLUSION

A new design approach for high performance voltage references has been introduced. This approach uses an environmental change to trigger an in-field self calibration that provides overall performance that is highly insensitive to process variations and to environment. These references are termed "environ-stabilized" references. The self-calibration capability makes it possible to practically place multiple inflection points throughout the desired operating range of the device thereby achieving extremely low temperature coefficients for the voltage reference.

In contrast to essentially all existing approaches to medium performance and high performance references which require specialized processes and expensive trimming operations in a temperature variable test environment, the proposed approach is compatible with standard low-cost bulk CMOS processes and all calibration is done on-chip with no need for either external test equipment or thermal cycling. Also, in contrast to most high performance voltage references which require accurate higher-order thermal models for all devices in the reference, the proposed approach does not need accurate thermal models of any devices.

Unique to this work is the use of a local on-chip heater to establish thermal changes during calibration. This local heater makes it possible to center inflection points at any ambient temperature without the use of external test equipment. The area overhead for this heater is small and since inflection point information is stored in memory after self-calibration, the power overhead required for the heater is negligible.

Simulation results for a prototype reference with three inflection points designed to operate over a temperature range from -40°C to +100°C show a total variation in reference voltage of less than 180μV which corresponds to an equivalent temperature coefficient of 1.06ppm/°C. This performance exceeds that of the best commercial parts available and it can be further improved by using additional inflection points.

APPENDIX A. INPUT SCRIPT FOR SIMULATING NPN TRANSISTORS IN SILVACO-ATLAS

```
go atlas

mesh
x.m l=-40 spacing=20
x.m l=-5 spacing=0.2
x.m l=0 spacing=0.2
x.m l=5 spacing=0.2
x.m l=10   spacing=2
x.m l=15 spacing=0.2
x.m l=20 spacing=0.2
x.m l=25 spacing=0.2
x.m l=60 spacing=20

y.m l=-0.2  spacing=0.05
y.m l=0.0  spacing=0.01
y.m l=0.04 spacing=0.01
y.m l=0.06 spacing=0.01
y.m l=0.15 spacing=0.05
y.m l=0.30 spacing=0.05
y.m l=1.0  spacing=0.15
y.m l=2  spacing=10
y.m l=10  spacing=20
y.m l=100  spacing=50

region num=1 y.max=0 oxide
region num=2 y.min=0 silicon

electrode name=emitter x.min=-0.8 x.max=0.8 y.min=0 y.max=0
electrode name=base  x.min=1.5 x.max=2 y.min=0 y.max=0
electrode name=xxx  x.min=-2 x.max=-1.5 y.min=0 y.max=0
electrode name=collector x.min=-4 x.max=-3 y.min=0 y.max=0

electrode name=emitter x.min=19.2 x.max=20.8 y.min=0 y.max=0
electrode name=base  x.min=21.5 x.max=22 y.min=0 y.max=0
electrode name=xxx  x.min=18 x.max=18.5 y.min=0 y.max=0
electrode name=collector x.min=16 x.max=17 y.min=0 y.max=0

#bulk
doping reg=2 uniform p.type conc=2e15

#collector L
doping reg=2 uniform n.type conc=2e16 x.right=3.5 x.left=-5 y.max=1
doping reg=2 gauss n.type conc=2e19 peak=0.8 char=0.1 x.right=3 x.left=-4
doping reg=2 gauss n.type conc=5e19 peak=0.0 char=0.08 x.right=-3.2
x.left=-4.2

#emiiter L
doping reg=2 gauss n.type conc=5e19 peak=0.0  junct=0.05 x.right=0.8
x.left=-0.8

#base L
```

```
doping reg=2 gauss p.type conc=1e18 peak=0.05 junct=0.15 x.right=2
x.left=-2
doping reg=2 gauss p.type conc=5e19 peak=0.0  char=0.08 x.left=1.5
x.right=2.2
doping reg=2 gauss p.type conc=5e19 peak=0.0  char=0.08 x.left=-2.2
x.right=-1.5

###########

#collector R
doping reg=2 uniform n.type conc=2e16 x.right=23.5 x.left=15 y.max=1
doping reg=2 gauss n.type conc=2e19 peak=0.8 char=0.1 x.right=23 x.left=16
doping reg=2 gauss n.type conc=5e19 peak=0.0 char=0.08 x.right=16.8
x.left=15.8

#emiiter R
doping reg=2 gauss n.type conc=5e19 peak=0.0  junct=0.05 x.right=20.8
x.left=19.2

#base R
doping reg=2 gauss p.type conc=1e18 peak=0.05 junct=0.15 x.right=22
x.left=18
doping reg=2 gauss p.type conc=5e19 peak=0.0  char=0.08 x.left=21.5
x.right=22.2
doping reg=2 gauss p.type conc=5e19 peak=0.0  char=0.08 x.left=17.8
x.right=18.5

# set bipolar models
models bipolar print lat.temp
contact name=emitter tungsten
thermcontact number=1 y.min=10 ext.temper=300

method gummel block newton

solve init
save outf=bjtex11.str
tonyplot  bjtex11.str -set bjtex04_0.set

solve vcollector=0.01
solve vcollector=0.05
solve vcollector=0.1
solve vcollector=0.2

solve vbase=1.8 ramptime=2e-6 tstop=1e-4 tstep=2e-7
save outf=bjtex11.str
tonyplot  bjtex11.str -set soiex05_2.set

#solve vbase=0 ramptime=2e-6 tstop=5.22e-4 tstep=2e-7
#save outf=bjtex11.str
#tonyplot  bjtex11.str -set soiex05_2.set

quit
```

APPENDIX B. AHDL SCRIPT FOR R_3 CONTROLLER

```
// Spectre AHDL for SiGe_KC, deco_3b, ahdl

module deco_3b (sel, s1, s2, s3, s4, s5, s6, s7, s8, s9, s10, s11, s12,
s13, s14, s15, s16 ) ()
node [V, I] sel, s1, s2, s3, s4, s5, s6, s7, s8, s9, s10, s11, s12, s13,
s14, s15, s16;

{
real v[20];
real vl=0;
integer kk;
integer ii;

initial{
      for (ii=0; ii<16; ii++){
                  v[ii]=5;
                  }
      }

analog {
      V(s1) <-$transition( v[0] );
      V(s2) <-$transition( v[1] );
      V(s3) <-$transition( v[2] );
      V(s4) <-$transition( v[3] );
      V(s5) <-$transition( v[4] );
      V(s6) <-$transition( v[5] );
      V(s7) <-$transition( v[6] );
      V(s8) <-$transition( v[7] );
      V(s9) <-$transition( v[8] );
      V(s10) <-$transition( v[9] );
      V(s11) <-$transition( v[10] );
      V(s12) <-$transition( v[11] );
      V(s13) <-$transition( v[12] );
      V(s14) <-$transition( v[13] );
      V(s15) <-$transition( v[14] );
      V(s16) <-$transition( v[15] );

      vl=V(sel);
      kk=vl;
      v[kk]=0;

      for (ii=0; ii<16; ii++){
            if (ii!=kk){
                  v[ii]=5;
                  }
            }

      }

}
```

APPENDIX C. AHDL SCRIPT FOR LEVEL SHIFTER

```
// Spectre AHDL for SiGe_KC, r_string, ahdl

module r_string (in, out, con ) ()
node [V, I] in, out, con;

{
analog      {
      V(out) <- $transition(V(in)* (V(con)*5+6e4)/60640);

      }
}
```

APPENDIX D. AHDL SCRIPT FOR CONTROL/ARITHMETIC UNIT

```
// Spectre AHDL for SiGe_KC, kio, ahdl

module kio (in, ref, clk, clk2,  ss, rdy,  d2, d1, d0 ) ()
node [V, I] in, ref, clk, clk2, ss, rdy, d2, d1, d0;
{
real cup;
real d_temp;

real ll=1250;
real lr=2400;

real lev_p1;
real lev_p2;
real lev_p3;
integer seg_p;
real lev;
real ii;
real indic;
real sig;
real vd0;
real vd1;
real vd2;

integer b0;
integer bn;

integer seg;
integer count;

stream fin;

initial{
      fin = $fopen("memory","r");
      $fread(fin, "%d", seg_p);
      $fread(fin, "%g", lev_p1);
      $fread(fin, "%g", lev_p2);
      $fread(fin, "%g", lev_p3);
      $fclose(fin);

      count=0;
      lev=lev_p1*(seg_p-2)*(seg_p-3)/2 -lev_p2*(seg_p-1)*(seg_p-3)+
lev_p3*(seg_p-1)*(seg_p-2)/2 ;
      indic=0;
      vd2= 0;
      vd1= 5;
      vd0= 0;

      }

analog {
      //select curve
      if ($threshold(V(clk) - 2, 1)) {
      cup=(V(in)-V(ref)*1.16)/0.335/V(ref)*4096;
```

```
      d_temp=floor(cup);

      if( d_temp<= ll){
            seg=1;
            vd0=5;
            vd1=0;
            vd2=0;        }
      if((  d_temp > ll)&(d_temp <= lr)){
            seg=2;
            vd1=5;
            vd0=0;
            vd2=0;        }
      if( d_temp> lr){
            seg=3;
            vd2=5;
            vd1=0;
            vd0=0;        }

      //
      //check for first time turn on
      //
      if (seg_p==0){
            if (seg==1){
            lev_p1=127; }
            if (seg==2){
            lev_p2=64;  }
            if (seg==3){
            lev_p3=1;   }
      indic=5;
            }
      //
      //set Vready and level
      //

      ii=lev_p1*(seg-2)*(seg-3)/2 -lev_p2*(seg-1)*(seg-3)+ lev_p3*(seg-
1)*(seg-2)/2 ;
      if (ii){
      lev=ii;
      indic=5;    }

            }
            //
            //assign output
            //
            V(d2) <-  $transition( vd2) ;
            V(d1) <-  $transition( vd1) ;
            V(d0) <-  $transition( vd0) ;

      ////////////////////////////////////////////////////////////////
      //
      //fix DC level
      //
      V(rdy) <- $transition( indic );
      V(ss) <- $transition( lev);
```

```
if ((indic==0)&($threshold(V(clk2) - 2.5, 1.0))) {
      count +=1;

      if(seg_p != seg ){
      if (count==1){

      if (seg_p==1){
      vd0=5;
      vd1=0;
      vd2=0;       }
      if (seg_p==2){
      vd1=5;
      vd2=0;
      vd0=0;       }
      if (seg_p==3){
      vd2=5;
      vd1=0;
      vd0=0;       }
      }

      if (count==3){
      b0=(V(in)-1.16*V(ref))/0.335/V(ref)*4096; }

      if (count==4){
            if (seg==1){
            vd0=5;
            vd1=0;
            vd2=0;       }
            if (seg==2){
            vd1=5;
            vd0=0;
            vd2=0;       }
            if (seg==3){
            vd2=5;
            vd1=0;
            vd0=0;       }
            }

      if (count==5)      {
            bn=(V(in)-1.16*V(ref))/0.335/V(ref)*4096;

            if (b0>bn){
                  sig=-1;            }
            if (b0<bn){
                  sig=1;             }
                  }

      if ((count >5)& !(indic)){

            if (bn<b0){
            lev -=1;
                  }
            if (bn>b0){
            lev +=1;
                  }
```

```
                    bn=(V(in)-1.16*V(ref))/0.335/V(ref)*4096;
                    if (((b0-bn)==0)|(sig*(b0-bn)>0)){
                    indic=5;    }

                    if (seg==1){
                    lev_p1=lev; }
                    if (seg==2){
                    lev_p2=lev; }
                    if (seg==3){
                    lev_p3=lev; }
              }
              }
      }}
final {
      if (indic){
      fin = $fopen("memory","w");
      $fstrobe(fin,"%d \n", seg);
      $fstrobe(fin,"%g \n", lev_p1);
      $fstrobe(fin,"%g \n", lev_p2);
      $fstrobe(fin,"%g \n", lev_p3);
      $fstrobe(fin,"%g \n", d_temp);
      $fclose(fin);     }
      }
}
```

APPENDIX E. AHDL SCRIPT FOR CALIBRATION SCHEME

```
// Spectre AHDL for SiGe_KC, sel_peak, ahdl

module sel_peak (en, clk, sel, in, ref ) ()
node [V, I] en, clk, sel, in, ref;
{
integer b[16];
real lev;
integer ok;
integer count;
integer cup=0;
integer l_set=1;
integer sign=-1;
integer dim=0;
integer vipe;

integer ii=0;
integer jj=0;

stream fmem;

initial     {

      fmem = $fopen("cache","r");
      for (ii=0; ii<16; ii++) {
      $fread(fmem, "%d", b[ii]);     }
      $fread(fmem, "%d", vipe );
      $fread(fmem, "%d", ok );
      $fclose(fmem);

      lev=vipe;
      ii=0;
      count=0;
      }

analog      {

      V(sel) <-$transition( lev );


      if ((ok!=3)&(V(en)>1.5)) {
      //
      //take first reading; ok= 0 -> 1
      //
      if ((!ok)&($threshold(V(clk) - 2.5, 1.0)))      {
            count +=1;

            for (ii=0; ii<16; ii++){
                  if (count==2*ii+1)      {
                  b[ii]=(V(in)-1.105*V(ref))/0.32/V(ref)*4096;     }
                  if ((count==2*ii)&(lev<15))    {
                  lev +=1;     }
                  }
```

```
            }

      if ((!ok)&(b[15]>0))    {
            ok=1; }


      //     .
      //take second reading; set ok= 1 -> 2; remember & set level
      //

      if ((ok==1)&($threshold(V(clk) - 2.5, 1.0)))    {
            count +=1;
            if (count==1){
            cup=b[jj]-(V(in)-1.105*V(ref))/0.32/V(ref)*4096;
            b[jj]=cup;
                  if (cup<0) {
                        ok=3;
                        vipe=lev; }
            }
            if ((count==2))   {
                  count=0;

                  if (jj<15)  {
                  jj +=1;           }

                  if (lev<15) {
                        lev +=1;
                              }
                        }

            }
            }

      }

final {
      fmem = $fopen("cache","w");
      for (ii=0; ii<16; ii++) {
      $fstrobe(fmem, "%d\n", b[ii]);      }
      $fstrobe(fmem, "%d\n", vipe );
      $fstrobe(fmem, "%d\n", ok );
      $fclose(fmem);
      }

}
```

APPENDIX F. DERIVATION OF EQUATION 2.4

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \tag{2.1}$$

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) \tag{2.2}$$

$$I_S = \frac{q\left[AT^3 \exp\left(\frac{-V_{go}}{V_T}\right)\right](V_T B T^{-n}) A_e}{Q_B} \tag{2.3}$$

Let V_{BE} at temperature T and T_O be

$$V_{BE}(T) = V_T \ln\left(\frac{I_C(T)}{I_S(T)}\right) \tag{X.1}$$

And

$$V_{BE}(T_O) = V_{T_O} \ln\left(\frac{I_C(T_O)}{I_S(T_O)}\right) \tag{X.2}$$

Where

$$V_{T_O} = \frac{kT_O}{q} \tag{X.3}$$

Manipulating (X.1) and (X.2)

$$T_O \cdot V_{BE}(T) - T \cdot V_{BE}(T_O) = \frac{kT \cdot T_O}{q} \ln\left(\frac{I_C(T)}{I_S(T)} \cdot \frac{I_S(T_O)}{I_C(T_O)}\right) \tag{X.4}$$

$$V_{BE}(T) = \frac{T}{T_O}\left(V_{BE}(T_O) + \frac{kT_O}{q} \ln\left(\frac{I_C(T)}{I_S(T)} \cdot \frac{I_S(T_O)}{I_C(T_O)}\right)\right) \tag{X.5}$$

Substituting the I_S expression (2.3) into (X.5)

$$V_{BE}(T) = \frac{T}{T_O}\left(V_{BE}(T_O) + \frac{kT_O}{q} \ln\left(\frac{I_C(T)}{I_C(T_O)} \cdot \frac{{T_O}^{4-n} \exp\left(\frac{-V_{go}}{V_{TO}}\right)}{T^{4-n} \exp\left(\frac{-V_{go}}{V_T}\right)}\right)\right) \tag{X.6}$$

Simplifying (X.6)

$$V_{BE}(T) = \frac{T}{T_O} V_{BE}(T_O) + \frac{kT}{q} \ln\left(\frac{I_C(T)}{I_C(T_O)}\right) + \frac{kT}{q} \ln\left(\frac{{T_O}^{4-n}}{T^{4-n}}\right) + \frac{kT}{q} \ln\left(\frac{\exp\left(\frac{-V_{go}}{V_{TO}}\right)}{\exp\left(\frac{-V_{go}}{V_T}\right)}\right) \tag{X.6a}$$

$$V_{BE}(T) = \frac{T}{T_O} V_{BE}(T_O) + \frac{kT}{q} \ln\left(\frac{I_C(T)}{I_C(T_O)}\right) + \frac{kT}{q} \ln\left(\frac{{T_O}^{4-n}}{T^{4-n}}\right) + V_{go} - V_{go}\frac{T}{T_O} \tag{X.6b}$$

$$V_{BE}(T) = V_{go} - \frac{T}{T_O}\left(V_{go} - V_{BE}(T_O)\right) + \frac{kT}{q} \ln\left(\frac{I_C(T)}{I_C(T_O)}\right) - (4-n)\frac{kT}{q} \ln\left(\frac{T}{T_O}\right) \tag{X.6c}$$

Introduce new variables S and x where S is a scale factor and x represents the order of temperature dependence of collector current I_C.

$$I_C(T) = ST^x \tag{X.7}$$

Substitute (X.7) into (X.6c)

$$V_{BE}(T) = V_{go} - \frac{T}{T_O}\left(V_{go} - V_{BE}(T_O)\right) + \frac{kT}{q}\ln\left(\frac{T^x}{T_O{}^x}\right) - (4-n)\frac{kT}{q}\ln\left(\frac{T}{T_O}\right) \tag{X.8}$$

$$V_{BE}(T) = V_{go} - \frac{T}{T_O}\left(V_{go} - V_{BE}(T_O)\right) - (4-n-x)\frac{kT}{q}\ln\left(\frac{T}{T_O}\right) \tag{X.8a}$$

Equation (2.4) is obtained by substituting $V_T = \frac{kT}{q}$ into (X.8a)

$$V_{BE} = V_{go} - \frac{T}{T_o}\left[V_{go} - V_{BE}(T_o)\right] - \left[(4-n) - x\right]V_T \ln\left(\frac{T}{T_o}\right) \tag{2.4}$$

APPENDIX G. DERIVATION OF EQUATION 2.5

$$V_{BE} = V_{go} - \frac{T}{T_o}\left[V_{go} - V_{BE}(T_o)\right] - \left[(4-n)-x\right]V_T \ln\left(\frac{T}{T_o}\right) \tag{2.4}$$

Let

$$\eta = 4 - n \tag{X.1}$$

Rewrite (2.4) and substitute $V_T = \frac{kT}{q}$

$$V_{BE} = V_{go} - \frac{T}{T_o}\left[V_{go} - V_{BE}(T_o)\right] - (\eta - x)\left(\frac{T_o}{T_o}\right)\frac{kT}{q}\ln\left(\frac{T}{T_o}\right) \tag{X.2}$$

Substitute $\frac{kT_o}{q} = V_{To}$

$$V_{BE} = V_{go} - \frac{T}{T_o}\left[V_{go} - V_{BE}(T_o)\right] - (\eta - x)V_{To}\frac{T}{T_o}\ln\left(\frac{T}{T_o}\right) \tag{X.2a}$$

$$V_{BE} = V_{go} - \frac{T}{T_o}\left[V_{go} - V_{BE}(T_o)\right] - (\eta - x)V_{To}\left(\frac{T}{T_o}\ln\left(\frac{T}{T_o}\right) + \left(\frac{T}{T_o} - 1\right) - \left(\frac{T}{T_o} - 1\right)\right) \tag{X.2b}$$

$$V_{BE} = V_{go} - \frac{T}{T_o}\left[V_{go} - V_{BE}(T_o)\right] - (\eta - x)\frac{V_{To}}{T_o}\left(T\ln\left(\frac{T}{T_o}\right) + (T - T_o) - (T - T_o)\right) \tag{X.2c}$$

$$V_{BE} = V_{go} - \frac{T}{T_o}\left[V_{go} - V_{BE}(T_o)\right] - (\eta - x)\frac{V_{To}}{T_o}\left(T\ln\left(\frac{T}{T_o}\right) - (T - T_o)\right) - (\eta - x)\frac{V_{To}}{T_o}(T - T_o) \tag{X.2d}$$

$$V_{BE} = V_{go} - \frac{T}{T_o}\left[V_{go} - V_{BE}(T_o)\right] - (\eta - x)\frac{V_{To}}{T_o}\left(T\ln\left(\frac{T}{T_o}\right) - (T - T_o)\right) - (\eta - x)V_{To}\frac{T}{T_o} + (\eta - x)V_{To} \tag{X.2e}$$

$$V_{BE} = \left[V_{go} + (\eta - x)V_{T_o}\right] - \left[\frac{V_{go} - V_{BE}(T_o) + (\eta - x)V_{T_o}}{T_o}\right]T - \left\{\frac{(\eta - x)V_{T_o}}{T_o}\left[T\ln\left(\frac{T}{T_o}\right) - T + T_o\right]\right\}$$

(X.2f)

Equation (X.2f) is identical to (2.5).

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