A digital background calibration technique for pipeline ADCs

by

Anilkumar Venkata Tammineedi

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Graduate College
Iowa State University

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Anilkumar Venkata Tammineedi

has met the thesis requirements of Iowa State University

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ADC	Analog to Digital Converter
A_o	Open Loop Gain of Op-amp
C_s	Sampling Capacitor
C_f	Feedback Capacitor
CMFB	Common Mode Feedback Circuit
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analog Converter
DNL	Differential Non-linearity
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
INL	Integral Non-linearity
K	Boltzmann's Constant (1.38e-23 J/K)
LSB	Least Significant Bit
MSB	Most Significant Bit
op-amp	Operational Amplifier
Q_{in}	Input Charge
S/H	Sample and Hold
SAR	Successive Approximation Register
SFDR	Spurious Free Dynamic Range
SNR	Signal to Noise Ratio
SNDR	Signal to Noise and Distortion Ratio

$\mathbf{T}$	Absolute Temperature
$\mathbf{V_{LSB}}$	Voltage Equivalent of 1 LSB
$\mathbf{V_{refn}}$	Negative Reference Voltage
$\mathbf{V_{refp}}$	Positive Reference Voltage
β	Feedback Factor of Closed Loop

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Finally I would like to thank my family for their incredible support and encouragement throughout, making me what I am today. I dedicate this small piece of work to my family, friends and teachers.

ABSTRACT

There is a constant increase in demand for high-resolution, high-speed Analog to Digital converters (ADCs) for applications in imaging systems (Ultrasonic, DVD, etc.), medical instrumentation and broadband communication systems. This has been the driving force in the development of numerous ADC architectures and techniques existing today, and further ongoing research. Among the different topologies, pipeline architecture has the advantage of combining both good speed and moderate resolution capabilities in the ADC.

Calibration is a technique to correct for errors after fabrication of the ADC to improve it's resolution. This work focuses on background (continuous) calibration which has the advantage of maintaining the high-resolution of the ADC even in the presence of environmental and power supply variations on the integrated circuit, by constantly correcting for errors without disturbing the data flow in the converter. A novel digital background calibration technique for pipeline ADCs employing non-radix 2 calibration algorithm and an extra stage is proposed.

The digital calibration removes errors due to capacitor mismatch, charge injection, finite op-amp gain and comparator offset. Neither external data converters nor high-precision analog components are required for calibration. Background calibration is achieved without limiting the speed of conversion, the cost being one extra stage and digital hardware. This technique would help to achieve high-resolution capabilities in the available CMOS technologies. A 3.3V, 12-bit, 25MHz pipeline ADC with the proposed calibration technique has been implemented in $0.35\mu m$ CMOS technology.

1 INTRODUCTION

1.1 Motivation

An effective and low cost technique to produce high-resolution analog to digital converters (ADCs) is calibration, wherein the errors are measured after the fabrication of the integrated circuit and corrected for. With background calibration, the errors can be corrected without interrupting the operation of the converter thus, maintaining the required resolution at all times even in the presence of environmental and power supply variations. This forms the motivation in developing new cost-effective techniques for background (continuous) calibration.

1.2 Organization of Thesis

This thesis aims to address key issues in the design of ADCs for better understanding of the need for calibration in general and background calibration in particular. This chapter identifies some of the important performance metrics used to evaluate the performance of ADCs and then reviews some of the available ADC architectures.

Chapter 2 discusses pipeline architectures in detail and analyses sources of errors and their effects with a design perspective. The motivation for the calibration method used in this work is derived from the study of the transfer characteristics of pipeline ADCs.

Chapter 3, the central focus of this work, studies two available digital self-calibration methods and introduces a background calibration technique based on these two methods.

Chapter 4 discusses some key design issues in general for pipeline ADCs and in particular for the 3.3 V, 12-bit, 25MHz prototype ADC with the proposed background calibration technique. Observations derived from this work and some future directions are presented in Chapter 5.

1.3 ADC Definition

An Analog to Digital converter is a device that converts real world (analog) signals to digital codes. The total analog range is divided into different steps (subranges) and to each step a digital code is assigned. Then during the conversion process, the input analog signal is mapped into one of these subranges and the appropriate digital code is measured [6].

The simplest ADC is a comparator which constitutes a 1-bit ADC. If the analog input is in the lower half of the total range, the output is a digital zero and if it is in the upper half of the total range, the output is a digital one. As an example a simple 2-bit ADC is illustrated in Figure 1.1. If the analog input signal is between 0 and 0.25 volt, the 2-bit output is 00 and if the input is between 0.75 and 1 volt, the 2-bit output is 11.

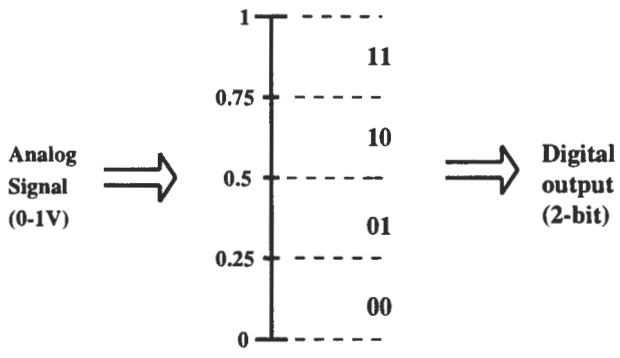

Figure 1.1 Description of a 2-bit ADC

1.4 ADC Characterization

ADCs are characterized in a number of different ways to indicate their performance capability. Some of the important characteristics of ADCs are introduced below.

1.4.1 Resolution

Resolution describes the level of quantization performed by the ADC. Resolution is usually defined as the base 2 logarithm of the number of subranges the input range is divided into. Thus, an N-bit resolution implies that the converter can resolve 2^N distinct analog levels. Resolution usually refers to the number of digital output bits and is not necessarily the absolute accuracy of the converter [3].

An $\mathbf{V_{LSB}}$ is defined as the voltage change required at the input to change the output digital code by one least significant bit (LSB). Mathematically, for an N-bit converter with full scale analog input range of V_{ref} it is given by,

$$V_{LSB} = \frac{V_{ref}}{2^N} \tag{1.1}$$

In this thesis, V_{LSB} is also represented as LSB for simplicity. So, for a 2-bit ADC having a full scale input range of 1 volt, the V_{LSB} (LSB) is given by,

$$V_{LSB} = \frac{1}{2^2} = 0.25 \text{ volts} \tag{1.2}$$

1.4.2 Nonlinearity

ADCs in most applications are required to have a linear transfer characteristic that approximates a straight line as shown by the dotted line in Figure 1.2. The transfer characteristic for an ideal ADC progresses in a series of uniform steps. Hence, nonlinearity is inherently present even in an ideal ADC. The transfer characteristic of a practical ADC contains steps which are not perfectly uniform and this deviation contributes to further nonlinearity as shown in Figure 1.2. Two types of nonlinearity are used to characterize

practical ADCs. Differential Non-Linearity (**DNL**) is defined as the measure of the deviation of the analog step sizes from the nominal step size of 1 LSB. Mathematically it is expressed as:

$$DNL(i) = A(i) - 1LSB \quad 0 \leq i \leq 2^N - 1 \tag{1.3}$$

where $A(i)$ is the actual analog step size for an N-bit converter. Thus for an ideal converter the maximum DNL is 0 for all digital values since all step sizes are 1 LSB.

Integral Non-Linearity (**INL**) is defined as the deviation of the transfer characteristic form the ideal characteristic. However there have been different ways of defining the actual transfer characteristic which by some is defined as the best-fit straight line such that the maximum difference is minimized and by others as the straight line obtained by connecting the two endpoints of the transfer response. Mathematically, INL is the cumulative of DNL.

$$INL(i) = \sum_{k=0}^{i} DNL(k) \quad 0 \leq i \leq 2^N - 1 \tag{1.4}$$

INL and DNL are generally expressed in terms of LSBs. The illustration of INL and DNL is shown in Figure 1.2.

1.4.3 Monotonicity

A *Monotonic* ADC is one in which the output digital code always increases for an increasing input. Monotonicity is an important specification for most ADCs since when they are used in feedback systems, non-monotonicity may cause a positive feedback and lead to instability of the system. An ADC is guaranteed to be monotonic if the maximum INL is less than 1/2LSB [1].

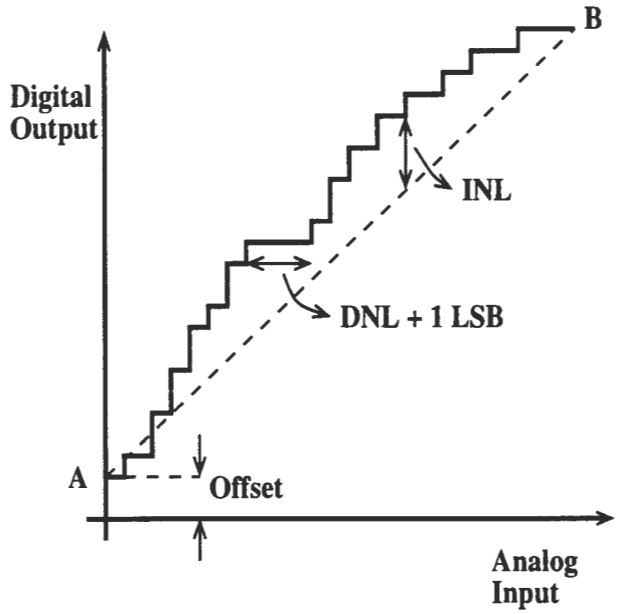

Figure 1.2 Illustration of INL and DNL Errors

1.4.4 Signal to Noise Ratio (SNR)

The signal to noise ratio (SNR) is the ratio of the signal power to the noise power in the output of the ADC. SNR can be easily measured from the spectrum of the output of the ADC. SNR is usually represented in dB and is calculated by measuring the difference between the signal peak and the noise floor and including a factor to adjust for the number of samples used to generate the spectrum as shown below.

$$SNR(dB) = Signalpeak(dB) - Noisefloor(dB) - 10 * logN \tag{1.5}$$

To generate an N-point FFT of a signal, N samples of the signal are taken. Sampling the signal N times increases the signal energy by a factor of N^2 and the noise energy by a factor of N. Thus the signal power to noise power is increased by a factor of N. The SNR improvement in dB is 10*logN. This is the reason for subtracting 10*logN in the above equation [6]. Thus, the noise floor in the FFT becomes lower relative to the signal as more samples are taken.

1.4.5 Signal to Noise and Distortion Ratio (SNDR)

The SNDR is also used to measure the performance of an ADC. It measures the degradation in signal power due to the combined effect of noise, quantization errors and harmonic distortion. The quantization of the analog input signal into a number of amplitude-discrete levels places limitations on the accuracy with which the signal can be reproduced. This error is referred to as 'quantization error' [1]. The SNDR of a system is usually measured for a sinusoidal input and is a function of the frequency and amplitude of the input signal. When a sinusoidal signal of a single frequency is applied to the system, the output of the system generally contains a signal component at the input frequency, referred to as harmonic distortion. Due to distortion, the output also contains signal components at harmonics of the input frequency. An ADC usually samples an input signal at some finite rate. As a result, some of the harmonic distortion products are aliased down to lower frequencies. The SNDR of the ADC is defined as the ratio of the signal power in the fundamental to the sum of the power in all of the harmonics, all of the aliased harmonics and all of the noise. Theoretically the $SNDR_{max}$ for an N-bit converter is given by,

$$SNDR_{max} = 6.02N + 1.76\ dB \tag{1.6}$$

1.4.6 Spurious Free Dynamic Range (SFDR)

Dynamic range of an ADC is a useful performance benchmark. Dynamic range is a measure of the range of input signal amplitudes for which useful output can be obtained from a system. SFDR is a frequency domain characteristic to define the dynamic range. SFDR is defined as the ratio between the maximum signal component and the largest distortion component. Converters with a good integral linearity usually give an SFDR that is larger than the SNR [1]. SFDR is illustrated in Figure 1.3.

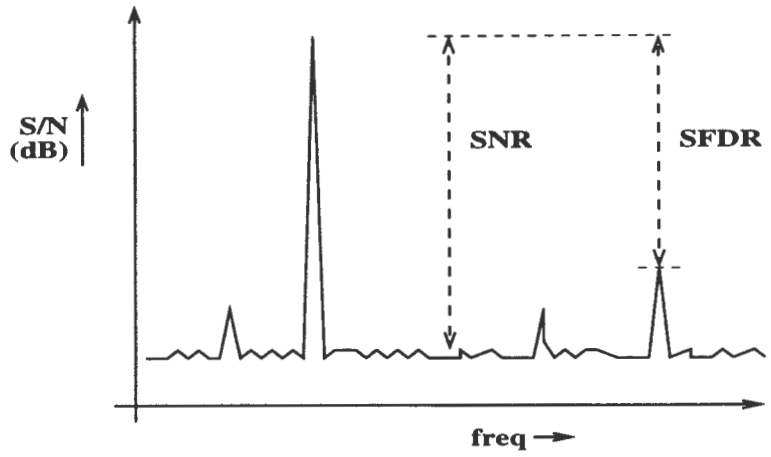

Figure 1.3 Illustration of SNR and SFDR

1.5 ADC Architectures

ADCs has been one of the highly studied and researched areas in analog circuit design. As a result, a number of techniques and architectures have been developed during the years. In this section, some of the prominent architectures are introduced and compared.

1.5.1 Flash ADC

The flash ADC architecture is one of the most straightforward ways to implement ADCs and also fundamentally the fastest architecture. Figure 1.4 shows the block diagram of a n-bit flash ADC. It consists of an array of $2^n - 1$ comparators and a set of $2^n - 1$ reference levels usually generated by a resistor string. Each of the comparators compare the input to the corresponding reference value and makes a decision if the input is greater or less than the reference value. The set of $2^n - 1$ comparator outputs are referred to as the thermometer code. This is passed on to a encoder which converts the thermometer code to the n-bit binary code [1].

The conversion speed is limited only by the speed of the comparator since all the

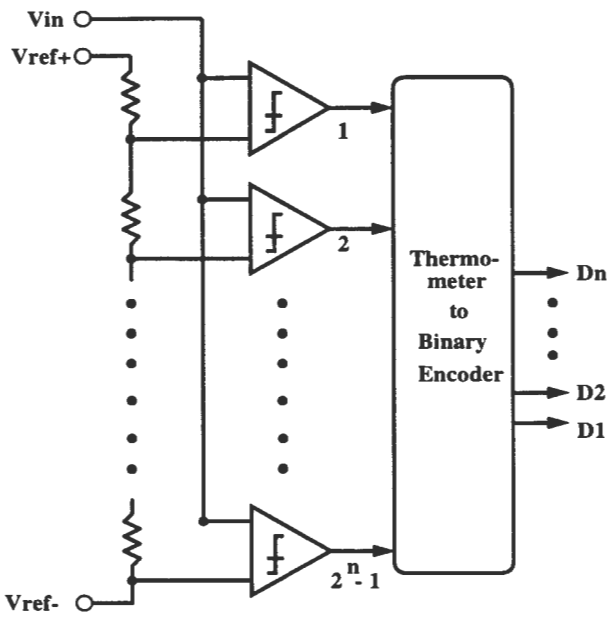

Figure 1.4 Block Diagram of Flash ADC

comparators operate in parallel. Hence, flash ADCs are capable of very high speed. However, Flash ADCs suffer from several drawbacks. Some of these are briefly mentioned below.

- Loading - The large number of comparators connected to Vin results in a large parasitic loading at the node Vin. This limits the analog input bandwidth and the nonlinearities of the capacitance introduces harmonic distortion of the sampled signal [2].

- Bowing - The input currents of bipolar comparators cause errors in voltages of the nodes of the resistor string. These errors cause the bias current in the resistor string to be different from the input currents of the comparators. The AC coupling due to capacitances in CMOS also causes a similar effect. This error contributes to the integral nonlinearity [2].

- Kickback noise - Latched comparators generate a great deal of noise at their inputs

during the transition from latch to track mode or vice-versa. This is because of the unmatched impedances at the comparator inputs (one input goes to the resistor string while the other goes to the input signal). If this noise does not decay fast enough, the next input sample would have an error [2].

- Metastability - Metastability occurs in comparators when the input difference is small making the circuit to take a long time to produce a well-defined logic output causing an erroneous digital output [2].

1.5.2 Two-step ADC

A two-step ADC consists of two stages, each containing a flash ADC. Figure 1.5 illustrates the block diagram of a two-step ADC. During the first step, the most significant bits of the output are determined by the first stage flash ADC. Then the DAC converts this digital data back into analog signal to be subtracted from the input signal. This residue of the subtraction is then passed on to the second stage to determine the least significant bits. The first step is usually referred to as coarse-quantization and the second as fine-quantization.

The conversion time for a two-step ADC is longer than a simple flash, but it is still very fast. Furthermore, the two-step ADC requires only $2*2^{\frac{n}{2}}$ comparators, thus leading to large saving in hardware and power. Note that the input to the second stage has the cumulative error of the DAC and the subtracter, thus demanding the second stage to resolve the input correctly even in the presence of the error, which is very difficult to achieve. This can be relaxed if the subtracter is followed by an amplifier of gain A, reducing the requirement of the second stage by the same factor. However, this amplifier adds a finite delay to the conversion period and can contribute to nonlinearities.

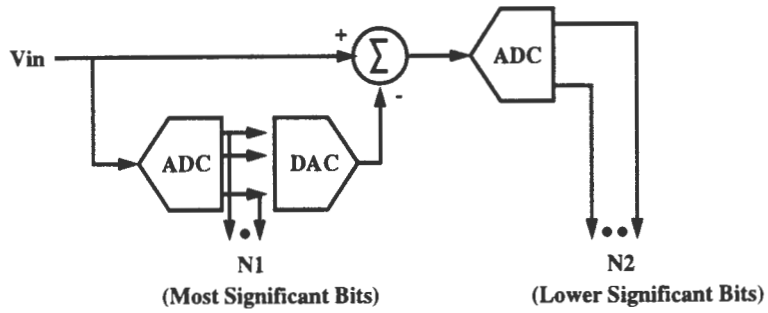

Figure 1.5 Block Diagram of a Two-step ADC

1.5.3 Folding ADC

Folding architectures have evolved from Two-step and Flash topologies. A folding architecture is similar in operation to a two-step converter in that a group of LSBs are found separately from a group of MSBs. However, whereas a two-step converter requires an accurate DAC, a folding converter determines the LSB directly through the use of analog preprocessing while the MSBs are determined at the same time [3]. The basic principle is to generate a residue voltage through analog preprocessing and subsequently digitize that residue to obtain the least significant bits. The most significant bits can be resolved using a coarse flash stage that operates in parallel with the folding circuit and hence samples the signal at approximately the same time that the residue is sampled.

The simplicity and the speed of folding circuits have made them popular particularly because they eliminate the need of S/H, DAC and subtracters. Nevertheless, these circuits suffer several drawbacks that limit their use for resolutions above 10 bits. One of the major drawbacks is its substantial nonlinearity. Also, the nonlinearity errors are dependent on the frequency of operation. Another drawback is that a folding factor of n results in frequency multiplication by n. Thus, the bandwidth required for the folding circuit is n times that of the input frequency imposing strong trade-offs among speed and power dissipation. Recently, to remove the nonlinearity problem folding architectures

are combined with interpolation techniques [2].

1.5.4 Successive Approximation ADC

The successive approximation method is also known as the 'binary search' method since it applies the binary search algorithm to determine the closest digital word to match the input signal. Successive approximation ADCs are popular for achieving good resolution with only moderate circuit complexity. Figure 1.6 illustrates the block diagram of the successive approximation ADC. It only consists of a Sample-and-Hold (S/H).a comparator, a Digital to Analog converter (DAC) and a digital logic circuit, referred to as the Successive approximation Register (SAR) to control the DAC.

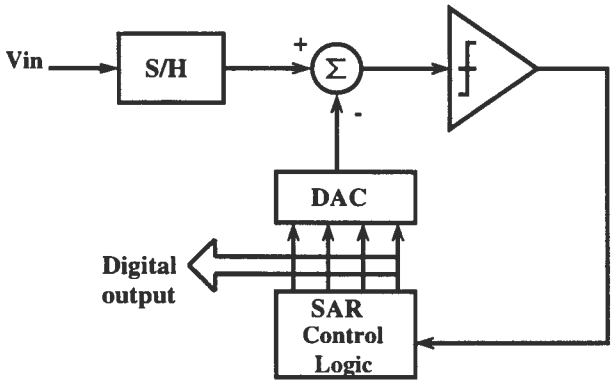

Figure 1.6 Block Diagram of Successive Approximation ADC

The flow chart of the successive approximation algorithm is illustrated in Figure 1.7 [3]. The flow chart is for a signed conversion i.e., the input is signed ($\pm$) and the output has a sign bit. The operation of the successive approximation ADC is as follows. The SAR is initialized and this initializes the output of the DAC. A sample of the input signal is taken by the S/H and the initial DAC output is subtracted from the input sample. The difference is quantized by the comparator which controls the SAR to either increase or decrease the DAC output. The new DAC output is again subtracted from the

input sample, and the process repeats until the desired accuracy is obtained. The single comparator successive approximation ADC resolves one bit per cycle. This architecture has the advantage of using very little hardware. However, the disadvantage is that the number of cycles required for the conversion is proportional to the number of bits. Hence, this is much slower than the flash and two-step architectures.

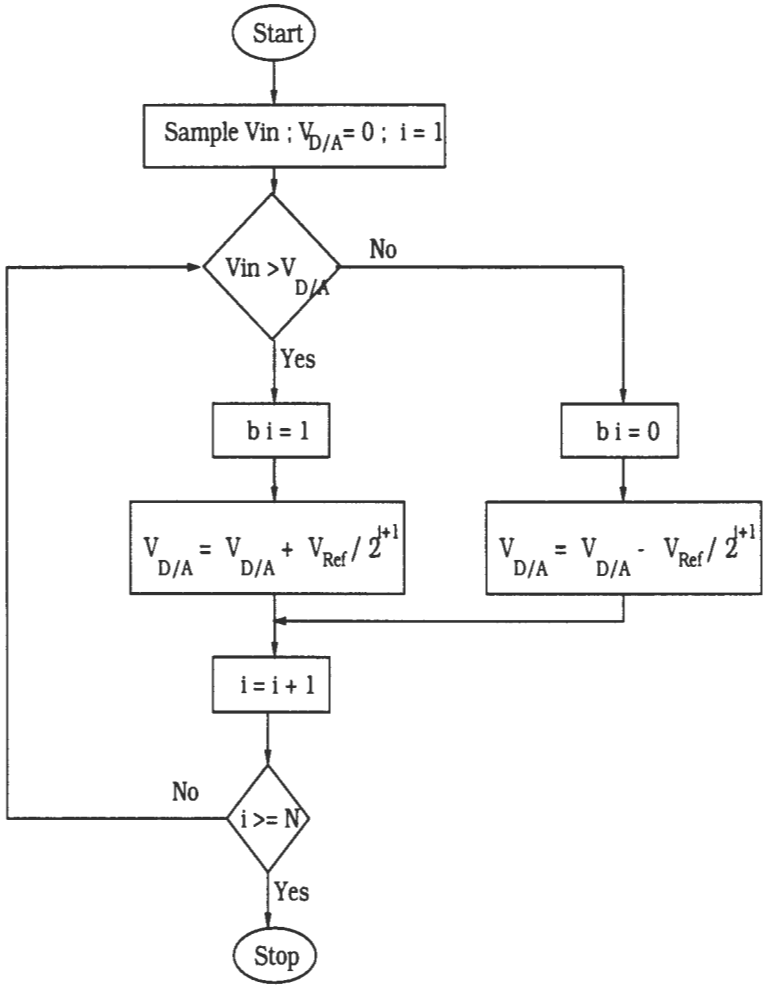

Figure 1.7 Flow Chart of a Successive Approximation ADC

1.5.5 Sigma-Delta ADC

Sigma-delta converters achieve high resolution with relatively little hardware. This is achieved by pushing the quantization noise to high frequencies and removing it with a digital filter. Figure 1.8 shows the block diagram of a first order, sigma-delta ADC. The analog input is quantized and the DAC converts it back to the analog signal which is subtracted from the input signal. The transfer function from the input (V_{in}) to the output (Y) is a delay. If the quantizer is modeled as additive white quantization noise, the converter can be treated as a linear system. Now the transfer function of the quantization noise q to the output Y is a high-pass. Thus, the quantization noise at low frequencies is suppressed as shown in Figure 1.9. The remaining high frequency quantization noise can be removed with a digital low-pass filter. The benefits increase as the sampling rate is increased.

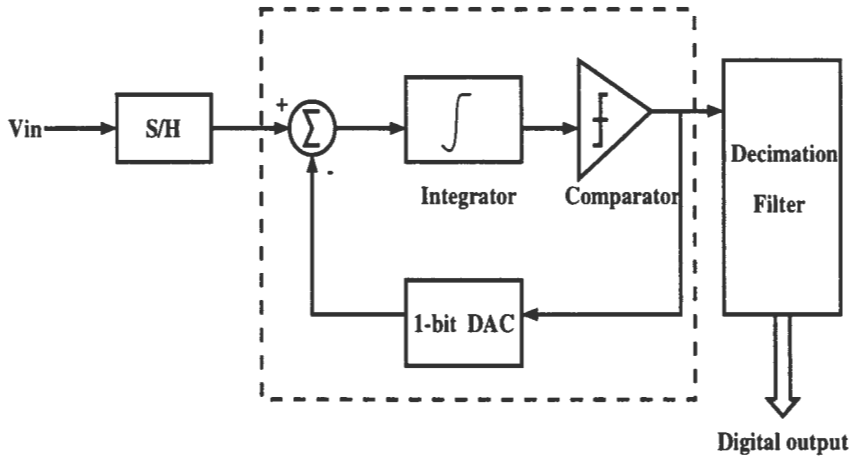

Figure 1.8 Block Diagram of a Sigma-delta Converter

The ratio of the sampling rate and the input signal bandwidth is known as the oversampling ratio. The ideal output SNR increases 9dB per octave in oversampling ratio. Thus, sigma-delta converters can achieve very high resolution for small signal frequencies, such as audio applications. Furthermore, more integrators can be added to

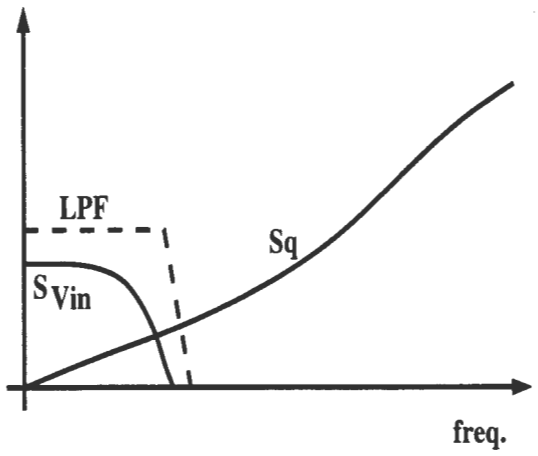

Figure 1.9 Power Spectral Density of a Sigma-delta Modulator's Output

increase the noise-shaping characteristics of the system. This further reduces the low frequency noise, however too many integrators introduce loop stability problems [4].

1.5.6 Pipeline ADC

The two-step architecture that was already discussed can be generalized to multiple stages, with each stage giving rise to certain number of output bits. There have been both single bit-per-stage and multiple bit-per-stage architectures. The first stage contributes the most significant bits and the last stage contributes the least significant bits. Figure 1.10 illustrates the block diagram of a pipeline ADC with N stages. With this kind of architecture, the concept of *pipeline* is very useful in getting a very high throughput. This is because, when the first stage has processed the input and the residue of the first stage proceeds to the second stage, the first stage instead of being idle, can be used to process the next input sample. Thus the concept of pipelining helps in getting a very high throughput.

Each stage of the pipeline ADC consists of a Sample-and-hold,a low resolution ADC, a low resolution DAC, and an interstage amplifier as shown in Figure 1.10. The amplifier

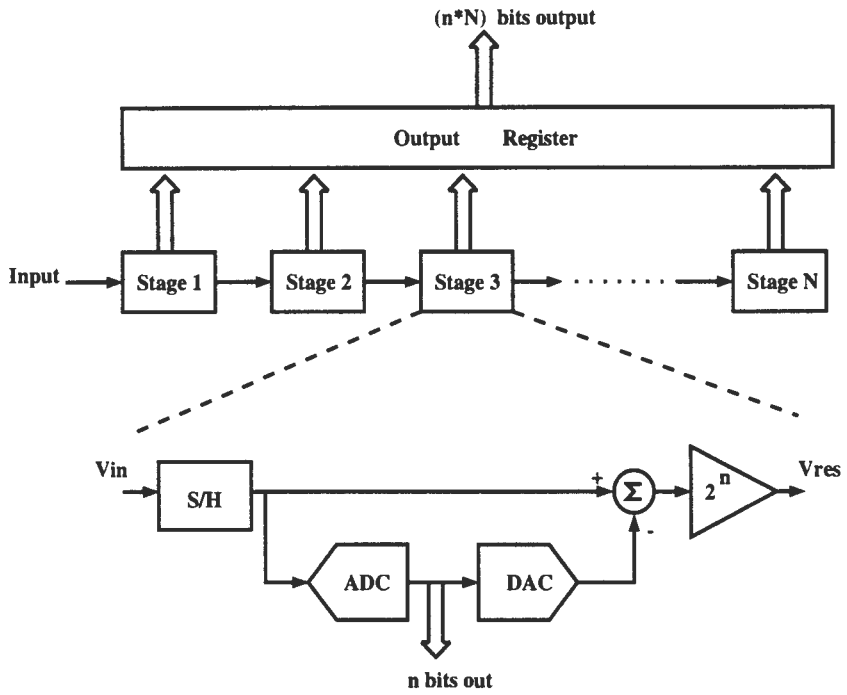

Figure 1.10 Block Diagram of a Pipeline ADC

is used to amplify the residue before passing it on to the next stage. By doing this, the resolution requirements for the following stages are relaxed.

While the concurrent operation of pipelined converters makes them attractive for high speeds, their processing of the analog input relies heavily on operational amplifiers (op-amps), which are relatively slow building blocks in analog design. The maximum allowable gain error and nonlinearity of the S/H and the residue amplifier should be well within 1LSB for the first few stages, thus mandating the use of high-gain op-amps in high resolution converters. The number of bits resolved in each stage and hence the number of stages of a pipelined ADC depend on various considerations such as resolution, speed and technology. Pipeline architectures, in principle, require less power and area than full-flash configurations. This is especially evident from the 1-bit-per-stage topology, where area and power grow linearly rather than exponentially, with the number of bits.

2 PIPELINE ADC CHARACTERISTICS AND ERRORS

In this chapter, the pipeline architecture will be discussed in detail and the different error sources and their effects on the transfer characteristic shall be analyzed.

2.1 Pipeline Architecture

A Typical 1-bit per stage pipeline A/D converter is first considered to understand the common sources of errors and the need for calibration. A simplified block diagram of an N-stage, 1-bit per stage, ADC is shown in Figure 2.1. The analog input goes to the sample-and-hold (S/H) amplifier followed by the successive pipeline stages, each consisting of an interstage S/H amplifier, an amplifier with a nominal gain of 2, a 1-bit digital-to-analog (D/A) converter, a 1-bit A/D converter and an analog subtracter. The front-end S/H amplifier is not necessary to implement the pipeline. Thus, N successive stages constitute the complete N-bit A/D converter.

Figure 2.1 can also be redrawn as Figure 2.2 where the S/H stage gives the first output bit and Stage 1 gives the second bit and so on. These are the two different ways of interpreting the operation of a pipeline ADC that is available in literature. In this work, Figure 2.2 is used for the implementation.

To understand the sources for errors, we need to consider the implementation of the single stage of the pipeline. The 1-bit ADC (also known as sub-ADC) is implemented by a comparator that senses the difference between the analog input to that stage and a threshold voltage V_{th}. The 1-bit DAC (also known as sub-DAC) is implemented by

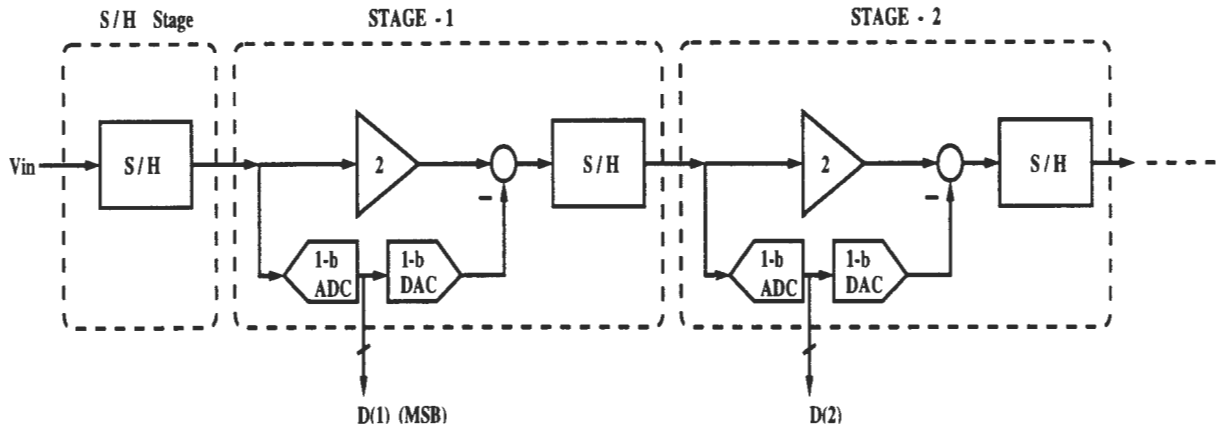

Figure 2.1 Block Diagram of a Pipeline ADC Showing Blocks in Each Stage

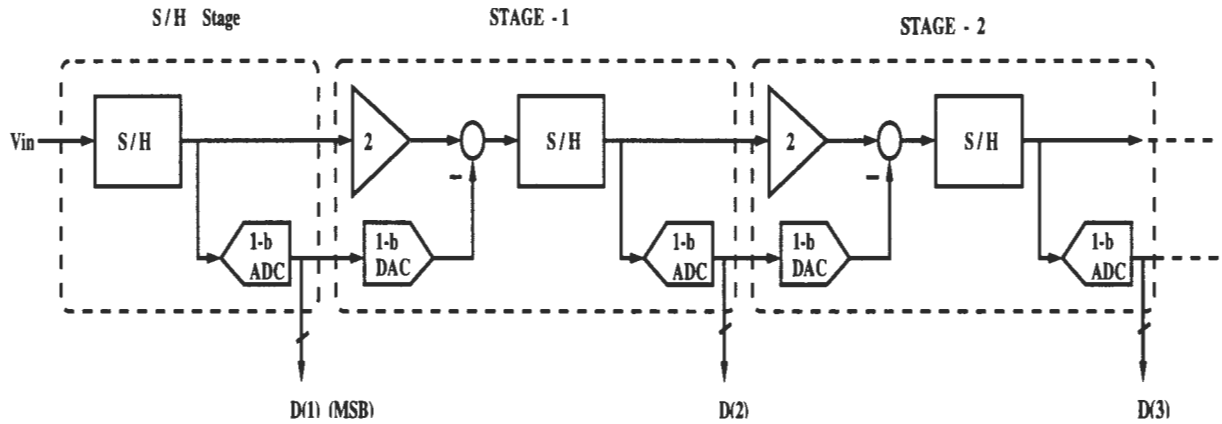

Figure 2.2 Modified Block Diagram of a Pipeline ADC Showing Blocks in Each Stage

switches connected to reference values, V_{refn} (negative reference) and V_{refp} (positive reference). Ideally the resolvable input range of any stage and hence the overall converter is set by the difference between these reference voltages ($V_{refp} - V_{refn}$). The resolvable input range of the A/D converter is defined as the range of inputs that the converter is guaranteed to quantize with no more than $\pm 1/2$ LSB of error [1]. The gain-of-2 amplifier in each pipeline stage is not only mandatory for implementing the pipeline's algorithm but also provides the added benefit of reducing the pipeline stage's offset, settling, noise and gain-of-2 linearity requirements by an amount proportional to the total gain preceding the stage [5].

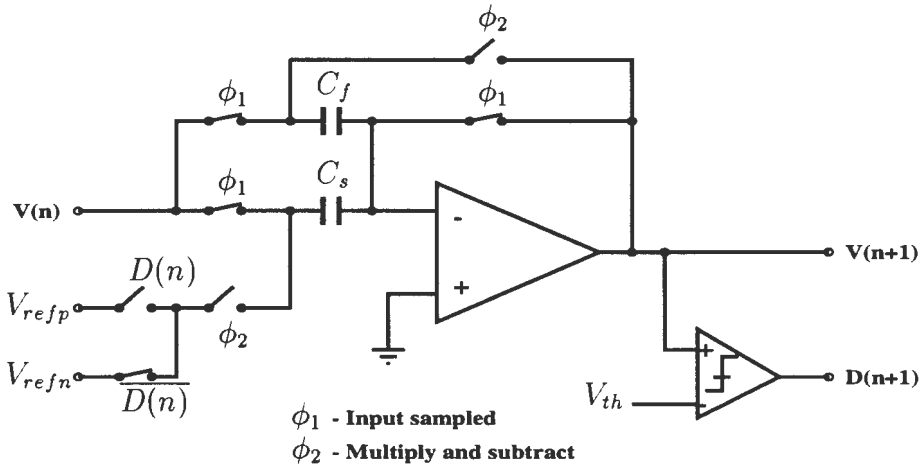

Figure 2.3 Switched-capacitor Implementation of a Single Stage of the Pipeline

The sample and hold, DAC, subtraction, and gain functions in a pipeline stage are readily merged into a single switched-capacitor CMOS circuit block. A single-ended version of the commonly used circuit implementation is shown in Figure 2.3. It consists of two identical capacitors C_s and C_f, an operational amplifier (op-amp), a comparator and switches [8]. The main disadvantage of pipeline ADC is that they require the use of op-amps to realize parasitic-insensitive S/H amplifiers. Although the S/H amplifiers

improve many aspects of the converter performance, the op-amp within the S/H amplifiers limits the speed of the converter [5]. The switched-capacitor operation has two phases, the sample phase and the hold phase. During the sampling phase, the voltage $V(n)$ at the input to the nth stage of the pipeline is sampled onto both C_s and C_f. During the hold phase, the bottom plate of C_f is connected to the output of the op-amp, while the bottom plate of C_s is connected to the reference voltage equal to either V_{refp} or V_{refn}, based upon the result of the previous stage's digital output. During the end of this phase, the comparator compares the output, $V(n+1)$ with the midpoint if the converter's resolvable input voltage range. The nominal comparator threshold voltage V_{th} is therefore,

$$V_{th} = \frac{V_{refp} + V_{refn}}{2} \tag{2.1}$$

and the digital output of the comparator D(n+1) is

$$D(n+1) = 1 \quad if \quad V(n) \geq V_{th} \tag{2.2}$$

$$D(n+1) = 0 \quad if \quad V(n) < V_{th} \tag{2.3}$$

The voltage residue, $V(n+1)$ is given by,

$$V(n+1) = 2V(n) - V_{refp} \quad if \quad D(n) = 1 \tag{2.4}$$

$$V(n+1) = 2V(n) - V_{refn} \quad if \quad D(n) = 0 \tag{2.5}$$

$V(n+1)$ and $D(n+1)$ serve as the inputs to the next pipeline stage, where the same operations are performed. In this fashion, the bits of the digital output are determined in succession, proceeding from the most to least significant bit. Since there will be a delay in the evaluation of the least significant bit, D-flipflops are used to handle the latency.

The ideal transfer function of an individual stage of the pipeline is given by the expression in Equations 2.4 and 2.5, and is plotted in the Figure 2.4.

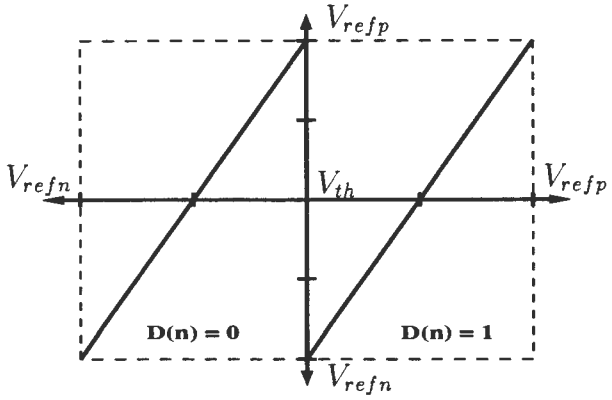

Figure 2.4 Ideal Residue Characteristics for a 1-bit Pipeline Stage

2.2 Errors in 1-bit-per-stage Pipeline ADC

In this section, some error sources affecting typical implementations of pipelined ADCs are discussed. These error sources have historically limited the performance of pipeline ADCs. These error sources can be broadly divided into two categories: noise, which varies from sample to sample, and mismatches, which do not vary from sample to sample [6]. This distinction has an important impact with regards to calibration. Mismatch related errors can be corrected by calibration, while noise related errors cannot be easily corrected by calibration. In general, the major sources of error in pipelined, switched-capacitor ADCs are comparator offset, charge injection from the sampling switches, finite op-amp gain, capacitor mismatch and noise. The effects of these errors except noise can be summed up to be one of Gain error, Comparator offset or DAC error. The effects of each of these on the ADC is investigated.

2.2.1 Gain Error

The first part of the transfer characteristic of the single stage of the ADC (Equations 2.4 and 2.5) is $2V(in)$. The limitation in achieving this is the finite op-amp gain and the mismatch in the value of capacitors. Ideally, the open loop gain of the op-amp has to be

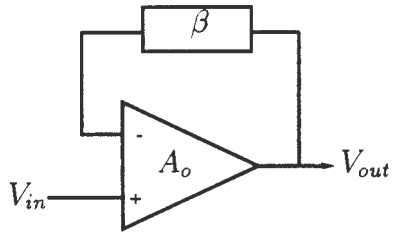

Figure 2.5 Gain Circuit using Op-amp

infinite to get an accurate value in switched-capacitor circuits. The effect of op-amp's finite open loop gain can be understood by Eq. 2.6 and Figure 2.5.

The gain of the this circuit is given by,

$$\frac{V_{out}}{V_{in}} = \frac{A_o}{1 + A_o\beta} = \frac{1}{1/A_o + \beta} \tag{2.6}$$

where A_o is the open loop gain of the op-amp and β is the feedback factor. The gain is usually approximated to $1/\beta$, assuming an infinite open loop gain. Eq. 2.6 can be modified as,

$$\frac{V_{out}}{V_{in}} = [\frac{1}{\beta}][\frac{A_o}{\frac{1}{\beta} + A_o}] \tag{2.7}$$

We can define K as the gain error coefficient that results from finite op-amp gain and given by,

$$K = \frac{A_o}{\frac{1}{\beta} + A_o} \tag{2.8}$$

At this point, three common configurations of Switched-capacitor circuits are studied. In all the cases, the basic operations include sampling the signal on the sampling capacitor(s) and transferring the signal charge onto the feedback capacitor by using an op-amp in the feedback configuration.

In Figure 2.6 the op-amp forces the sampled signal charge on C_s to transfer to C_f as

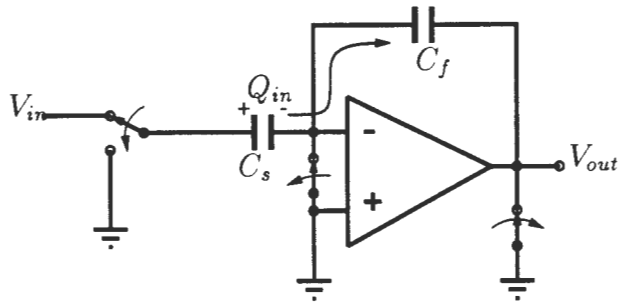

Figure 2.6 Switched Capacitor Circuit with Separate C_s and C_f

indicated by the arrow. The output voltage is given by,

$$V_{out} = \frac{Q_{in}}{C_f} = \frac{C_s \cdot V_{in}}{C_f} = \left(\frac{C_s}{C_f}\right) V_{in} \tag{2.9}$$

In the configuration shown in Figure 2.7, only one capacitor is used for both sampling and holding. This configuration cannot implement the gain function, while it can achieve high speed operation because the feedback factor can be much larger than that of the previous configuration, operating much closer to the unity gain frequency of the amplifier [7]. This configuration is often used as the front-end input S/H circuit.

Figure 2.8 shows another configuration which is a combined version of the configurations in Figure 2.6 and Figure 2.7. In this configuration, the signal is sampled on both C_s and C_f, and the resulting transfer function is,

$$V_{out} = \frac{Q_{in}}{C_f} = \frac{C_f V_{in} + C_s V_{in}}{C_f} = \left(1 + \frac{C_s}{C_f}\right) V_{in} \tag{2.10}$$

In this configuration, C_f is also used as the sampling capacitor in order to improve the feedback factor. The effect of feedback factor on the speed of operation can be understood by the following equation,

$$BW_{closedloop} = \beta \cdot \omega_t \tag{2.11}$$

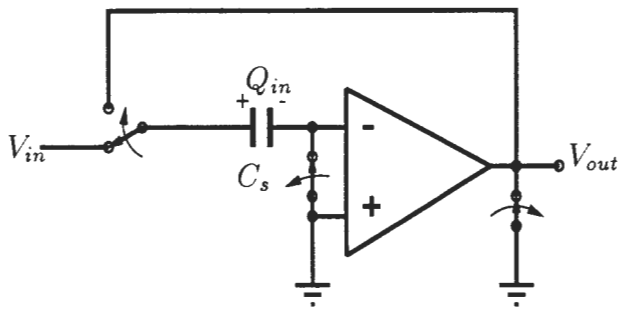

Figure 2.7 Switched Capacitor Circuit with One Capacitor

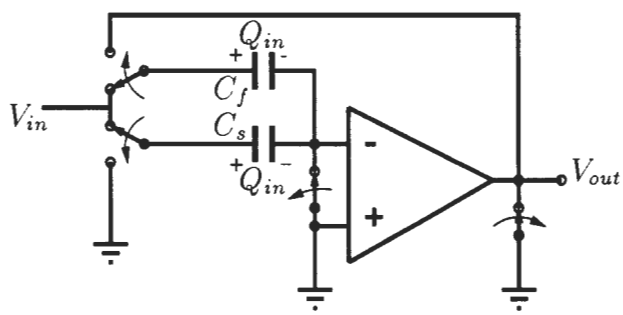

Figure 2.8 Switched Capacitor Circuit with C_f Shared as Sampling Capacitor

At this point, the affect of per-stage resolution on the speed on the ADC can also be considered. Decreasing the per-stage resolution is important if the speed of the switched-capacitor circuit is to be maximized since a small per-stage resolution allows the configuration to have a large feedback factor and a low load capacitance. Note that the op-amp's input capacitance, C_{opamp} was not included in the above discussion. The C_{opamp} will reduce the feedback factor as shown below.

$$\beta = \frac{C_f}{C_s + C_f + C_{opamp}} \tag{2.12}$$

The op-amp's input capacitance will have a similar effect on the other two configurations as well. Ignoring, the op-amp's input capacitance, the gain error coefficient, K can now be written as,

$$K = \frac{A_o}{1 + \frac{C_s}{C_f} + A_o} \tag{2.13}$$

Now, the above factor can be introduced in the transfer function of a single stage of the pipeline. Eq. 2.4 and Eq. 2.5 can be now modified as,

$$V(n+1) = K[(1 + \frac{C_s}{C_f})V(n) - (\frac{C_s}{C_f})V_{refp} \quad if \quad D(n) = 1 \tag{2.14}$$

$$V(n+1) = K[(1 + \frac{C_s}{C_f})V(n) - (\frac{C_s}{C_f})V_{refn} \quad if \quad D(n) = 0 \tag{2.15}$$

The above equation, shows that the gain obtained would be different from the expected gain. It has to be noted that the gain error for the input S/H can be tolerated if the A/D conversion does not require absolute scale. This can be modeled as having a linear gain function in front of the ideal S/H circuit as shown in Figure 2.9 [7].

If the gain is linear, then it does not introduce any error except reducing the signal amplitude by a small portion. Another important factor to consider is the linearity of the op-amp. The negative feedback around the op-amp reduces the distortion by the loop gain factor, $A_o\beta$, to obtain a highly linear transfer characteristic. In an ADC, the

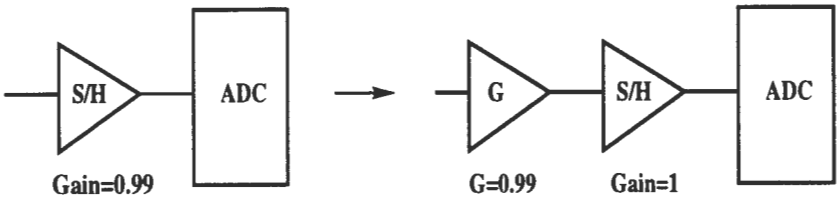

Figure 2.9 Front-end S/H Gain Error [7]

distortion in the S/H will result in a large INL error. For this reason, high resolution ADCs require high op-amp dc open loop gain.

The affect of the gain error in the interstage amplifiers can be understood from the transfer function of each stage. For this purpose, we shall consider the last 4-bit section of the N-bit pipeline and analyze the transfer characteristic. The last 3-bit pipeline section is assumed to be ideal with a resolvable input range between V_{refp} and V_{refn}. Figure 2.11 shows the resulting transfer characteristic when the preceding pipeline stage, Stage $N-4$ is also ideal and has the full resolvable input range.

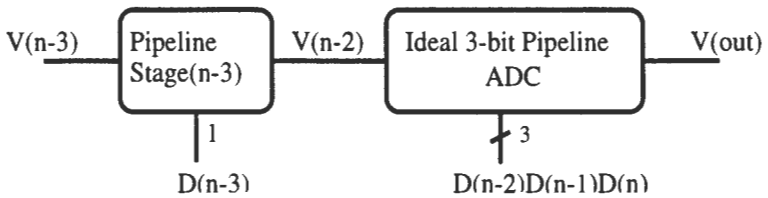

Figure 2.10 Block diagram of the 4-bit Section of a Pipeline

From Eq. 2.14 and Eq. 2.15 it can be seen that the final gain can be either greater than or less than 2, depending upon the values of the gain error coefficient, K and the capacitor values C_s and C_f. Figure 2.12 shows the transfer characteristic of an individual stage of a pipeline, with a gain of <2.

It can be seen that there will be missing codes in this case, since the output range of each stage in the pipeline does not completely access the following stage's full input

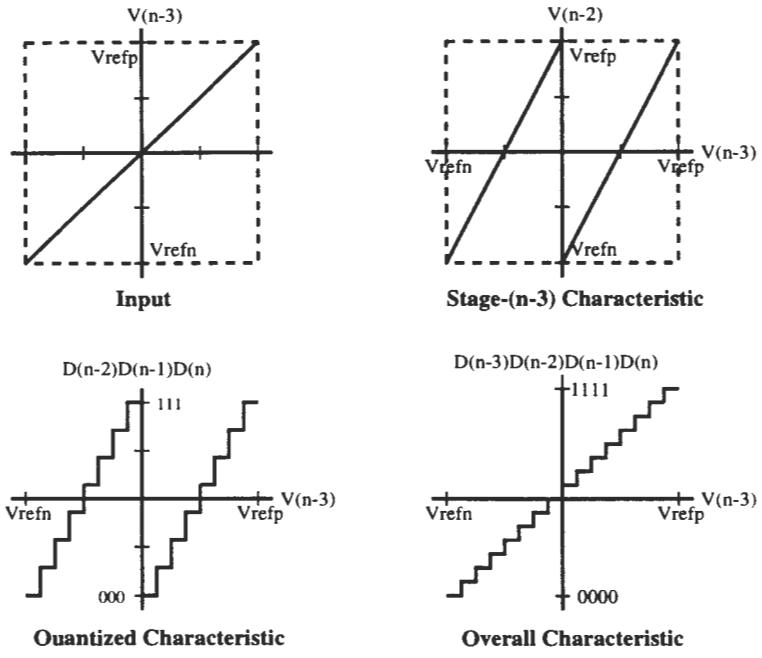

Figure 2.11 Ideal Transfer Characteristics of the 4-bit Pipeline Section[8]

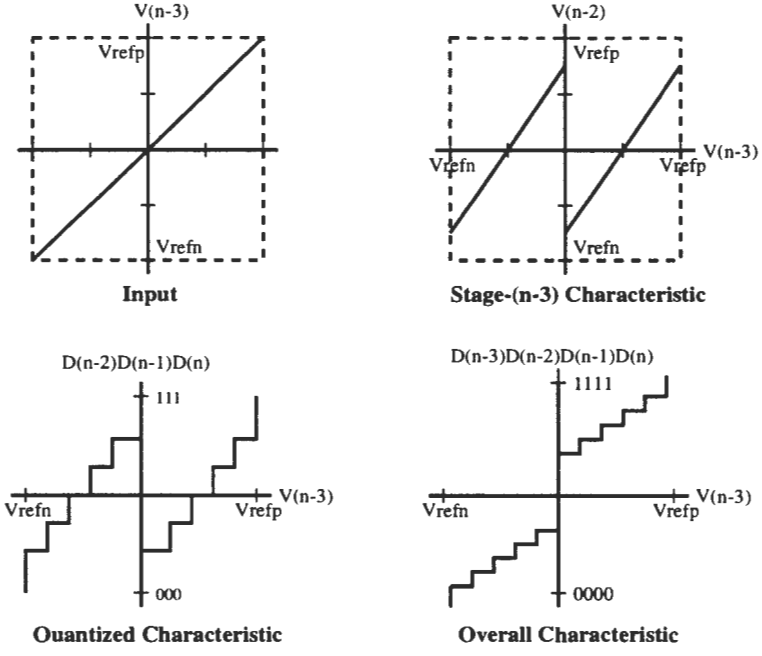

Figure 2.12 Transfer Characteristics of the 4-bit Pipeline Section with Gain < 2

range.D(n-3) changes from a logic 0 to a logic 1 before the analog output of the stage, V(n-2) reaches within an LSB of the 3-bit section of the pipeline's maximum resolvable signal, V_{refp}. The effect of this is that the 3-bit digital output word D(n-2)D(n-1)D(n) will fail to reach all logic 1's before the D(n-3) changes from a logic 0 to a logic 1. The LSB in this case is the LSB of the overall converter multiplied by the total gain preceding the 3-bit section of the pipeline. Similarly, most negative resolvable input voltage of the 3-bit pipeline,V_{refn}, is not reached after D(n-3) changes to logic 1. This causes the digital word D(n-2)D(n-1)D(n) to fail to reach all logic 0's. Both of these can be seen in the overall characteristic as missing codes in the mid-range of the 4-bit digital code. However, missing codes can be eliminated by digital self-calibration as explained by [9].

Figure 2.13 shows the transfer characteristics of the 4-bit pipeline section with a Gain >2. In this case, the output voltage of stage (n-3) exceeds the resolvable input range of the succeeding 3-bit pipeline due to the gain error in stage (n-3). It can be seen in the overall characteristic that for a wide range of analog input near V_th results in no change in the output code. As a result, missing decision levels result in the 4-bit converter's transfer characteristic and hence that of the overall N-bit ADC. Missing decision levels cannot be removed by digital self-calibration technique proposed by [9].

2.2.2 Comparator Offset

Comparator offset is another important source of error in pipeline data converters. This is due to fact that comparator offset results in missing decision levels similar to the gain>2 case discussed in the previous section. Figure 2.14 shows the effect of comparator offset with the comparison threshold being $(V_{th} + \delta)$ instead of V_{th}. It can be seen that Comparator offset can result in both missing decision levels and missing codes. The simplest way to implement a comparator is to use simple regenerative cross-coupled inverters. However, this might exhibit offset voltages as large as 100mV. For this purpose,

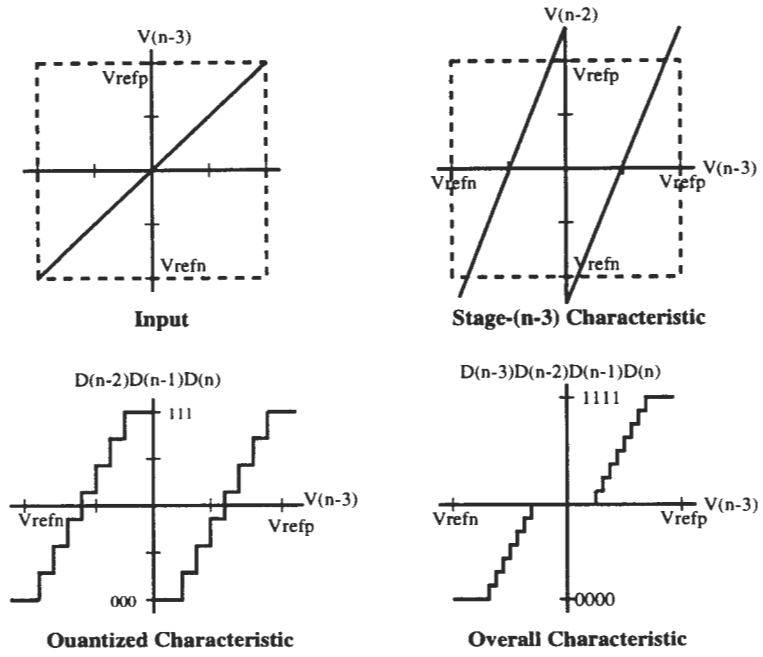

Figure 2.13 Transfer Characteristics of the 4-bit Pipeline Section with Gain > 2

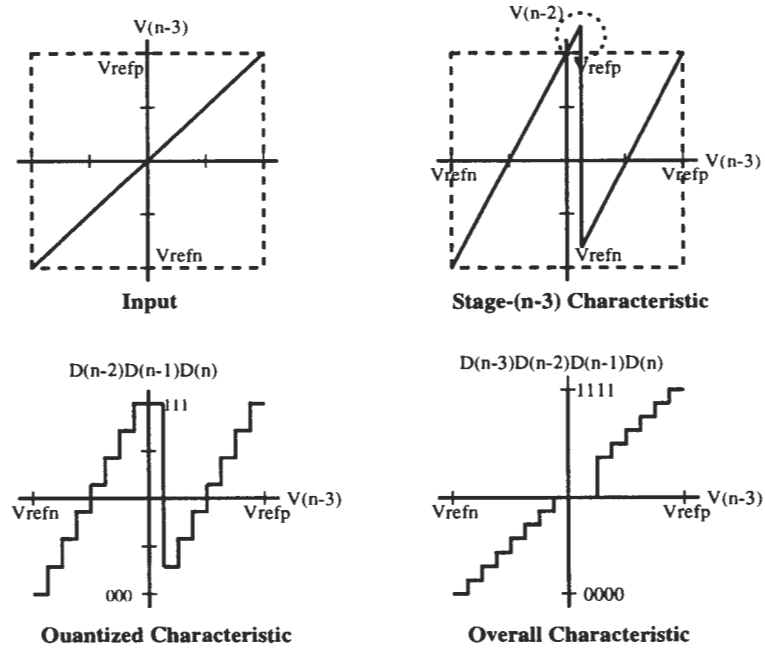

Figure 2.14 Transfer Characteristics with Positive Comparator Offset

the regenerative stage is preceded with preamplifiers. Offset cancelation techniques using multi-stage and switched capacitor configurations can also be used [3].

2.2.3 Charge Injection and Amplifier Offset

The charge injection error and the op-amp offset can be dealt with similarly, since the effect of these errors on the transfer characteristic would be the same. The op-amp offset can be modeled as an output offset voltage, V_{off} and can be introduced in the transfer characteristic as:

$$V(n+1) = 2V(n) - V_{refp} + V_{off} \quad if \quad D(n) = 1 \tag{2.16}$$

$$V(n+1) = 2V(n) - V_{refn} + V_{off} \quad if \quad D(n) = 0 \tag{2.17}$$

Eq. 2.16 and Eq. 2.17 show that the transfer characteristic will shift by the amount of the offset, V_{off}. This is illustrated in Figure 2.15.

Charge injection from the switches can be made input voltage-independent through proper sequencing of the switching and having a differential switched capacitor configuration. Thus, voltage independent charge injection (say, α) can be modeled as an offset at the output, similar to the amplifier output offset voltage. Hence, Eq. 2.16 and Eq. 2.17 hold good here by just replacing V_{off} with α. From the Figure 2.15 it can be seen that amplifier offset and charge injection can cause both missing decision levels and decision codes.

In this chapter, pipeline architecture and typical error sources of a 1-bit per stage pipeline and their effects on the transfer characteristic were analyzed. This leads to the motivation for the digital calibration algorithm that will be explained in Chapter 3.

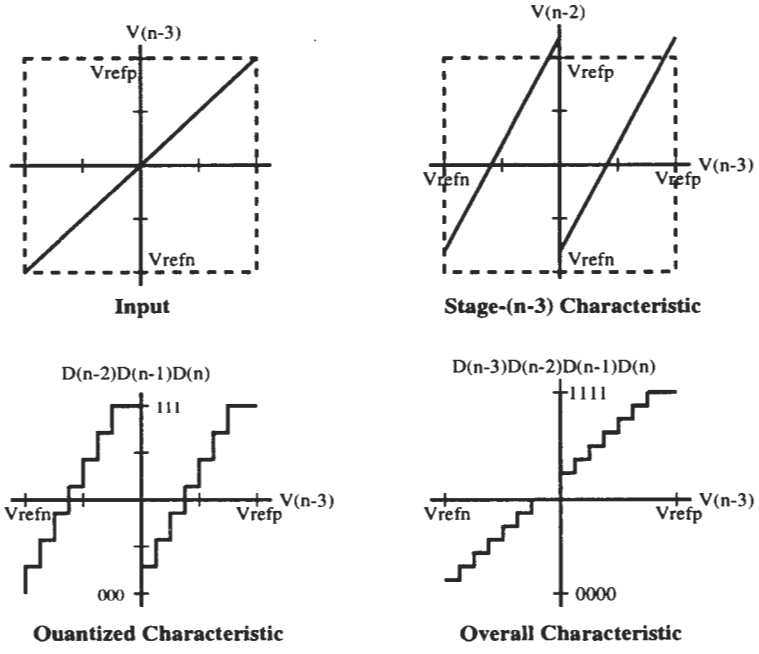

Figure 2.15 Transfer Characteristics with Positive Op-amp Offset

3 DIGITAL SELF-CALIBRATION

3.1 Introduction

To minimize the different errors discussed in Chapter 2, high-precision matching of components is usually required in traditional ADC approaches. This is not compatible with the currently available digital CMOS processes. It is very difficult to get more than 10-bits of linearity without the use of component trimming or some form of calibration. Trimming is a costly option usually done at the foundry using laser beams to cut across the small components to get accurate matching.

Calibration is the process of measuring the deviation of the obtained transfer characteristic of the ADC from the ideal characteristic and making suitable corrections to remove the errors. This is a potentially attractive alternative to trimming which has the disadvantages of its cost, changes due to component aging and deviations in operating conditions from those under which trimming was performed. Considerable effort has recently been devoted to development of calibration techniques that enable realization of high-speed, high-linearity data converters in digital CMOS technologies.

Self-calibration is the process of using the components of the ADC itself to measure the transfer characteristic. This can be done either in the analog domain or the digital domain. Typical analog domain techniques are to measure the capacitor mismatch and comparator offsets in terms of analog values and correct them by adding some analog components, requiring extra analog circuitry. Typical digital domain calibration techniques are to measure the errors in the digital domain and correct the digital code

of the ADC with extra digital circuitry. Digital circuitry is easier to implement in digital CMOS process compared to analog circuitry at the expense of area and power dissipation. Therefore, digital self-calibration was preferred to analog calibration in this work. Currently most calibration techniques fall under three categories:

- Calibration performed at the foundry [10]
- Calibration performed every time the converter is powered up [9][11][12][13]
- Continuous (background) calibration [14][15][8][16].

While power-up calibration techniques are better than costly factory calibration techniques, continuous calibration techniques have the advantage of correcting for errors without interrupting the operation of the converter. Section 3.2 covers a digital self-calibration technique based on a radix < 2 and 1-bit-per-stage conversion algorithm presented in [9]. To achieve more accuracy of the calibration results, [17] proposed an improved digital self-calibration algorithm by applying accuracy bootstrapping technique [18]. This will be discussed in section 3.3. The above are power-up calibration techniques compared to the proposed background calibration technique presented in section 3.4.

3.2 Non-radix 2 Calibration Algorithm

3.2.1 Graphical Explanation of the Algorithm

In Chapter 2, the different sources of errors and their effects on the transfer characteristic of a radix 2 pipeline were discussed. An ideal ADC samples the analog input signal in equal time steps. Provision of equal decision level spacing in an ADC is one of the most difficult tasks for a high-accuracy, high-speed ADC. Accuracy limitations of component values, charge injection and offsets can contribute to missing decision levels,

as discussed and illustrated in Chapter 2. Missing decision levels reflect analog circuit imperfections. Decision levels cannot be created by digital techniques alone [9]. When the output of any stage exceeds the reference boundary, missing decision levels occur. On the other hand, when the output extrema forms a gap to the reference boundary, missing codes happen and it can be eliminated by digital calibration.

In Chapter 2 it was seen that for a gain < 2 case, the residue characteristics showed missing decision codes and no missing decision levels. This was the motivation in developing a non-radix 2 calibration algorithm in [9]. The digital self-calibration presented in [9] uses a non-radix 2 pipeline ADC and removes the missing codes by digital self-calibration. The calibration tries to linearize the ADC characteristics at the cost of more stages.

First, the radix 2 case with no errors is discussed to understand how the output digital code is actually obtained from the residue characteristics. As shown in Figure 3.1 the Stage (n-3) characteristic has two linear parts : (a) when D(n-3)=0 and (b) when D(n-3)=1. The overall transfer characteristic is linearized by shifting the second part of the characteristic by the required amount as illustrated in the figure. The transfer function can be formalized for this 4-bit case by Eq. 3.1 and Eq. 3.2.

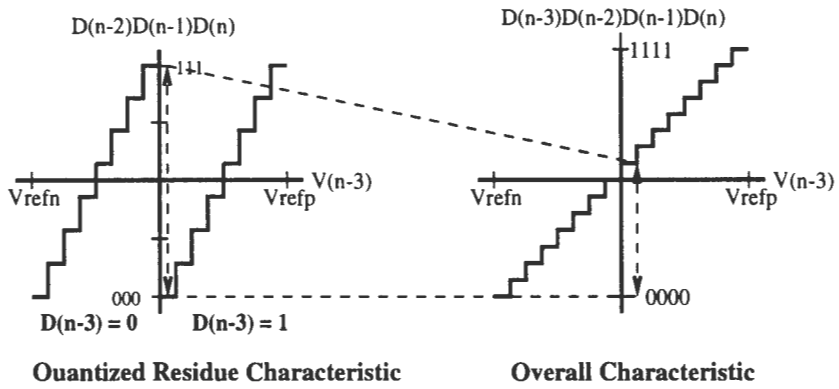

Figure 3.1 Illustration of Digital Code Derivation in Radix 2 Case

$$Y = \quad X \qquad \text{if} \quad \text{D(n-3)=0} \tag{3.1}$$

$$Y = \quad X + 8 \quad \text{if} \quad \text{D(n-3)=1} \tag{3.2}$$

The '8' in Eq.3.2 comes from the difference in the digital outputs for the input of $V_{th} = \frac{V_{refn}+V_{refp}}{2}$ and with D(n-3)=0 and D(n-3)=1. That is, the digital output for the input V_{th} and D(n-3) =0 is 111('7') and the digital output for the input V_{th} and D(n-3) =1 is 000('0'). Using the same notation as [9], the digital output code for input V_{th} and Din = 0 is S_1 (Din is D(n-3) in this case) and the digital output code for input V_{th} and Din = 1 is S_2. Thus, this can be used to generalize Equations 3.1 and 3.2.

$$Y = \quad X \qquad \text{if} \quad \text{D(n-3)=0} \tag{3.3}$$

$$Y = \quad X + (S_1 - S_2) \quad \text{if} \quad \text{D(n-3)=1} \tag{3.4}$$

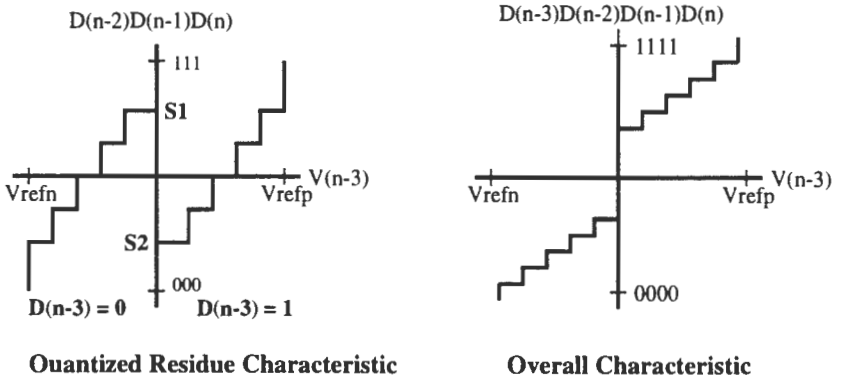

Figure 3.2 Illustration of Digital Code Derivation in Non-radix 2 Case

It is important to note that the above equations hold good for even radix < 2 ADC, the only difference being S_1 and S_2 in this case are different from the radix 2 ADC. Figure 3.2 illustrates S_1 and S_2 for radix < 2 ADC. It can be seen that by shifting the second part of the characteristic by the difference between S_1 and S_2, the overall transfer characteristic would become linear.

Eq.3.3 and Eq.3.4 form the digital self-calibration algorithm proposed in [9]. Assuming that the pipeline has a total of $(n + K)$ stages, the algorithm needs the last K stages of the pipeline to measure the S_1 and S_2 of the nth stage. After linearizing the characteristic, the algorithm continues to measure the S_1 and S_2 of the $(n-1)$th stage using the stages ahead of it (which has a linear characteristic now) and so on until the 1st stage(MSB). The total number of decision levels that can be accessed by a radix 2 pipeline with N stages is 2^N. The actual number of decision levels accessible will always be less than 2^N for a radix < 2 pipeline ADC. Hence, to access the same number of decision levels, more stages are required. A 15-bit 1-Msamples/s digitally self-calibrated pipelined ADC based on the above calibration algorithm was demonstrated [9]. Non-radix 2 gain was set to 1.93, K to 6 and a total of 17 stages. Stages 1 through 11 were implemented each with a gain of 1.93 and stages 12 through 17 each with a gain of 2. The block diagram of [9] is shown in Figure 3.3.

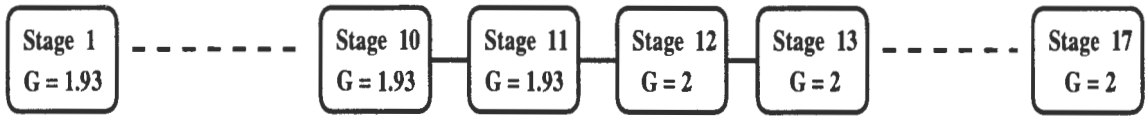

Figure 3.3 Block Diagram of the Prototype Implemented by Karanicolas [9]

3.2.2 Determination of Calibration Constants S_1 and S_2

The measurement of the calibration constants S_1 and S_2 of a stage is done by operating the pipeline section ahead of this stage with specific inputs forced at the input of the section. In order to obtain S_1 for a particular stage, the analog input is grounded and the input bit is forced to be '0' and the residue from the stage is quantized using the successive pipeline stages. In order to obtain S_2 for a particular stage, the analog input is grounded and the input bit is forced to be '1' and the residue from the stage is

quantized using the successive pipeline stages. The S_1 and S_2 are determined during the *calibration mode* for all the stages and stored in a digital memory. Once determined they are used during the *run mode*. Figure 3.4 shows the determination of the calibration constants, $S_1(9)$ and $S_2(9)$ for the 9th stage. Note that $S(10)$ and $S(11)$ have already been determined. A detailed explanation of this can be referred from [9].

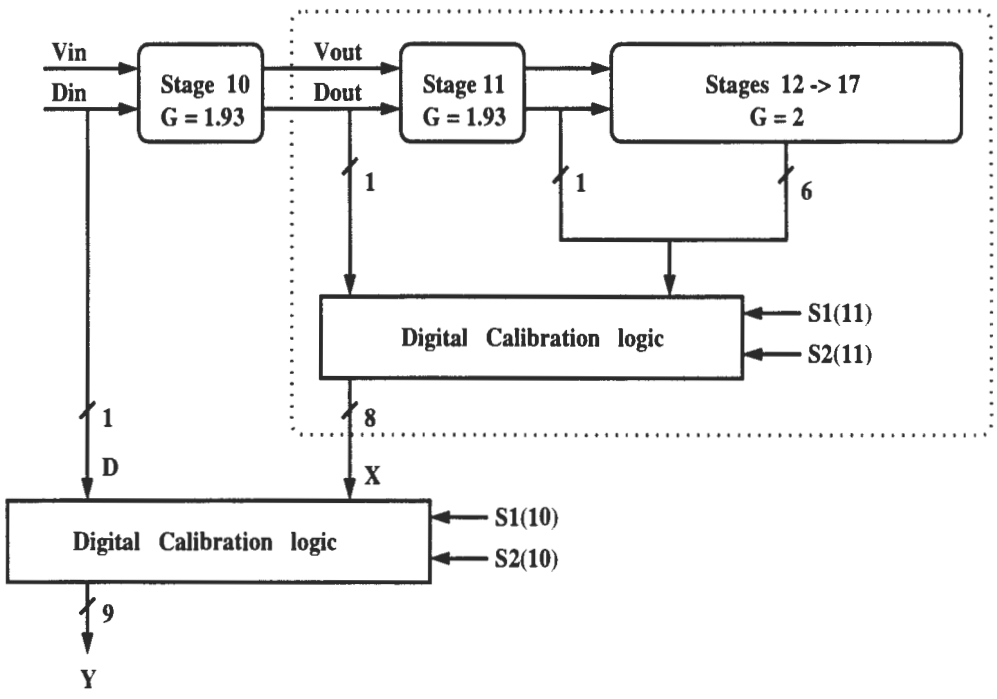

Figure 3.4 Block diagram of Digital Calibration of Higher Level Stages

3.2.3 Comparator Offset Tolerance

As discussed in Chapter 2, comparator offset of a traditional pipeline ADC is a primary limitation to accuracy. The digital calibration of [9] is tolerant to comparator offset. Figure 3.5 shows the residue plot of a stage with comparator offset from the previous stage.

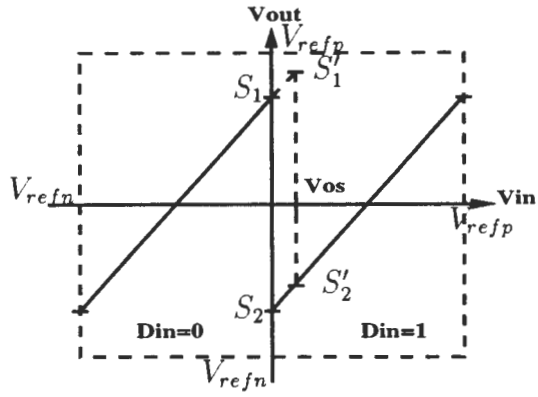

Figure 3.5 Residue Characteristics of a Stage with a Comparator Offset=Vos

The key feature of the residue plot is the equation:

$$S_1' - S_2' = S_1 - S_2 \tag{3.5}$$

This means that the difference in S_1-S_2 does not change so that the calibrated residue output is unchanged when there is a comparator offset [9]. But, this remains true only as long as the effective comparator offset maintains the residue within the reference boundary box.

3.3 Accuracy Bootstrapped Self-calibration Algorithm for a Non-radix 2 Pipeline

In the digital self-calibration algorithm discussed above, when a stage is being calibrated, only those stages that are ahead of this stage are being used to measure the two calibration constants, S_1 and S_2. For example the S_1 and S_2 for stage 11 has only 6-bit accuracy since only stages 12 through 17 are used for the measurement. Also, stages 12 through 17 are never calibrated, which assumes that the converter has at least 6-bit linearity. These are the major drawbacks of this calibration scheme. To make the

calibration algorithm more accurate, [17] proposes a digital calibration algorithm based upon the accuracy bootstrapping algorithm [18] that uses all stages of the pipeline cyclically to measure S_1 and S_2 for each stage. The results were shown to be better in this case, because of more precision of S_1 and S_2 for all the stages. The block diagram for this is shown in Figure 3.6.

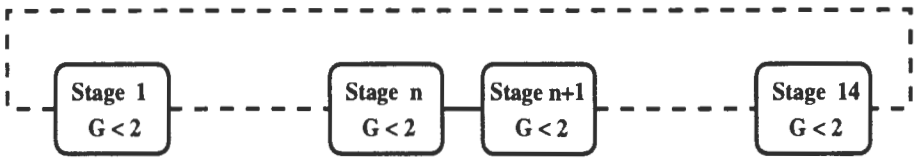

Figure 3.6 Block Diagram of the Accuracy Bootstrapped Algorithm for a 14-stage ADC

For a 14-stage ADC, the last stage (stage 14) is first calibrated. S_1 and S_2 for stage 14 are measured using stages 1 through 14. Then, stage 13 is calibrated using stage 14 and 1 through 13. The calibration procedure continues until the first stage is calibrated. By this way, the calibration constants for all the stages have the same accuracy and all stages are being calibrated.

3.4 Background Calibration Technique

3.4.1 Need and Motivation

The use of power-up and factory calibration techniques are limited to the extent that they cannot correct for errors without interrupting the converter's operation. Background (continuous) calibration addresses this limitation and enables a converter to function in the presence of environmental fluctuations and supply variations by constantly correcting for errors without disturbing the data flow in the converter. Calibration schemes discussed in sections 3.2 and 3.3 are power-up calibration techniques. This

work introduces a method for continuously calibrating pipelined data converters using the self-calibration algorithms that have been discussed in sections 3.2 and 3.3. The key advantage of the proposed technique is that the calibration is done in the digital domain and requires no extra clock cycles. Though this work has been discussed for 1-bit-per-stage architectures, it could be extended to multi-bit-per-stage architectures also.

As discussed in sections 3.2 and 3.3, the calibration of the ADC only requires two values of each stage, S_1 and S_2 to be stored in a digital memory. If these are measured continuously without interrupting the operation of the converter and written to the digital memory, updating the values for the respective stages, calibration can be done in *background.* But, this is not a simple task since the rest of the stages of the pipeline are used to measure the calibration constants for each stage. This work presents a technique to measure the calibration constants of each stage without interrupting the operation of the converter. This can be done by having an extra stage in the pipeline. Intuitively, the extra stage of the pipeline will be measuring the value of S_1 or S_2 of a stage in the pipeline while the rest of the stages will be converting the analog input. This is not very trivial because alternate stages of the pipeline operate in different clock phases and the extra stage will have to be logically shifted through the different stages of the pipeline. Two adjacent stages operate in different clock phases because, if stage 1 samples the input during clock phase ϕ_1 and gives the residue (output) during ϕ_2, stage 2 has to sample the input (stage 1's output) during ϕ_2 and give the output during ϕ_1.

3.4.2 Tabular Representation of a Pipeline ADC

The operation of a typical pipeline ADC can be represented in a tabular form for easier understanding on how the residues are handled by the different stages. A 4-stage ADC operation is represented in Table 3.1. The symbols used in the table are as follows:

Sx represents the xth input sample (e.g. S2 - is the 2nd input sample)

Sx.y represents yth-bit of the 'x'th sample being sampled (e.g. S2.1, S2.2, S2.3, S2.4 - are the 4-bits of the 2nd input sample)

Rx.y represents that the residue(output) of the yth-bit of the 'x'th sample (e.g. R2.1, R2.2, R2.3, R2.4 - are the Residues of the 2nd input sample)

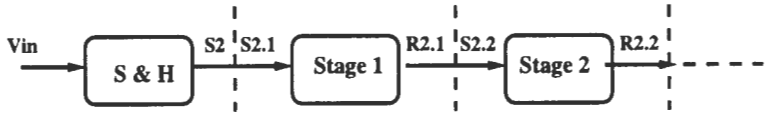

Figure 3.7 Illustration of Symbols Used in the Table

Table 3.1 Tabular Representation of the Operation of a 4-stage Pipeline ADC

Sample		Stage 1		Stage 2		Stage 3		Stage 4	
ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_2	ϕ_1	ϕ_1	ϕ_2	ϕ_2	ϕ_1
S1		**S1.1**							
			R1.1	S1.2					
S2		**S2.1**			R1.2	S1.3			
			R2.1	S2.2			R1.3	S1.4	
S3		**S3.1**			R2.2	S2.3			R1.4
			R3.1	S3.2			R2.3	S2.4	
S4		**S4.1**			R3.2	S3.3			R2.4
			R4.1	S4.2			R3.3	S3.4	
S5		**S5.1**			R4.2	S4.3			R3.4
			R5.1	S5.2			R4.3	S4.4	

S1, S2 ,etc., are the input samples at the output of the front-end sample and hold. The residues of each stage are used by the corresponding comparators to determine the digital bits. Stage 4 forms the LSB stage and the sample and hold corresponds to the MSB. It can be seen that always Stage 1 samples the first sample, Stage 2 samples the

output of Stage 1, Stage 3 samples the output of Stage 2 and so on. Hence, 4 stages contribute to 5-bits of digital output.

3.4.3 Tabular Representation of the Background Calibration Technique

Background calibration as mentioned can be performed by having an extra stage in the pipeline. For example, in the 14-stage case, with background calibration there will be only 14 valid output bits and 1-bit for the calibration data instead of 15 valid output bits. If the pipeline takes a cyclic configuration as shown in Figure 3.8 and all stages are identical then the input (output of the S/H) can be connected to any stage getting the digital output correspondingly. For example, when Vsamp is given to Stage 1, Stage 1's output forms the 2nd bit (Vsamp corresponds to the 1st bit) and Stage 14 forms the LSB, and when Vsamp is given to Stage (n+1) , output of Stage (n+1) forms the 2nd output bit and Stage (n) forms the LSB. This configuration is used to achieve background calibration. When the ADC is not being calibrated, all the 14 outputs are valid data bits but when the ADC is being calibrated only 13 outputs are valid data bits and one is used for calibration.

The output from the S/H has to be shifted through all the stages to achieve calibration of all the stages. Since alternates stages in the pipeline operate on different phases, the input can only be shifted through either all the odd stages or all the even stages. To make switching of the input through all the stages possible, the output of the S/H has to be valid on both the clock phases ϕ_1 and ϕ_2. The simplest way to achieve this is to have two S/H's with one following the other. The calibration measures the S1 for all the stages and then goes on to measure S2 for all the stages. The background calibration can be understood with the help of Table 3.2 where S1 is being measured for all the stages without interrupting the conversion of the input signal. The symbols used in the table are as follows:

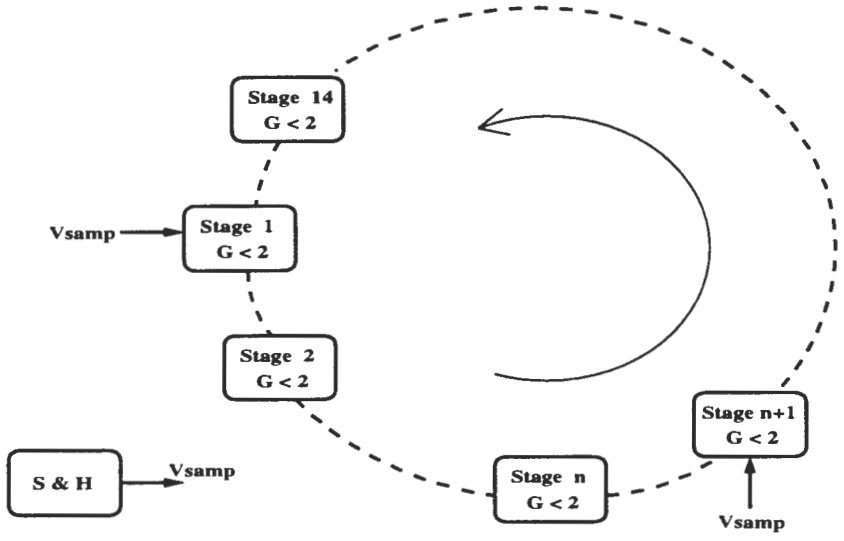

Figure 3.8 Cyclic Configuration of the Pipeline (S/H not shown)

Sx represents the xth input sample valid on ϕ_1 (e.g. S2 - is the 2nd input sample)

Sxd represents the delayed xth input sample valid on ϕ_2 (e.g. S2d - is the delayed 2nd input sample)

Sx.y yth-bit of the 'x'th sample being sampled (e.g. S2.1, S2.2, S2.3, S2.4 - are the 4-bits of the 2nd input sample)

Rx.y represents that the residue(output) of the yth-bit of the 'x'th sample (R2.1, R2.2, R2.3, R2.4 - are the Residues of the 2nd input sample)

Cx.y yth-bit input of the calibration value (S_1) for stage 'x' (e.g. C2.1, C2.2, C2.3 - are the Calibration values with input = 0 and Din = 0 for stage 2)

Ox.y yth-bit of the output of the calibration for stage 'x' (e.g. O2.1, O2.2, O2.3 - are the outputs of the calibration values corresponding to S_1 for stage 2)

Note that all Cx.1's are V_{th} (Comparator threshold voltage). Figure 3.9 shows the illustration for calibration of Stage 1 to illustrate the above symbols.

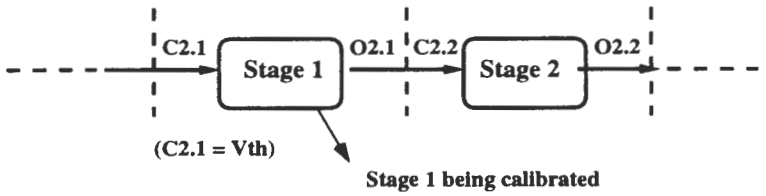

Figure 3.9 Illustration of the Calibration Symbols Used in the Table

To start with the calibration, since the last stage (stage 4) is the extra stage it is calibrated first (C4.1). Now, since stage 1 is required to track the calibration output, O4.1, it cannot be used to track the input S3. However, stage 4 is now used to track the input sample S3d (because stage 4 tracks on ϕ_2). And for sample S4 we see that stage 3 is free (extra stage) and hence it tracks the input sample S4 and S5. During which stage 2 starts calibrating. Thus we see that all even stages are calibrated and then stage 1 is calibrated and then all odd stages are calibrated. From the table it can be seen that all stages are being calibrated without missing an input sample. This follows for any pipeline ADC with even number of stages. The 'even' criteria stems from the fact that the pipeline cannot be connected in the cyclic form without even number of stages (since alternate stages have to operate on different clock phases). Once the S_1's of all stages have been measured, S_2's of all stages can be measured in the similar way. This can be stored in the memory and calibration similar to [9] and [17] can be used for digital calibration. Since the values are being updated constantly without interrupting the actual conversion, this is an effective background calibration technique. It can be seen from the table that 12 clock cycles are needed to measure the S_1's for all the 4 stages. Hence, to measure both S_1's and S_2's for all the stages a total of 24 clock cycles are required. In general, for an N-bit converter, $2 * 2^N$ cycles are required to calibrate all the stages.

Table 3.2 Tabular Representation of the Calibration of a 4-stage Pipeline ADC

Sample		Stage 1		Stage 2		Stage 3		Stage 4	
ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_2	ϕ_1	ϕ_1	ϕ_2	ϕ_2	ϕ_1
S1		**S1.1**							
	S1d		R1.1	S1.2					
S2		**S2.1**			R1.2	S1.3			
	S2d		R2.1	S2.2			R1.3	*C4.1*	
S3		*C4.2*			R2.2	S2.3			*O4.1*
	S3d		*O4.2*	*C4.3*			R2.3	**S3.1d**	
S4		S3.2			*O4.3*	**S4.1**			R3.1
	S4d		R3.2	S3.3			R4.1	S4.2	
S5		S4.3			R3.3	**S5.1**			R4.2
	S5d		R4.3	*C2.1*			R5.1	S5.2	
S6		S5.3			*O2.1*	*C2.2*			R5.2
	S6d		R5.3	**S6.1d**			*O2.2*	*C2.3*	
S7		**S7.1**			R6.1	S6.2			*O2.3*
	S7d		R7.1	S7.2			R6.2	S6.3	
S8		*C1.1*			R7.2	S7.3			R6.3
	S8d		*O1.1*	*C1.2*			R7.3	**S8.1d**	
S9		S8.2			*O1.2*	*C1.3*			R8.1
	S9d		R8.2	S8.3			*O1.3*	**S9.1d**	
S10		S9.2			R8.3	**S10.1**			R9.1
	S10d		R9.2	S9.3			R10.1	S10.2	
S11		S10.3			R9.3	*C3.1*			R10.2
	S11d		R10.3	**S11.1d**			*O3.1*	*C3.2*	
S12		*C3.3*			R11.1	S11.2			*O3.2*
	S12d		*O3.3*	**S12.1d**			R11.2	S11.3	
S13		**S13.1**			R12.1	S12.2			R11.3
	S13d		R13.1	S13.2			R12.2	S12.3	

4 PROTOTYPE IMPLEMENTATION

A 12-bit, 25MHz pipeline ADC prototype was built in 0.35μm CMOS technology to demonstrate the proposed background calibration technique. This chapter discusses the implementation of the prototype and other key aspects in the design of pipeline data converters.

4.1 Sample-and-Hold (S/H)

The sample and hold is one of the basic and most important switched-capacitor building block. Since, the S/H is the first block in the ADC, the accuracy and speed of the entire ADC cannot exceed that of the S/H. Hence, a lot of care is taken in designing and understanding the various aspects of the S/H. The simplest way of implementing a S/H is first introduced to understand the need of advanced structures.

4.1.1 The Simplest S/H

The simplest S/H consists of a MOS switch and a capacitor as shown in Figure 4.1. When the switch is ON, the input voltage is stored on the capacitor and when the switch is OFF, the voltage on the capacitor is held. However, there are several practical limitations to this circuit. The finite bandwidth of the circuit will limit the output from tracking the input instantaneously. Therefore, a small acquisition time must be allocated for this step response. There will be a tracking error due to the attenuation of the sampling network.

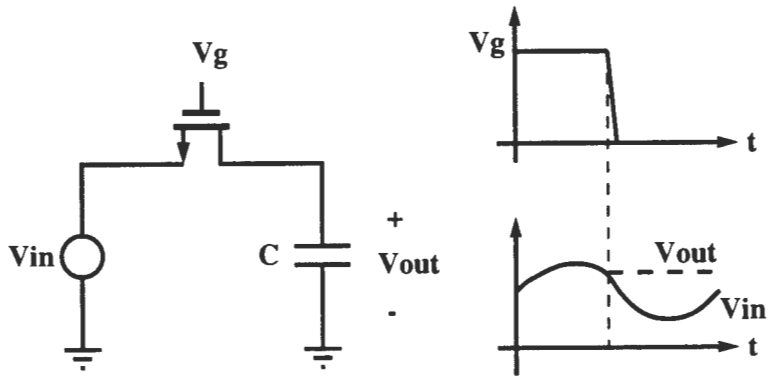

Figure 4.1 Simple MOS Sample-and-Hold Circuit

The most important limitation of this circuit is the dependence of the on-conductance on the input signal.

$$g_{ds} = \mu C_{ox} \frac{W}{L}(V_g - V_{in} - V_t) \tag{4.1}$$

When the switch turns OFF, clock feed-through and charge injection introduce error in the output. Clock feed-through occurs because of the parasitic capacitances, C_{gs} and C_{gd} coupling the gate voltage to the output. Since this error is signal-independent, it only introduces an offset. To the first order this can be eliminated by using a differential configuration. Charge injection is the charge in the channel that is dumped into the source and drain when the switch turns OFF. Since the channel charge is signal dependent (by Eq.4.2), charge injection causes a signal dependent error.

$$Q_{ch} = WLC_{ox}(V_g - V_{in} - V_t) \tag{4.2}$$

This circuit is also sensitive to parasitic capacitance. Any parasitic capacitance at the output changes the amount of signal charge sampled. Bottom-plate sampling can greatly help reduce these errors.

4.1.2 Bottom-plate Sampling

A technique called Bottom-plate sampling is used to remove the errors in the simple S/H circuit at least to the first order. Figure 4.2 shows the bottom-plate sampling configuration. Clock ϕ' falls just before ϕ. When both clocks are high, the bottom plate of the capacitor, C is connected to ground through transistor M2. The output, V_{out} tracks the input, V_{in} during this time. When ϕ' falls from high to low, the charge on the capacitor ($q = CV_{in}$) is trapped and conserved. When ϕ falls from high to low, transistor M1 is turned OFF and the voltage is held on the capacitor.

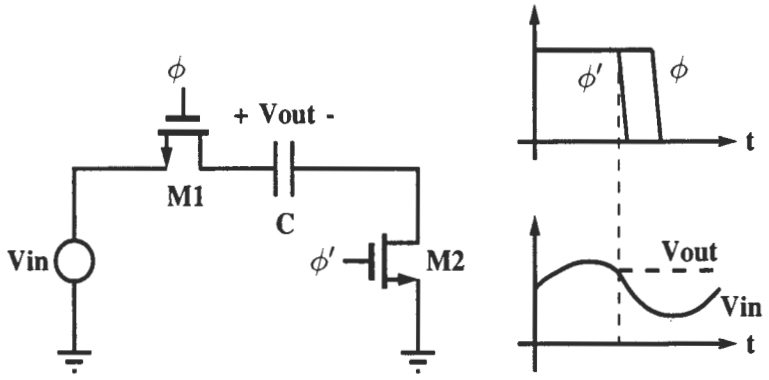

Figure 4.2 Bottom-plate Sample-and-Hold Circuit

When M2 turns OFF, the voltage at the bottom plate of the capacitor changes because of clock-feed-through and charge injection. However, both of these are signal independent because both source and drain of the transistor are at ground potential and not connected to input. The charge injection from the transistor M1 does not alter the charge stored on capacitor, C due to the principle of charge conservation. Typical differential configuration using an op-amp is shown in Figure 4.3. Modifications to these configurations were discussed in Chapter 2.

Although the op-amp greatly improves the performance of S/H circuit, it adds substantial complexity to the design and introduces errors that were discussed in Chapter

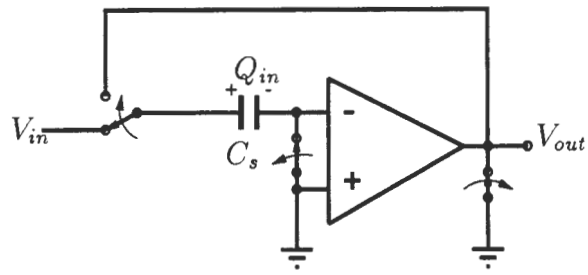

Figure 4.3 S/H Configuration Using an Op-amp

2. The finite DC gain of the op-amp introduces a fixed-gain error. Any offset in the op-amp will appear directly at the output in this configuration. The finite bandwidth of the op-amp limits the clock frequency of the S/H. This configuration was used to realize in S/H in the prototype built.

4.2 Multiplying Digital-to-Analog converter

Figure 4.4 shows the schematic of the fully differential Multiplying Digital-to-Analog converter (MDAC) [19]. The circuit uses 2 primary non-overlapping clocks ϕ_1 and ϕ_2 and also ϕ_1+ and ϕ_1- for bottom-plate sampling. ϕ_1- falls just before ϕ_1 and ϕ_1+ falls just after ϕ_1.

The operation of the circuit is as follows:

(1) When ϕ_1, ϕ_1- and ϕ_1+ are high, switches M1,..,M9 are ON with both the op-amp inputs and the outputs connected to the common-mode voltage. The '0.9C' and 'C' capacitors track the input during this time.

(2) When ϕ_1- goes low first, the inputs of the op-amp are disconnected from the common-mode voltage, but remain connected to each other through M1. Switches M2 and M3 are chosen to be much smaller than M1 so that the charge injection error is small.

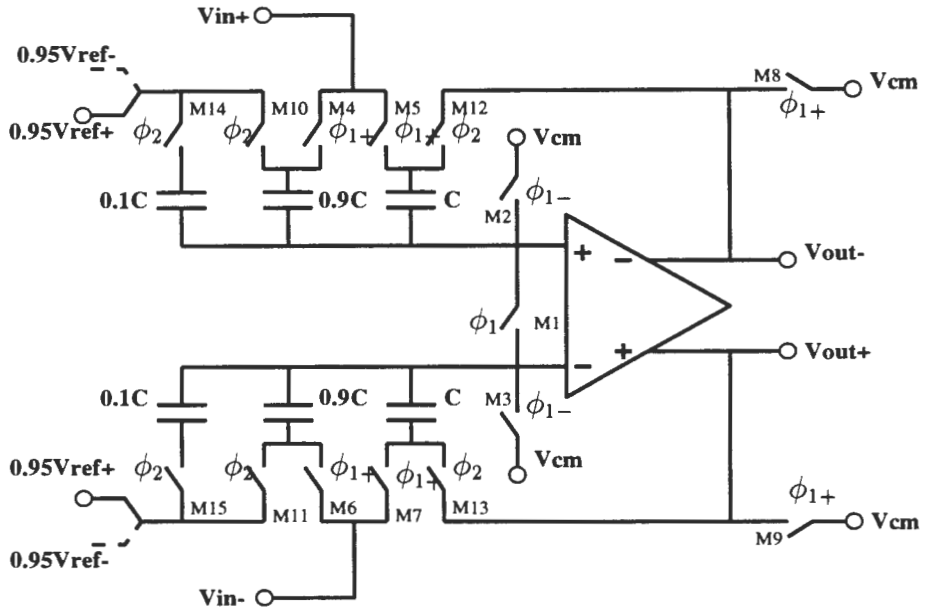

Figure 4.4 Fully Differential Multiplying Digital-to-Analog Converter

(3) Then ϕ_1 goes low and M1 is turned OFF. At this time, the capacitors are charged with the input voltage and this charge is conserved. The charge injection from switch M1 is signal independent as explained before. This is further removed here by the differential configuration, assuming the charge from M1 is evenly distributed into the 2 input nodes.

(4) Then ϕ_1+ goes low and M4, M5, M6, M7, M8 and M9 are turned OFF. The charge injection from these switches does not affect the total charge on the sampling capacitors because of charge conservation principle (bottom-plate sampling). M4, M5, M6 and M7 are chosen to be large to reduce the effects of non-linear resistance and impedance mismatch. During ϕ_1 neglecting the op-amp offset the charge on the capacitors is,

$$Q_1 = V_{in}(0.9C + C) = 1.9V_{in}C \tag{4.3}$$

(5) During ϕ_2 the integrating capacitor (C) is connected to the op-amp output and the sampling capacitor (0.9C) in addition to the '0.1C' capacitors are connected to either

V_{ref+} or V_{ref-} depending upon the digital output of the previous stage. The total charge during this phase is,

$$Q_2 = V_{out}C \pm V_{ref}(0.09C + 0.1C) = V_{out}C \pm V_{ref}C \tag{4.4}$$

By principle of charge conservation, the charge is the same in both clock phases. By equating the two charges, $Q_1 = Q_2$, the transfer function of the MDAC is obtained as,

$$V_{out} = 1.9V_{in} \pm V_{ref} \tag{4.5}$$

The resulting output consists of two parts - one arising from the feedforward of the integrating capacitors and the other from the charge transfer from the sampling to the integrating capacitors. Since only the second part is dependent on the ratios of the capacitors, the feedforward technique reduces the effect of the capacitor mismatch on the interstage gain. This is important because the accuracy of the interstage gain of 2 determines the linearity of the ADC.

Besides feedforward, there are two other motivations for sharing the integrating capacitors (used also for sampling the input during the sampling mode). Since the feedback factor effects the speed of operation as given by,

$$BandWidth_{closedloop} = \beta \cdot \omega_t \tag{4.6}$$

And $\beta = \frac{C_f}{C_s+C_f} = 1/2$ in this case. By this the feedback factor is increased and hence the speed of the circuit. This was already discussed in Chapter 2.

Secondly, the sampling capacitor size is reduced by about 50% which results in considerable die-area saving considering the total number of stages. However, the size of the capacitors should be decided carefully taking $\frac{KT}{C}$ noise into consideration. For this $\frac{KT}{C}$ value should be calculated and it should be at least less than 0.1LSB.

4.3 Deriving the Op-amp Specifications

The first step in the design of ADC is to derive the op-amp specifications from the given ADC requirements. The following sections try to quantize the op-amp specifications from the ADC requirements. The prototype was targeted at 25 Msamples/sec and 12-bit accuracy.

4.3.1 DC Gain

As discussed in Chapter 2, the fixed open-loop DC gain of the op-amp gives a fixed gain error in the output. The DC gain should be such that this error is much less than the 1/2LSB. The block diagram of the switched capacitor circuit is given by Figure 4.5.

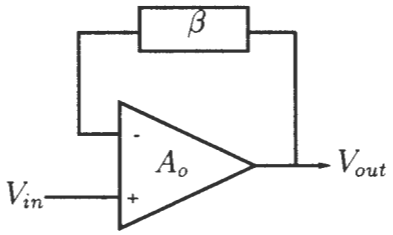

Figure 4.5 Gain Circuit Using an Op-amp

The transfer function of Figure 4.5 is given by,

$$\frac{V_{out}}{V_{in}} = \frac{A_o}{1 + A_o\beta} \tag{4.7}$$

Now, because of the fixed DC gain, the closed loop gain will be different from $\frac{1}{\beta}$. The relative error should be much less than $\frac{1}{2}$LSB. The relative error is given by,

$$Error = \frac{\frac{A_o}{1+A_o\beta} - 2}{2} < \frac{V_{ref}}{2^{12}} \tag{4.8}$$

Solving the equation for A_o with β=1/2 (since the same op-amp is used for the Gain of 2 block) the open-loop DC gain requirement of the op-amp can be obtained.

4.3.2 Bandwidth

Since the bandwidth of the op-amp limits the speed of operation of the ADC, this is an important specification of the op-amp. With the assumption that the op-amp is compensated such that the higher-order poles play a minor role in settling,

$$A(s) = \frac{\omega_{ta}}{s} \tag{4.9}$$

$$A_f(s) = \frac{A(s)}{1+\beta A(s)} \tag{4.10}$$

$$A_f(s) = \frac{1}{\beta}[\frac{1}{1+\frac{s}{\omega_{ta}\beta}}] \tag{4.11}$$

$$\tau = \frac{1}{\omega_{ta}\beta} \tag{4.12}$$

Hence the unit step response for the system is,

$$V_{out}(s) = \frac{1}{\beta}(1-e^{\frac{-t}{\tau}}) \tag{4.13}$$

If δ is defined as the error between the final value and the above response, δ is given by,

$$1-\delta = 1-e^{\frac{-ts}{\omega_{ta}\beta}} \tag{4.14}$$

$$ts = \frac{1}{\omega_{ta}\beta} ln(\delta) \tag{4.15}$$

where ts is the settling time of the op-amp. By allocating a good error budget for δ and for a known settling time (ts), the bandwidth, ω_{ta} can be determined.

4.3.3 Load Capacitance

The load capacitance is an important consideration as it affects the bandwidth of the op-amp. The load capacitance would include $C_s + C_f$ of the next stage and also the capacitance in the switched-capacitor common-feedback circuit.

4.4 Operational Amplifier

As discussed already, the op-amp, more accurately called the operational transconductance amplifier is the key block that limits the performance of the MDAC and furthermore, the performance of the ADC. It was shown that to get a high-resolution and high-speed ADC, the DC gain and the unity gain frequency have to be very high. However, the realization of a CMOS operational amplifier that combines high DC gain with high unity gain frequency has been a problem [20].

The high gain requirement leads to multistage designs with long-channel devices biased at low current levels, whereas the high unity gain frequency requirement calls for a single-stage design with short-channel devices biased at high current levels. Cascoding is a well-known approach to enhance the DC gain of an amplifier without degrading the high-frequency behavior. However, cascoding alone is not enough to achieve the required gain for a 12-bit accuracy. In this design a gain-boosted fully differential folded-cascode amplifier is implemented. The gain boosting helped to achieve the required DC gain and a satisfactory settling behavior as well. The op-amp used in the prototype was designed by Xiaohong Du of Iowa State University [21]. This was used since it was already fabricated and some test results were expected.

4.4.1 Fully Differential Folded-Cascode Op-amp

In order to increase the open-loop gain, cascode techniques have been traditionally used in op-amp designs. Two famous cascode architectures are the Telescopic cascode and the Folded cascode. The main disadvantage of the Telescopic architecture is the limited output swing. The output swing in the telescopic op-amp is less than the folded cascode op-amp by at least one $V_{DS_{sat}}$.

The folded cascode architecture has cascode transistors at the output, to achieve higher output impedance but which are opposite in type from the input transistors to

get a higher signal swing. Figure 4.6 shows a fully differential folded-cascode amplifier. The input differential pair transistors, M1 and M2 are n-channel transistors whereas the cascode transistors M5 and M6 are p-channel transistors. This arrangement of opposite-type transistors allows the output of the amplifier to be at the same bias voltage level as the input i.e., the output common-mode voltage can be set at the same level as the input common-mode voltage. This is convenient for pipeline architecture since the output signal of one stage would be the input for the next stage.

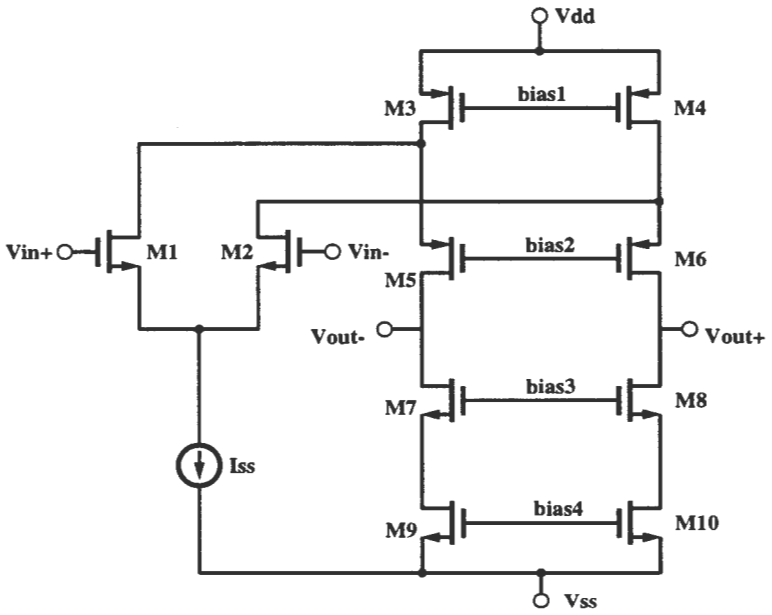

Figure 4.6 Schematic of the Fully Differential Folded-Cascode Op-amp

The dominant pole of the system is due to the load capacitance and the second pole is caused by the parasitic capacitances at the drain of the input transistors. The DC gain of the op-amp is of the order of $(g_m r_o)^2$ due to cascoding and is given by,

$$A_o = -\frac{g_{m1}}{\frac{g_{d7}g_{d9}}{g_{m7}} + \frac{(g_{d3}+g_{d1})g_{d5}}{g_{m5}}} \tag{4.16}$$

4.4.2 Principle of Gain Boosting

The gain-boost technique is based on increasing the cascoding effect of transistor M2, by adding an additional gain stage as shown in Figure 4.7. This stage reduces the feedback from the output to the drain of the input transistor [20]. The addition of the amplifier ideally increases the output impedance by a factor equal to one plus the loop gain(A_{add}) over that which would occur for a classical cascode current mirror.

$$R_{out} = [g_{m2}r_{o2}(A_{add} + 1) + 1]r_{o1} \tag{4.17}$$

Hence, the DC gain can be increased by several orders of magnitude.

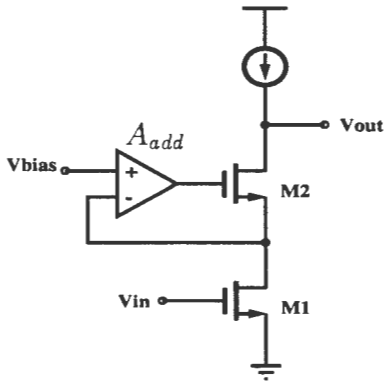

Figure 4.7 Cascoded Gain Stage with Gain Boosting

Figure 4.8 shows the original gain of the folded cascode amplifier without gain boosting (A_{orig}), the gain of the additional gain stage (A_{add}), and the total gain of the folded cascode amplifier with gain boosting (A_{tot}). Where DC value of A_{tot} would be approximately equal to $A_{orig} * (1 + A_{add})$. However, for $\omega > \omega_1$ (the 3dB frequency of the final amplifier), the output impedance is dominated by C_L which results in a first order roll-off of $A_{tot}(\omega)$. Moreover, this implies that ω_2 (3dB frequency of the boosting amplifier) should be greater than ω_1 so as not to limit the speed of the final op-amp. This is equivalent to the condition that the unity gain frequency (ω_4) of the boosting gain

stage has to be larger than the 3dB bandwidth (ω_3) of the original stage, but can be much lower than the unity gain frequency (ω_5) of the original stage [20]. The additional boosting stage introduces both poles and zeroes and hence they get canceled. However, the location of the poles and zeroes can affect the transient response a lot. A doublet always introduces a slow settling component in the transient response if the pole and zero are not close enough. Hence, the farther they are (can be seen from the dip in the phase response) the slower is the settling in the transient response. This was verified by having ideal gain boosting amplifiers and changing the location of the poles of the boosting amplifiers.

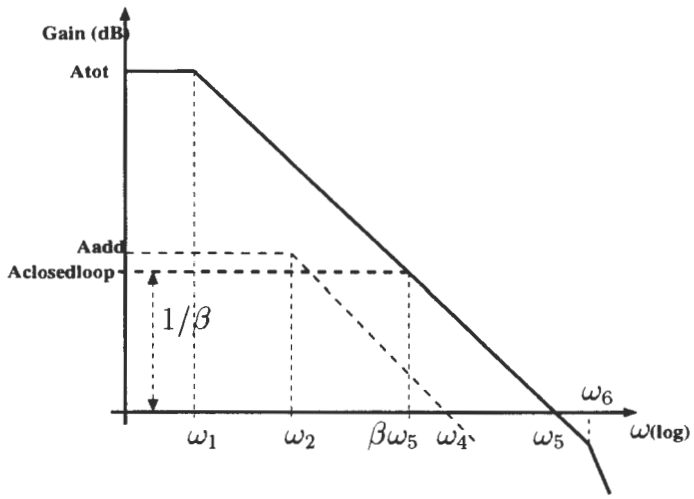

Figure 4.8 Bode Plots of the Op-amp Showing the 'safe' Pole Locations

A safe range of locating the unity gain frequency (ω_4) of the boosting stage is given by the following condition.

$$\beta\omega_5 < \omega_4 < \omega_6 \tag{4.18}$$

where ω_6 is the second pole location of the final amplifier and $\beta\omega_5$ is the 3dB frequency of the final amplifier when in closed loop.

4.4.3 Boosting Amplifier Design

The requirements of the boosting amplifier is to meet the unity gain frequency requirements that were discussed in the previous section and the required gain. Two types of boosting amplifiers were used because of the difference in signal swings - one for the p-channel transistors M5 and M6, and the other for the n-channel transistors M7 and M8. The boosting amplifiers constituted only of a differential stage and a level-shifter before it as shown in Figure 4.9 and 4.10.

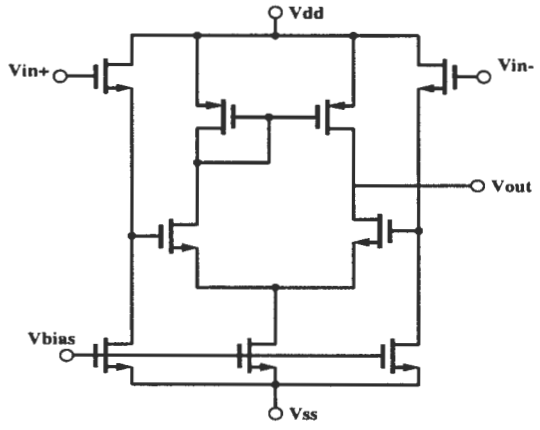

Figure 4.9 PMOS Boosting Amplifier

Since the boosting amplifiers need not be very fast, the power and area was very less than the main amplifier. The DC gain of the differential stage is of the order of $g_m r_o$. NMOS differential stage was used since the gain obtained would be much greater than PMOS differential pair because for 0.35μ process, $\mu_n/\mu_p > 3$. The PMOS boosting amplifier had a DC gain of 44 and the NMOS boosting amplifier had a gain of 52. Compensation capacitors were added at the output of the boosting amplifiers to meet the frequency requirement of Eq. 4.18.

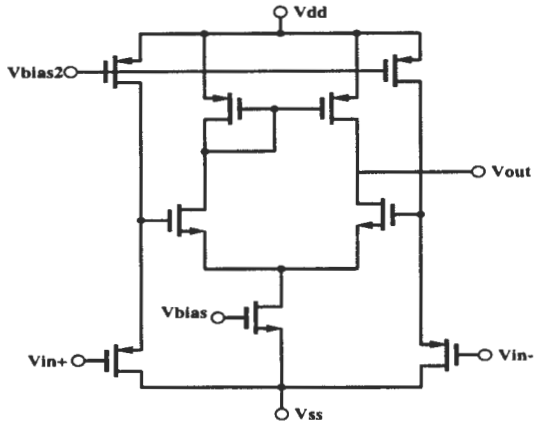

Figure 4.10 NMOS Boosting Amplifier

4.4.4 Gain-boosted Fully Differential Folded-Cascode Amplifier

Figure 4.11 shows the fully differential folded cascode amplifier with gain boosting without the common mode feedback circuit. The compensation capacitors at the output of the boosting amplifiers is added to achieve a good settling time by controlling the pole-zero locations. When the op-amp is slewing, the maximum current available for the slew rate is limited by the bias currents of the transistors M7 or M8. Even if the common mode feedback circuit is fast, the slew rate of a fully differential op-amp is seldom to the degree of a single-ended output op-amp. For this reason, fully differential folded-cascode op-amps are usually designed with the bias currents in the output stage equal to the bias currents in the input transistor pair [3]. This current in fairly large for high speed applications. In this design, the transistors M7 and M9 are biased with 2mA. To bias transistors biased in the saturation region,

$$I_D = \frac{\mu C_{ox} W}{2L}(V_{gs} - V_t)^2 \tag{4.19}$$

W/L's can be calculated by allowing a reasonable excess bias voltage $(V_{gs} - V_t)$ for the transistors.

$$\frac{W}{L} = \frac{2I_D}{\mu C_{ox}(V_{gs} - V_t)^2} \tag{4.20}$$

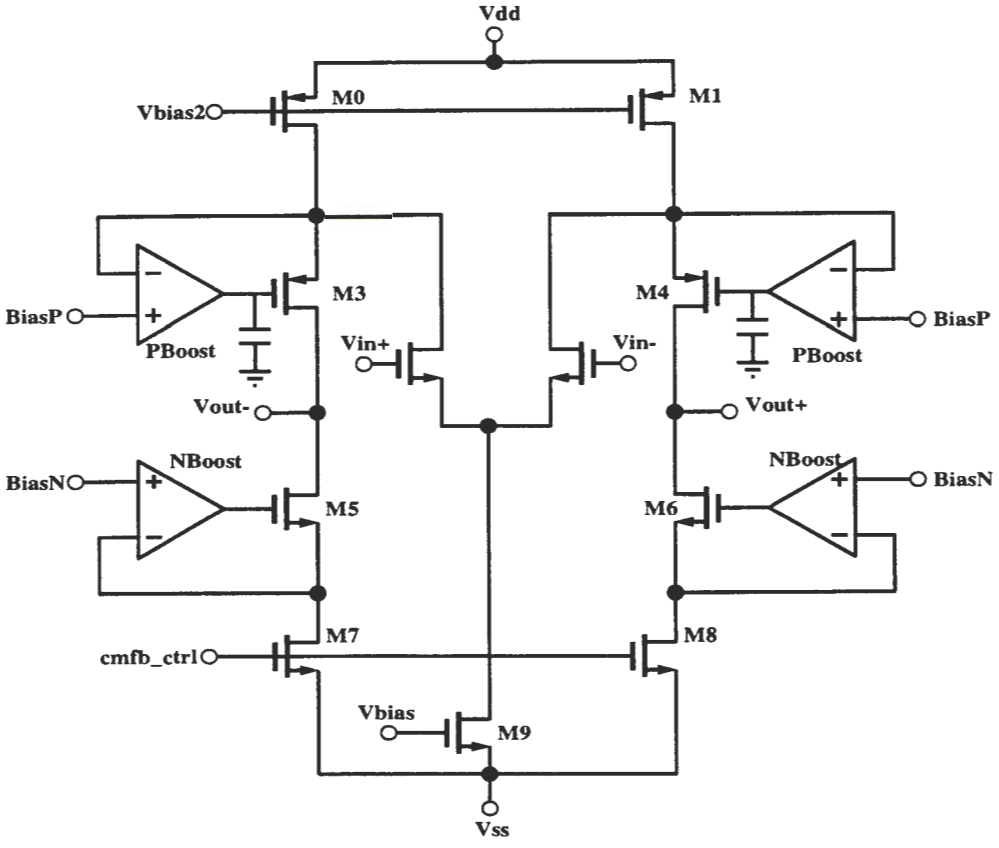

Figure 4.11 Fully Differential Gain-boosted Folded-Cascode Amplifier

The final DC gain of the amplifier is more than 12K (81dB). The phase margin is 59 degrees and the unity gain bandwidth is 545 MHz.

4.4.5 Common Mode Feedback Circuit (CMFB)

A common mode feedback circuit is necessary for fully differential op-amps to establish the common mode output voltage. Two typical types of CMFB circuits are continuous time and switched-capacitor type. Since the op-amp is used in switched capacitor circuit, the CMFB circuit is generally preferred to be of switched-capacitor type, since they allow a larger output swing [3]. The switched capacitor used is a simple circuit as shown in Figure 4.12.

The two capacitors are of the same size and should not be very large since this loads the op-amp, at the same time a smaller value might make it sensitive to charge injection from the switches. During the sampling phase, the pair of capacitors are precharged to the required value, such that the output of the op-amp is at common mode voltage. During the hold mode, the other ends of the capacitors are connected to the two outputs of the op-amp. Thus, if there is a common mode shift in the outputs of the op-amp, the value on the capacitors shifts by the same amount to keep the output at the common mode because of the negative feedback.

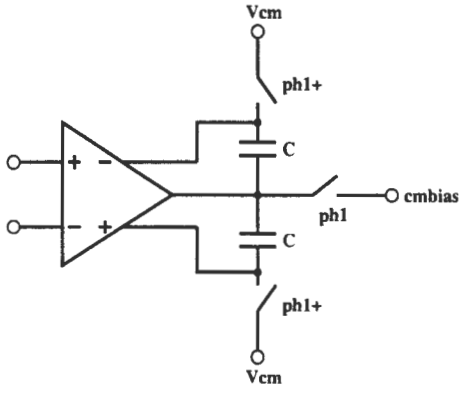

Figure 4.12 Common-mode Feedback Circuit

The simulation results of the Sample and Hold using the above op-amp is shown in Figure 4.13.

4.4.6 Comparator Design

The comparator starts to compare the output of the op-amp only after the output has settled to its final value, mandating the requirement of a very high speed comparator. A typical high speed comparator having a preamplifier followed by a track-and-latch stage was designed. The preamplifier is used to amplify the inputs and reduce the effects of kickback. The track-and-latch stage then amplifies this signal further during the

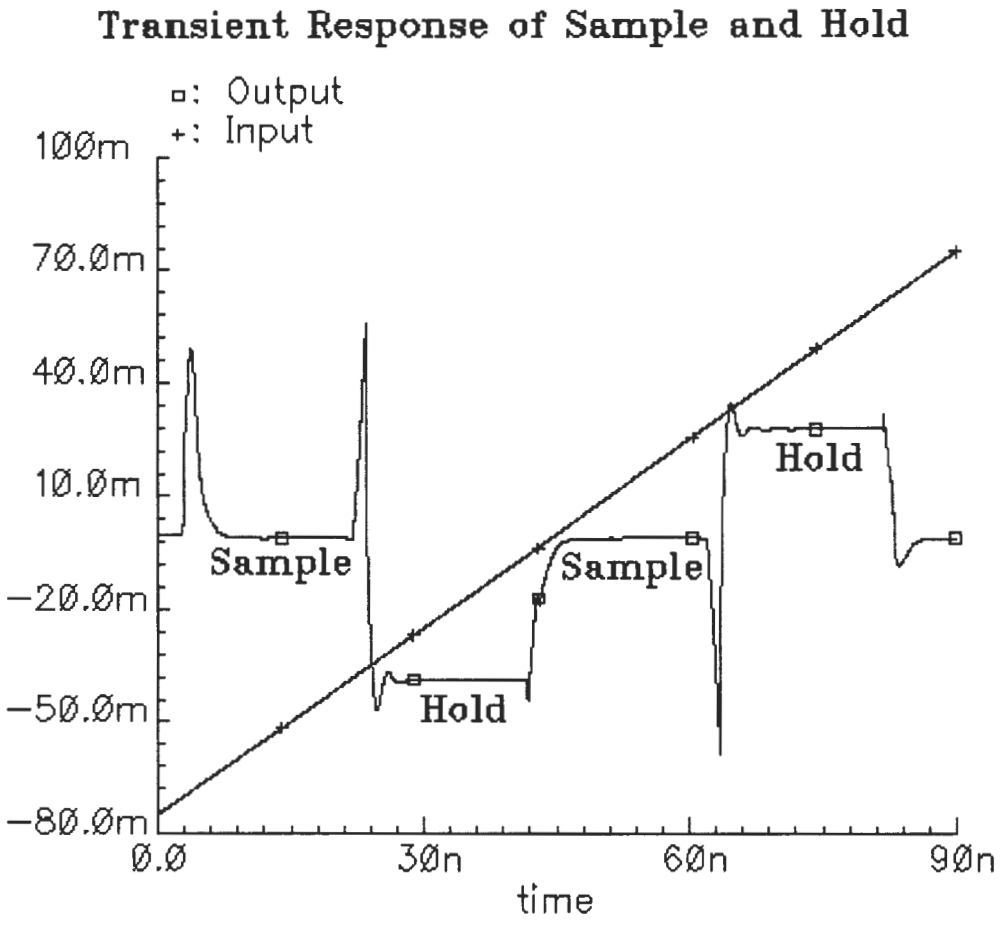

Figure 4.13 Transient Response of Sample and Hold

track phase, and then amplifies it again during the latch phase, when positive feedback is applied. The positive feedback regenerates the analog signal into full-scale digital signal.

Figure 4.14 shows the schematic of the comparator. The preamplifier's gain is decided based on the trade-off between resolution and speed. To get a better resolution the gain of the amplifier should be more and speed increases with decrease in the gain. Kickback denotes the charge transfer into the inputs when the track-and-latch stage goes from the track mode to the latch mode. Without a preamplifier or buffer, this kickback will enter the driving circuitry and cause very large glitches, especially in the case when the impedances seen looking into the two inputs are not perfectly matched.

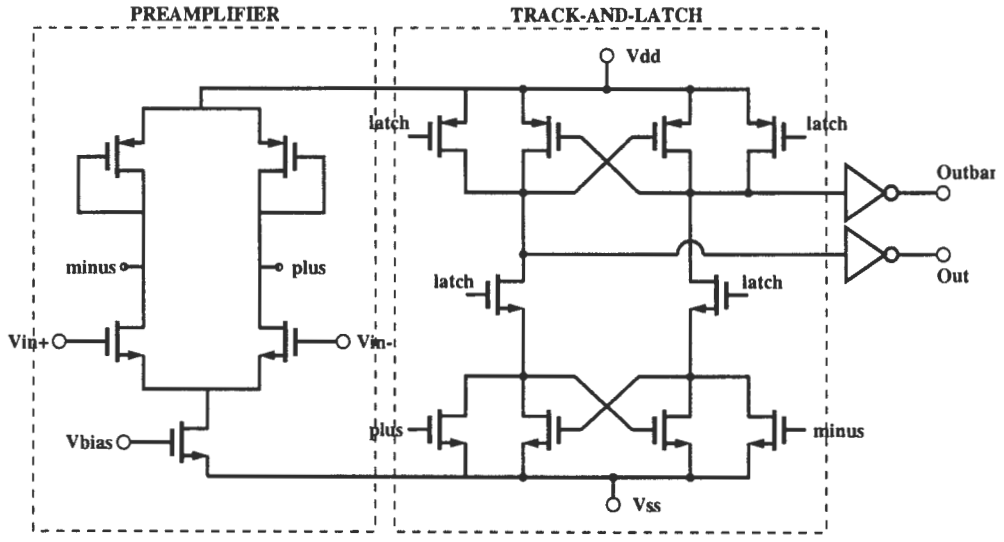

Figure 4.14 Preamplified Track-and-latch Comparator Schematic

The speed of the comparator highly depends on the time constant of the track-and-latch stage in its latch mode which in its simplest form is two inverters connected back-to-back as shown in Figure 4.15. The latch time for this is given by,

$$T_{latch} = K\frac{L^2}{\mu_n V_{eff}} \ln\left(\frac{\triangle V_{logic}}{\triangle V_o}\right) \tag{4.21}$$

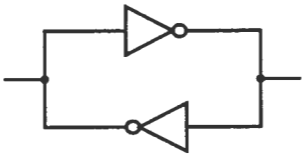

Figure 4.15 Simple Latch Mode Model of the Comparator

We can see that the transistors should have a minimum channel length, L and a high V_{eff} to reduce the time for latching.

If $\triangle V_o$ is small, the latch time can be considerably large, sometimes making it larger than the allowed time for the latch phase. When this happens, the comparator might take a wrong decision and this condition is referred to as *metastability.*

One very important consideration for comparators is to ensure that no memory is transferred from one decision cycle to the next. For example, if a comparator latches to one direction, it might have a tendency to stay in that direction, which is referred to as *hysteresis.* In order to eliminate it, the comparator should be reset by connecting the internal nodes to one of the power supplies or by connecting differential nodes together using switches before the track mode. To test the hysteresis of a comparator overdrive recovery test is usually performed [22]. In this test, during the first clock cycle the input is +1LSB. In the second clock cycle the input is negative full scale making the output to recover and also change polarity while in the following cycle the input is -1LSB making the output to recover but not change polarity. From the above test, it can be seen that in order for a comparator to respond correctly in the overdrive recovery test, the minimum clock period must allow two phenomena to complete - overdrive recovery in the preamplifier and generation of logic levels after the latch is strobed.

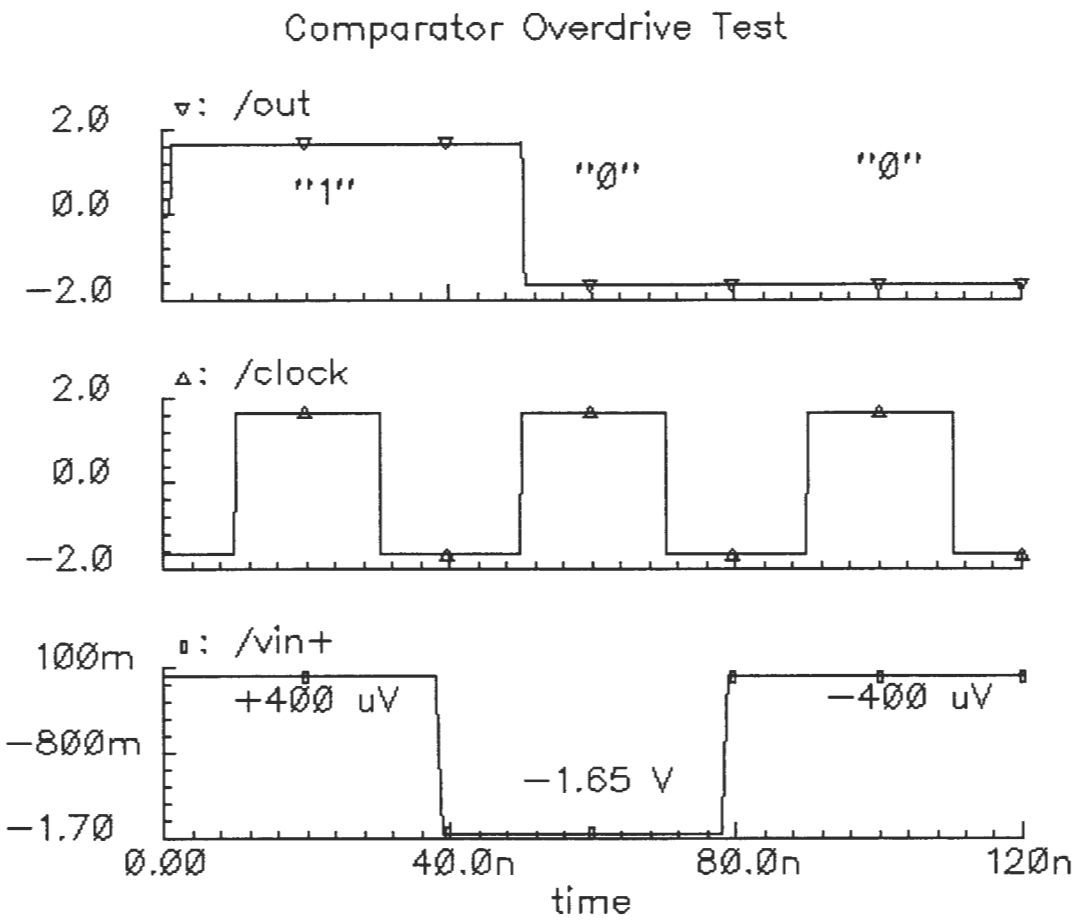

Figure 4.16 Comparator Overdrive Test Simulation Results

4.4.7 Single Stage of the Pipeline

In a simple pipeline the only two components of every stage are the op-amp and the comparator. However, for background calibration technique proposed here, the stages have to be modified to accommodate both calibration data and signal data at the same time in the pipeline. As presented in Chapter 3, the input to the MDAC in each stage can be either the S/H output, the previous stage's output or calibration input. For this the simplest solution is to have a 3:1 multiplexer. However, by making the signals pass through two extra switches, some amount of resolution is lost which is hence not a good solution. In the prototype, this problem was removed by having parallel switches and controlling the clocks by AND gates. This is illustrated in Figure 4.17. The ANDed clocks now have a good rise and fall time which aides in reduces the effect of charge-injection.

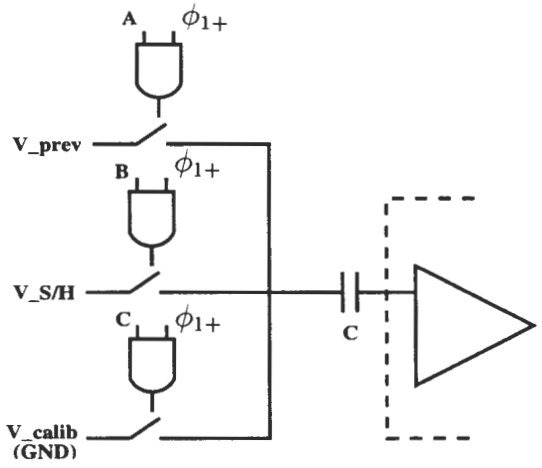

Figure 4.17 ANDing Technique to Remove the Multiplexer

By taking care that only one of A, B or C is high at any point of time, one of the three inputs can be given to the circuit. Also the digital inputs (digital outputs of previous stage) have the same three options of either being from the S/H stage, or previous stage or calibration input (the calibration is performed by measuring the output with a zero

analog input and first with digital input logic '1' and then with logic '0'). A simple 3:1 multiplexer can be used in this case, since the signals are digital levels and no signal resolution is lost by passing through extra switches. From the Table 3.2 it can be seen that in any one cycle only one of the stages is in the calibration mode, one is connected to the S/H and all the rest of the stages are connected to the previous stages. This makes it easier to generate the control signals for switching through all the stages. Since the calibration needs a delayed input signal, a second S/H following the first was used in the prototype. From the Table 3.2 it can also be seen that all odd stages of the pipeline take the input from the first S/H while all even stages of the pipeline take the input from the second S/H, the reason for this being all odd stages operate on clock ϕ_1 while all even stages operate on the alternate clock ϕ_2. All control signals were properly latched to clocks to avoid glitches in the actual signal. For example, all odd stages sample the input during ϕ_1 and the output is valid during ϕ_2. The comparator compares during ϕ_2 after the output has settled to its final value. The signals A, B, C in Figure 4.17 should be valid before ϕ_1, and hence latched during ϕ_2. Similarly, the control signals that control the digital multiplexer should be valid during ϕ_2 and hence they are latched during ϕ_1. As mentioned, control signals for all odd stages were given through a 3:7 decoder since the prototype was built with 14 stages in all.

Also since the output of the op-amp is differential, the comparator need not have an additional reference voltage. The outputs of the op-amp are directly given to the comparator inputs.

4.4.8 Clock Generator

As already mentioned adjacent stages of the pipeline operate on alternate non-overlapping clocks ϕ_1 and ϕ_2. Also, for bottom plate sampling ϕ_1- and ϕ_1+ are also required. The comparators and control signals are latched in the center of these signals to allow sufficient time for settling. All the clocks were generated internally. The non-

overlapping clocks were generated by the commonly used technique employing NAND gates and Inverters. A twice the frequency (50 MHz) clock was used to generate all the clocks as shown in Figure 4.18. The two D-flipflops with their outputs connected to the inputs help in achieving the $\div 2$ function to help get the comparator clocks in the center of ϕ_1. Sizing of the inverters was done appropriately to drive the necessary loads. The output inverters are very huge in size to achieve very fast rise and fall times.

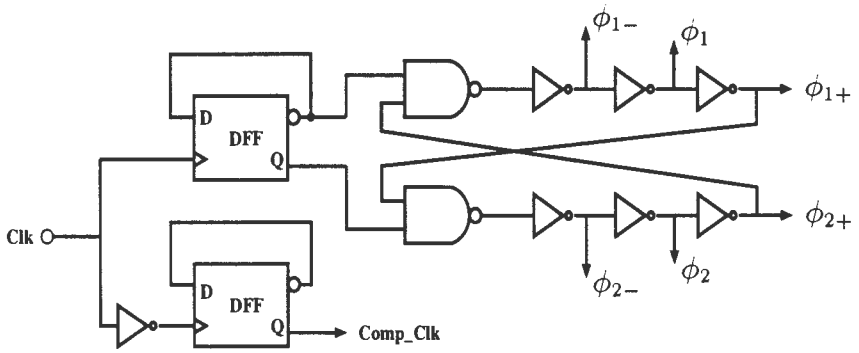

Figure 4.18 Clock Generator Schematic

4.4.9 Layout Considerations

One of the most important and crucial aspects of the design of analog systems is Layout. Special care was taken for the layout to be very symmetrical to avoid random offsets in all individual blocks. In mixed-signal chips, it is often unclear what is the best strategy to minimize the impact of noise coupling from the digital circuitry to the sensitive analog circuitry via the common substrate. The most effective way to reduce substrate noise is to create a low-impedance path from the p+ substrate to Vss, the lowest potential in the chip. In this chip, separate supply rails were used for digital circuits and analog circuits. A large number of guard rings were used around most transistors throughout to avoid latch-up problems and also to reduce the body(bulk)

voltage fluctuation which in turn might cause variation in the drain current through body effect. A separate substrate pin was used to set the substrate potential.

The two key sensitive blocks for layout are the operational amplifier and the comparator. The op-amp was fully differential and much care was taken to keep the symmetry in layout. All sensitive transistors in the op-amp and the comparator were inter-digitized to reduce mismatches. In the $0.35\mu m$ HP process, no standard linear capacitors were available. The capacitors were formed by the sandwich of Metal 2, 3 and 4 layers as shown in Figure 4.19. A common centroid layout with dummies was chosen for the capacitors in the MDAC to reduce mismatch. The top plates of the comparators were connected to the inputs of the op-amp since it had less parasitics.

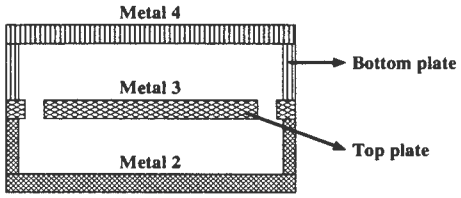

Figure 4.19 Metal Sandwich Capacitor

The layout of the clock generator is important for two reasons - the rise and fall times of the clocks affect the performance of switched-capacitor circuits by a great deal and the order in which alternate stages in the pipeline should be clocked. To have a good rise and fall time all clocks were buffered in every stage with inverters, so as to avoid the effect of loading due to routing. Clocking for two consecutive stages, say Stage 1 and Stage 2 should be such a way that Stage 2 stops sampling the output of Stage 1 before Stage 1 goes into sampling mode. Instead of having different clocks for this purpose, the same clock was used and above condition was taken care in layout. By having the clock generator at the end of the last stage and the clocks routed from the last stage to the first stage, takes care of this problem with the help of the delay due to routing. Figure

4.20 shows the layout of total chip with 14 stages and 2 S/H blocks.

The prototype was designed to be interfaced with an FPGA for easily implementing the digital calibration after measuring the calibration constants, and also to get the output bits in the correct order, since they would also be shuffled along with the stages during calibration.

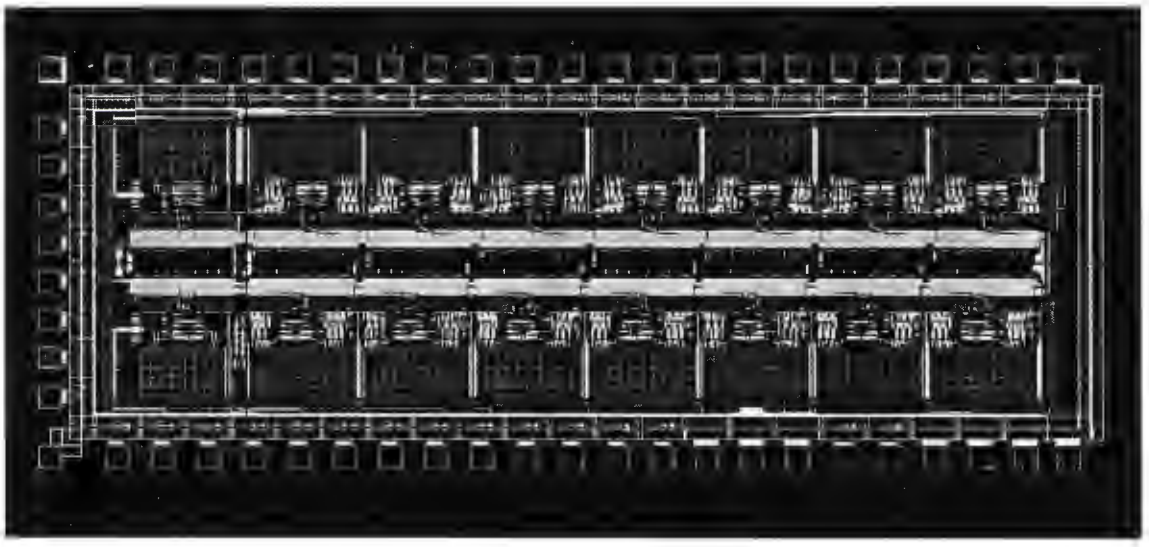

Figure 4.20 Layout of the Prototype

5 CONCLUSION

5.1 Thesis Summary

The digital background calibration technique described in this thesis provides a methodology for designing high-resolution, high-speed ADCs. The technique can be employed for pipeline or cyclic ADC architectures. The modular attributes of the pipeline and cyclic ADCs are powerful concepts for the system designer because of the potential for the ADC to be quickly modified to suit the needs of a given application.

The proposed technique in this thesis continuously corrects for errors due to capacitor mismatch, charge injection, finite op-amp gain and comparator offset. The calibration technique has advantage of not requiring any high-resolution, high-linearity analog components or external reference data converters. Background calibration enables the ADC to operate without interruption in the presence of environmental fluctuations, power supply changes and component aging.

Background calibration is achieved without limiting the conversion speed, the cost being one extra stage and digital hardware. To calibrate all the stages of the pipeline, $2 * 2^N$ clock cycles are required. Hence to achieve the required resolution a latency of $2 * 2^N$ clock cycles is required after the power-up of the ADC.

5.2 Future Work

In the proposed technique, though the output characteristic achieved is linear there will be a gain error between different characteristics as the stages are shuffled during calibration. This can be easily corrected digitally since they are linear and hence two points on the curve can get the slope and offset of the characteristic and from that the output digital code can be multiplied by a corresponding constant to remove the gain error. This has to be further investigated to achieve a simple solution.

Power dissipation is becoming an increasingly important issue in the design of ADCs because of the popularity of portable devices. In the prototype built, each stage consumes around 30mW of power, with the op-amp consuming most part of it. This might not be very good for low power applications and hence reducing the power consumption is an important direction for future work.

A further direction of this work can be to investigate the application of this technique to parallel pipeline ADCs since parallel architectures have the advantage of achieving very high speed. This can help in achieving both high resolution and high speed ADCs in the available CMOS technologies.

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