

**Power conversion techniques in nanometer CMOS for low-power
applications**

by

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TABLE OF CONTENTS

	Page
LIST OF TABLES	iv
LIST OF FIGURES	v
ABSTRACT	x
CHAPTER 1. INTRODUCTION	1
1.1 Basics on Power Conversion Schemes	3
1.2 Two-Step Power Conversion Schemes	9
1.2.1 Fully-Integrated Linear Regulators	11
1.2.2 Fully-Integrated Switching Regulators	13
1.3 One-Step Power Conversion Schemes	16
1.4 Thesis Organization	18
1.5 References	21
CHAPTER 2. ANALYSIS AND MODELING OF LOSSES IN LOW- POWER BUCK REGULATORS	26
2.1 Switching Losses Analysis	30
2.1.1 Transitional Losses	30
2.1.2 Gate & Switching Node Capacitance Losses Estimation	35
2.2 Conduction Losses Analysis	43
2.2.1 Power FETs Conduction Losses Estimation	43
2.2.2 Parasitics Conduction Losses Estimation	44
2.2.3 Body-Diode Losses Estimation	45
2.3 Simulation & Validation	46
2.4 Conclusion	58
2.5 References	59
CHAPTER 3. A FULLY-INTEGRATED BUCK REGULATOR WITH ON- CHIP PASSIVES AND CIRCUIT STUFFING	60
3.1 Feasibility Analysis and Optimization	61
3.2 Proposed Architecture	67
3.3 Circuit Implementation	69
3.3.1 Power Train and Self-Regulation	69
3.3.2 Compensator	70
3.3.3 PWM Comparator	71
3.3.4 Dynamic Level Shifter	73
3.4 On-Chip Inductor Design and Modeling	74

3.5 Experimental Results	79
3.6 Conclusion	81
3.7 References	83
 CHAPTER 4. A DCM-ONLY BUCK REGULATOR WITH HYSTERETIC- ASSISSTED ADAPTIVE MINIMUM On-TIME CONTROL FOR LOW-POWER MICROCONTROLLERS	 85
4.1 Limitations of Existing Control Schemes in Handling a Wide Range of Operating Scenarios in DCM	87
4.2 Proposed Control Scheme	88
4.3 Power-Gating and Circuit Implementation	98
4.3.1 Adaptive Minimum Constant On-time Pulse Generator	99
4.3.2 Control Comparator	101
4.4 Measurement Results	102
4.5 Conclusion	111
4.6 References	112
 CHAPTER 5. CONCLUSION	 115
5.1 Fully Integrated DC-DC Buck Converter in DCM/PFM Scenario	116
5.2 References	119
 BIBLIOGRAPHY	 120
 ACKNOWLEDGEMENTS	 128

LIST OF TABLES

	Page
Table 2.1. Design parameters for CCM scenario.	49
Table 2.2. Design parameters for DCM scenario.	49
Table 3.1. Loss and passive components comparison between 0.35 μ m and 65nm technologies	64
Table 3.2. Design Parameter for On-Chip Inductor	77
Table 4.1. Performance Summary	103
Table 4.2. Performance Comparison with other Published Work	111

LIST OF FIGURES

	Page
Figure 1.1. Schematic of a typical linear regulator with P type MOSFET as power transistor	5
Figure 1.2. A block diagram of a typical DC-DC buck regulator topology	7
Figure 1.3. Two-Step power conversion scheme for SoCs based on a separate PMIC and arrays of on-chip power converters within the SoC itself	11
Figure 1.4. Examples of on-chip power regulator topologies: Linear topology	13
Figure 1.5. Examples of on-chip power regulator topologies: Capacitor-based topology	16
Figure 1.6. Examples of on-chip power regulator topologies: Inductor-based topology	16
Figure 1.7. A block diagram of a typical SIMO power converter topology	18
Figure 2.1. (a) A typical buck converter including critical parasitics, and important waveforms in (b) CCM operation, and (c) DCM operation	29
Figure 2.2. A plot of the control signal of each power FET along with the voltage and current across the FET's drain-source terminals during the switching events noted in Fig. 1.1: (a) high-side FET in event (A), (b) high-side FET in event (B), (c) low-side FET in event (D), and (d) low-side FET in event (C)	36
Figure 2.3. Charge flow diagrams and loss equation derivations for CCM operation for (a) Event A (b) Event B	41
Figure 2.4. Charge flow diagrams and loss equation derivations for CCM operation for (a) Event C (b) Event D	42
Figure 2.5. Charge flow diagrams and loss equation derivations for DCM operation for (a) Event A (b) Event D	43

- Figure 2.6. The comparison between calculated and simulated power conversion efficiency in CCM and DCM scenarios with rail-to-rail gate control (a) CCM
(b) DCM 52
- Figure 2.7. The comparison between calculated and simulated power conversion efficiency in CCM and DCM scenarios with non-rail gate control (a) CCM
(b) DCM 53
- Figure 2.8. The comparison between calculated and simulated switching & conduction losses in CCM scenarios with rail-to-rail gate control: (a) CCM with 2MHz switching frequency (b) CCM with 3MHz switching frequency (c) CCM with 4MHz switching frequency 54
- Figure 2.9. The comparison between calculated and simulated switching & conduction losses in DCM scenarios with rail-to-rail gate control: (a) DCM with 130nS Ton (b) DCM with 205nS Ton (c) DCM with 290nS Ton 55
- Figure 2.10. The comparison between calculated and simulated switching & conduction losses in CCM scenarios with non-rail gate control: (a) CCM with 2MHz switching frequency (b) CCM with 3MHz switching frequency (c) CCM with 4MHz switching frequency 56
- Figure 2.11. The comparison between calculated and simulated switching & conduction losses in DCM scenarios with non-rail gate control: (a) DCM with 130nS Ton (b) DCM with 205nS Ton (c) DCM with 290nS Ton 57
- Figure 2.12. The comparison between calculated switching losses with proposed formulas in this thesis, calculated switching losses with formulas proposed in [4-5], simulated switching losses in CCM scenarios at 2MHz switching frequency 58

Figure 3.1. The calculated efficiency of the regulator with different power FETs size under different switching frequency	66
Figure 3.2. Top level block diagram for proposed buck regulator showing the self- regulation scheme, loop compensation, and the cascoded power switches	68
Figure 3.3. Schematic of the proposed compensator of the fully-integrated buck regulator	72
Figure 3.4. Schematic of the proposed PWM comparator of the fully-integrated buck regulator	72
Figure 3.5. Schematic of the proposed buffer stage of the PWM comparator	73
Figure 3.6. The schematic of the proposed dynamic level shifter	74
Figure 3.7. Three-segment lumped circuit model of the on-chip inductor	76
Figure 3.8. Proposed Inductor S-Parameter Simulation Results: Red Curve Inductor, Blue Curve ideal elements	77
Figure 3.9. The layout of proposed buck regulator with circuit stuffing	78
Figure 3.10. The simulated efficiency of the extracted layout of the proposed regulator: a) versus load current, and b) versus output voltage	80
Figure 3.11. Transient response of the extracted layout of the proposed regulator showing response to load/output voltage steps and self-regulation transition	81
Figure 4.1. Conventional controllers operating in DCM: (a) ACOT, and (b) Voltage- mode hysteretic. (c) Simulated inductor peak current and switching frequency versus load for the AMOT controller alone, hysteretic controller alone, and the transition between them in the proposed Hysteretic-Assisted AMOT controller	90

- Figure 4.2. (a) Block diagram of the proposed HA-AMCOT controller, (b) Important signals showing the operation of the controller when the load current is less than, or higher than half the constant inductor peak current, and (c) A complete flow chart describing the operation. 96
- Figure 4.3. Schematics of the proposed: (a) AMOT pulse generator with power-gating, and (b) Control comparator with power-gating. 98
- Figure 4.4. Die photo of the proposed HA-AMOT regulator showing double bonding at the input ground rails, as well as the switching node. 103
- Figure 4.5. Transient measurements showing inductor current, output voltage, and switching node of the proposed regulator with 3.3V input voltage, 1.2V output voltage, and various load currents. (a), (b), (c), and (d) show the results with a 4.7 μ H inductor, while (e), (f), (g), and (h) show the results with a 10 μ H inductor 106
- Figure 4.6. Measured inductor peak current versus load for various scenarios showing the transition points between the AMOT and hysteretic modes. 107
- Figure 4.7. The measured efficiency versus load current of the proposed HA-AMOT regulator for various operating scenarios 107
- Figure 4.8. Comparison between the measured efficiency using the HA-AMOT control with and without power-gating, with hysteretic mode forced across the entire load range (pure hysteretic operation), and with the on-time modified to operate as a conventional ACOT controller in DCM. 108

Figure 4.9. The regulator's response to a 1mA to 40mA load step with 3.3V input, 1.2V output, and 4.7 μ H inductor: (a) with a 20 μ s time scale, and (b) with a 4 μ s time scale and more frequent load

ABSTRACT

As System-on-Chip (SoCs) in nanometer CMOS technologies grow larger, the power management process within these SoCs becomes very challenging. In the heart of this process lies the challenge of implementing energy-efficient and cost-effective DC-DC power converters. To address this challenge, this thesis studies in details three different aspects of DC-DC power converters and proposes potential solutions. First, to maximize power conversion efficiency, loss mechanisms must be studied and quantified. For that purpose, we provide comprehensive analysis and modeling of the various switching and conduction losses in low-power synchronous DC-DC buck converters in both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) operation, including the case with non-rail gate control of the power switches. Second, a DC-DC buck converter design with only on-chip passives is proposed and implemented in 65-nm CMOS technology. The converter switches at 588 MHz and uses a 20-nH and 300-pF on-chip inductor and capacitor respectively, and provides up to 30-mA of load at an output voltage in the range of 0.8–1.2 V. The proposed design features over 10% improvement in power conversion efficiency over a corresponding linear regulator while preserving low-cost implementation. Finally, a 40-mA buck converter design operating in the inherently-stable DCM mode for the entire load range is presented. It employs a Pulse Frequency Modulation (PFM) scheme using a Hysteretic-Assisted Adaptive Minimum On-Time (HA-AMOT) controller to automatically adapt to a wide range of operating scenarios while minimizing inductor peak current. As a result, compact silicon area, low quiescent current, high efficiency, and robust performance across all conditions can be achieved without any calibration.

CHAPTER I. INTRODUCTION

The wide use of portable communication, navigation, and multi-media devices has fueled the demand for increasing the functional capabilities of these devices while reducing their power consumption and implementation size and cost. To meet this demand, the concept of mixed-signal System-on-Chip (SoC) has been introduced, where numerous analog, RF, and digital processing circuitries are implemented together in a single CMOS chip [1, 2]. The SoC concept, along with the dramatic scaling of the feature size of CMOS technologies to the nanometer levels, have been certainly transformational in terms of expanding the functional capabilities of mobile devices and reducing their power, size, and cost. Nonetheless, several complex challenges in terms of how power can be delivered to the SoC have been introduced as a byproduct of the SoC concept itself as well as the nature of nanometer CMOS technologies. Firstly, the SoC concept entails that the SoC contains an extensive mix of various circuit functions (analog, RF, and digital), with each function requiring its own independent and isolated power supply domain with unique specifications. Even within a specific circuit function, several independent power supply domains may be required. For instance, a data converter function may require a power supply domain for its analog part and another one for its digital part. As a result, the number of independent power supply domains in SoCs has grown significantly, and can easily exceed 30 in larger SoCs [2]. Implementing such a large number of power supply domains is very challenging in terms of cost and size. This is due to the fact that traditional power supplies require energy-storing passive components (i.e. inductors and capacitors) that are too large to integrate on chip, and therefore must be off chip. In addition to the fact that these off-chip passive components are

relatively expensive, they also consume significant real state area on the Printed Circuit Board (PCB), which further increases the cost and size of the system. Moreover, for the SoC to utilize these off-chip passive components, additional package pins become necessary, which is difficult to accommodate in pin-limited SoCs without adopting larger and more expensive packaging options. Secondly, as CMOS technology scales down to nanometer levels, the voltage rating of its devices, as well as the power supply levels required by the various circuit functions within the SoC, scale down to 1.8V or lower. Utilizing these devices to implement power supplies that operate from a Li-Ion battery with voltage levels as high as 5V while ensuring the reliability of these devices becomes challenging, and often times comes at the expense of complicated design and large silicon area [3], or additional mask cost for implementing special high-voltage devices [4, 5].

In this chapter, we will first introduce the basics of power conversion schemes, focusing on the step-down converting solutions. The introduction includes the definitions and basic components that are widely implemented across many applications. After that, the different methods that can be employed to generate a large number of power supply domains from a single shared battery in mixed-signal SoCs are discussed, along with the advantages and limitations of each method in terms of efficiency, dynamic operation, and cost. This includes two-step approaches that involve a separate Power Management Integrated Circuit (PMIC) for primary power conversion, followed by secondary power converters within the SoC itself to generate multiple on-chip power supply domains. These secondary power converters can be linear regulators, or alternatively, can be fully-integrated high-frequency switched-C and switched-L regulators with on-chip passive components in order to improve power conversion efficiency. Single-step approaches will also be discussed, which includes

Single-Inductor-Multiple-Output (SIMO) power conversion schemes. This chapter will also give an overview of some proposed techniques that can be used to reduce the silicon area overhead of on-chip power supplies, along with techniques to improve the power conversion efficiency as well as dynamic and noise performance. Finally, the organization of the thesis will be discussed.

1.1 Basics on Power Conversion Schemes

As it is discussed previously, nanometer CMOS mixed-signal SoCs requires a large number of independent and well-isolated power domains with only limited input power sources. Most likely, the power source will be a single battery with higher voltage than the desired voltage level for the system(e.g. coin cell battery or Li-Ion battery). Thus, step-down power converters are widely implemented in order to generate these power domains from a single power source. In general, there are two categories of broadly used DC-DC step-down converters: (a) linear regulators; (b) switching regulators.

Fig. 1.1 shows the schematic of a generic linear regulator with a P type MOSFET(MP_1) as the power transistor. By adjusting the resistive divider R_1 and R_2 , the regulator is able to maintain a constant output voltage as:

$$V_O = V_{REF} \times \frac{R_1 + R_2}{R_2} \quad (1.1)$$

where V_{REF} typically comes from the band-gap. Depending on the application and the type of the load, the output capacitor C_L can be implemented either on PCB or integrated on die[6, 7]. The way this circuit works is that the feedback loop constantly modulating the resistance of the power transistor MP_1 so as to create a resistive ladder between MP_1 and the load, creating the regulated output voltage V_O while dumping current that is consumed by the load. In general, the feedback loop architecture may vary while the power transistor may also be implemented as a N type MOSFET depending on the application and the compensation techniques[8]. The advantage of this type of regulator is simple to implement, robust and low cost.

One major disadvantage of the linear regulator is that the power conversion efficiency degrades with respect to the ratio between the input and the output of the regulator since all the current delivering to the load also flows through MP_1 . Thus, the power conversion efficiency of the linear regulator can be approximately derived as:

$$\eta = \frac{P_O}{P_{IN}} = \frac{V_O \times I_O}{V_{IN} \times I_{IN}} \quad (1.2)$$

While P_O and P_{IN} are denoted as output and input power, respectively. Note that the input power calculation ignores the power consumed by amplifier A_1 assuming it is relatively small(e.g. tens of μA). Based on eq. (1.2), the power conversion efficiency with input voltage as 3.3 V and output voltage as 1.2 V can only be approximately 36%, which is considered as fairly inefficient. DC-DC switching regulators, on the other hand, are famous for their high power conversion efficiency over a wide range of input and output conditions. This has been realized by transferring energy between energy-storage elements(e.g. inductor and capacitor) based on certain patterns(e.g. turn on and off switches)[9-10]. By doing this, the energy is

saved since the power switches do not have to constantly burning all the redundant power any more comparing to the linear regulator since the energy can be stored on those energy-storage components. Among all types of DC-DC step-down switching regulators, the inductor based, DC-DC buck regulator is the best in class in terms of the power conversion

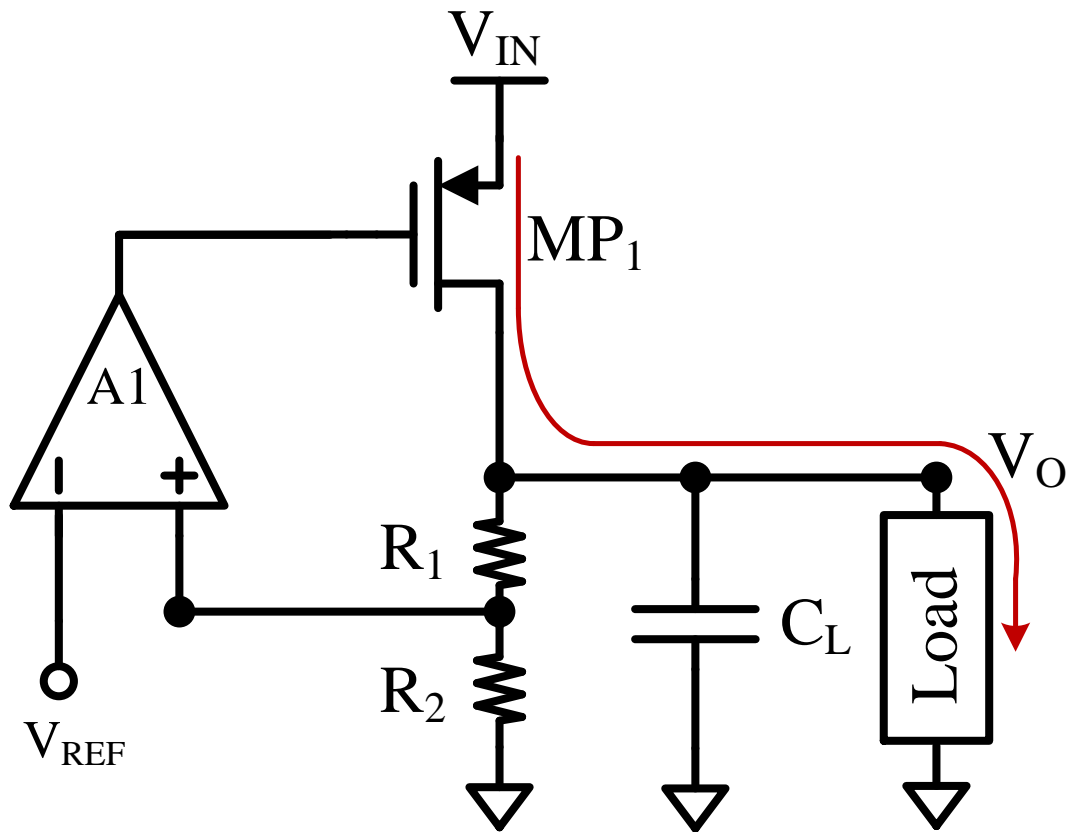


Figure 1.1. Schematic of a typical linear regulator with P type MOSFET as power transistor

efficiency. Based on the report from the literatures, those kind of switching regulator can achieve 95% efficiency and above[11].

The block diagram of a typical DC-DC buck regulator is shown in Fig. 1.2. This type of regulator is typically composed with an off-chip inductor and an off-chip capacitor at 1-100 μH and μF level. The high-side power transistor MP_1 and low-side power transistor MN_1 and their corresponding gate driver are the major contributor to the total silicon area. This will help reduce the conduction loss due to charging and discharging the inductor in order to achieve high power conversion efficiency. The control and compensation block is typically composed of amplifiers, comparators, ramp generators and digital logic circuits, etc. The functionality of this block is to properly control the on/off of the high-side power transistor MP_1 and low-side power transistor MN_1 so that a desired output level can be generated and maintained. Note that the output level is a DC voltage with AC component on top of it. This AC component is called “ripple” and typically stays in the range of a few mV to tens of mV.

Typically, the “on” time of the high-side power transistor MP_1 is defined as T_{on} while the “on” time of the low-side power transistor MN_1 is defined as T_{off} . To control the buck regulator, one famous control topology, Pulse-Width-Modulation(PWM) control is to keep the sum of T_{on} and T_{off} unchanged(e.g. fixed switching frequency) while modulating the ratio between T_{on} and T_{off} to achieve the desired output voltage level. On the other hand, one can also keep T_{on} or T_{off} unchanged and modulating the operating frequency of the regulator to achieve the same goal. This type of control topology is referred as Pulse-Frequency-Modulation(PFM) control. No matter which control topology is used, as long as the regulator stays in Continuous-Conduction-Mode(CCM) condition, the relationship between the input and output can be derived as[12]:

$$V_O = V_{IN} \times \frac{T_{on}}{T_{on} + T_{off}} \quad (1.3)$$

By analyzing the above equation, one can easily come to the conclusion that, in theory, the regulator can generate the same output voltage with different switching frequency as long as the ratio between the high-side power transistor “on” time and total period is the same. However, this does not mean that designer can pick whatever switching frequency they want in the actual design. In general, the operating frequency of the regulator is inversely proportional to the ripple at the output. On the other hand, the power loss due to turning on/off the power transistors is proportional to the operating frequency. Thus, designers need to carefully budget all the design parameters so as to achieve the best performance of the regulator based on the specific application.

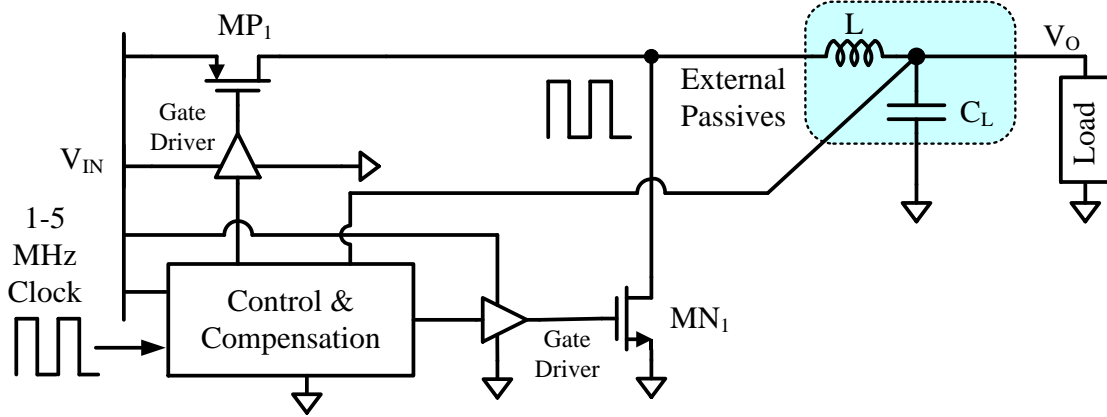


Figure 1.2. A block diagram of a typical DC-DC buck regulator topology

The efficiency analysis for a buck regulator is slightly different than the linear regulator since the loss mechanism of a buck regulator is more complex. In general, there are two types of losses in a buck regulator: a) conduction losses; b) switching losses. Conduction losses are due to the finite resistance of the power transistor MP_1 and MN_1 while the switching losses are due to the energy it takes to charge and discharge the parasitic capacitance of the power transistor(e.g. gate to source capacitance). Thus, the efficiency of a buck regulator can be derived as:

$$\eta = \frac{P_O}{P_{IN}} = \frac{P_O}{P_O + P_{loss_cond} + P_{loss_sw}} \quad (1.4)$$

Where P_{loss_cond} and P_{loss_sw} represent the conduction losses and switching losses, respectively. In general, for a given input and output condition, P_{loss_cond} is proportional to the product of the load and the “on” resistance of the power transistor while P_{loss_sw} is proportional to the product of the equivalent gate capacitance of the power transistor and the switching frequency. Moreover, the “on” resistance of the power transistor is inversely proportional to the total gate capacitance of the power transistor since a “larger” MOSFET typically contains more parasitic capacitance. Thus, for a given load and switching frequency, it is possible to arrive at an optimized size of the power transistor after some iteration.

Typically, the PWM control topology is widely used for the load range around hundreds of mA as it can achieve a relatively flat and optimum efficiency curve over a wide range of load variation[13]. However, once it comes to light load conditions(e.g. less than 10mA), the switching losses will dominate the conduction losses, causing a massive

efficiency degradation. In this case, the PFM control is preferred since the switching frequency can be adjusted depending on the load conditions so that the switching losses and conduction losses can be balanced. Thus, the classic DC-DC buck regulator typically contains both PWM and PFM modes so as to achieve high efficiency curve over a wide load range (e.g. 10mA to 1A)[14].

1.2 Two-step Power Conversion Schemes

Conceptually, all the power supply domains needed by the SoC can be implemented externally with high power conversion efficiency using a separate Power Management Integrated Circuit (PMIC) and then delivered to the SoC. However, as the number of power supply domains increases, this solution becomes unrealistic from a cost and size perspective, not only due to the passive components involved, but also due to the large count of package pins that would be required in the PMIC and the SoC to connect these power supply lines. Moreover, since the SoC may require many of these power supplies to be adaptive (i.e. their voltage levels may need to be varied with time to optimize the load performance), some form of communication between the SoC and the PMIC is necessary, which adds to the complexity of the system design and limits the speed at which these power supplies can be adapted by the SoC. Moreover, due to the package and PCB parasitics associated with routing these power supply lines, the overall efficiency and the dynamic performance of the power supplies can be significantly degraded. For the above reasons, the two-step approach shown in Fig. 1.3 has become the most attractive and commonly-employed power conversion scheme in SoCs today. As shown, a separate PMIC is still used, but only for generating a

limited number of primary power supply domains directly from the battery, typically one for analog functions and another for digital functions [1, 2]. These shared power supplies are usually implemented using switching power regulators, and thus offer high power conversion efficiency. Subsequently, these primary power supplies are used to generate a large number of independent secondary power supplies within the SoC itself using arrays of on-chip power regulators. This two-step approach has the advantage of limiting the number of external power supplies that must be routed to the SoC, which saves a significant count of package pins. Furthermore, the separate PMIC can be implemented in a suitable CMOS technology that can interface with the high-voltage battery without reliability concerns. Moreover, since the primary power supplies routed to the SoC have much lower voltage levels, implementing the secondary on-chip power supplies within the SoC using nanometer CMOS technology is greatly simplified in terms of reliability. Additionally, with the secondary power supplies integrated within the SoC, adapting them dynamically to the specific demand of their loads can be done without the complexity of communicating with the PMIC. Finally, the off-chip passive components count is greatly reduced as they are needed for only few primary power supplies, which reduces the size and cost of the whole system. The on-chip secondary power supplies can be implemented in several ways as detailed below.

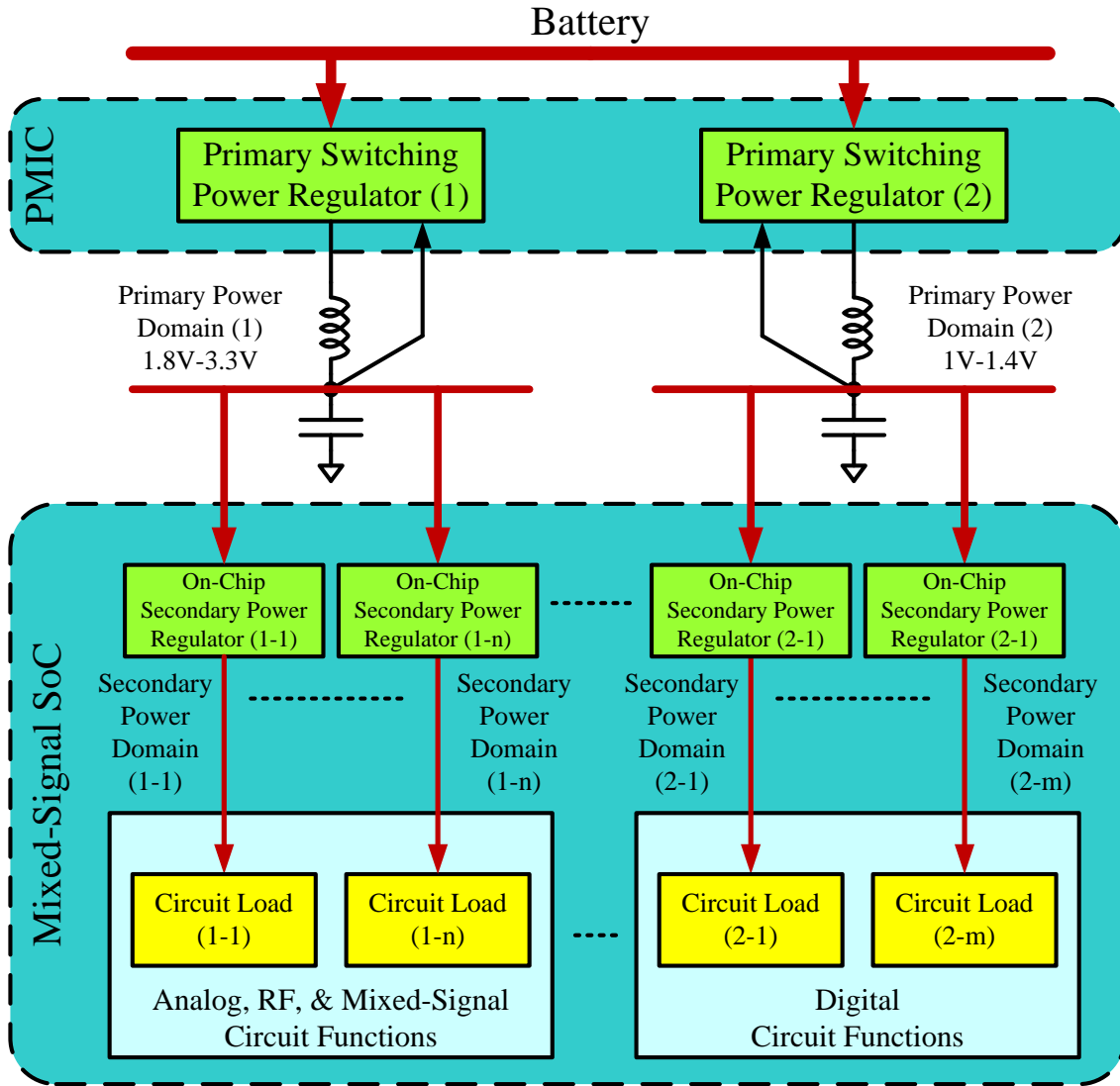


Figure 1.3. Two-Step power conversion scheme for SoCs based on a separate PMIC and arrays of on-chip power converters within the SoC itself.

1.2.1 Fully-Integrated Linear Regulators

Linear regulators are very popular due to their relatively compact size and small passive components count (usually a single capacitor), which help reducing their implementation cost. Moreover, they offer low noise performance due to lack of inherent

switching, as well as their ability to suppress noise from the primary power supplies. Although conventional linear regulators require output capacitors that are too large to integrate on chip, numerous new topologies, example of which is shown in Fig. 1.4, have been proposed that enable their implementation using only hundreds of Pico-Farads capacitors [15-20]. These topologies have made linear regulators very popular in SoCs since fully-integrated realizations became possible with only on-chip capacitors. Moreover, many of these topologies offer wide-band performance when implemented in nanometer CMOS, which allows for faster dynamic operation. However, linear regulators suffer from poor power conversion efficiency and can significantly affect the overall efficiency of the system if widely used across the SoC. Moreover, fully-integrated topologies with on-chip capacitors suffer from poor Power Supply Rejection (PSR) around the typical frequencies used in the primary switching power supplies [21]. This limits their ability to reject the switching noise present at the primary power lines and may require employing complicated control techniques in the primary power supplies to reduce their switching noise [21-23].

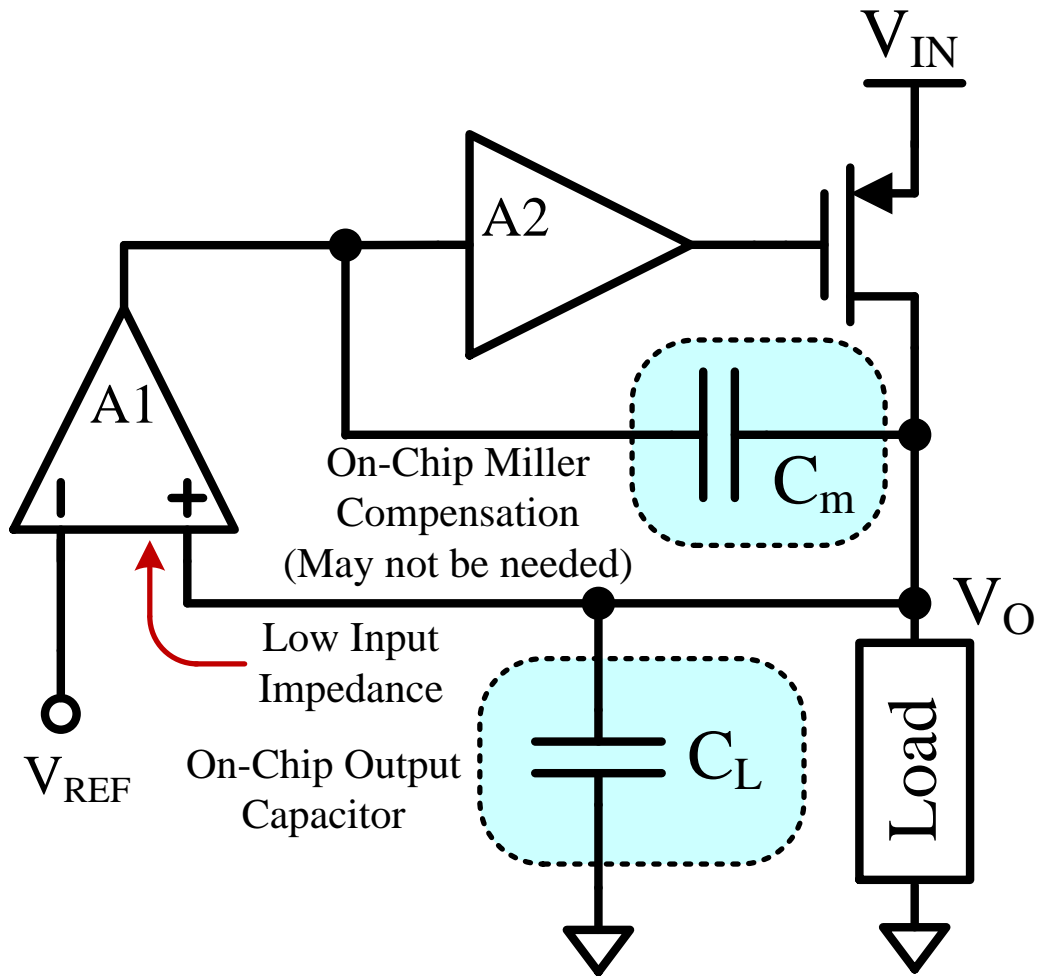


Figure 1.4. Examples of on-chip power regulator topologies: Linear topology

1.2.2 Fully-Integrated Switching Regulators

To circumvent the efficiency degradation caused by employing linear regulators as secondary power supplies within SoCs, they can be replaced by fully-integrated capacitor-

based [2, 24-27] or inductor-based [28-31] switching regulators, examples of which are shown in Fig. 1.5 and 1.6. Traditionally, these regulators require large off-chip passive components due to their low switching frequency, which can't be increased to avoid excessive switching losses and degraded efficiency. However, with the scaling of CMOS technologies to nanometer levels, these regulators can be implemented with much higher switching frequencies while maintaining reasonable switching losses and better overall efficiency than linear regulators [1]. Consequently, the passive components required can be scaled down to levels where they can be implemented on-chip [2, 24-31], and much faster dynamic performance can be achieved.

One major limitation of fully-integrated realizations of switching regulators, however, is their large silicon area compared to linear regulators, primarily due to the area overhead of the on-chip passives. In fact, the area of some of these realizations can consume between twice to ten times the area of a corresponding linear regulator. In inductor-based realizations, this problem is exacerbated by the fact that the area underneath on-chip inductors (implemented using top thick metal layers) is left unused to avoid additional losses through electromagnetic coupling with any circuits or routing underneath the inductor. This forces implementing the rest of the regulator's circuitry (including the output capacitor) outside the inductor area, leading to much larger silicon area. To reduce the overall area, there have been recent proposals to stuff circuits underneath on-chip inductors, particularly in step-down regulators [30]. These implementations rely on the fact that the switching frequency, though high, but not as high as RF applications where electromagnetic coupling losses are a real concern. Moreover, since in step-down regulators the output capacitor is shorted to one side of the inductor anyway, it may be feasible to at least stuff that capacitor underneath the

inductor. These realizations can significantly reduce the total area of the regulator to bring it closer to the area of a corresponding linear regulator. In capacitor-based realizations, there is little that can be done, other than increasing the switching frequency, to reduce the total area because the on-chip capacitors use the poly-well layers, which renders their area unusable for anything else.

Another major limitation of fully-integrated realizations of switching regulators is the quality factor of the on-chip passive components, which significantly degrades the overall power conversion efficiency. In inductor-based realizations, the series resistance of the on-chip inductor dominates the losses and limits the overall efficiency to about 10% better than linear regulators in best case scenarios [30]. This can be circumvented in some cases by using multi-phase designs to reduce conduction losses in the inductor and use non-standard CMOS technologies that offer additional thick metal layers for implementing higher quality inductors [29, 31]. However, these technologies are more expensive than standard CMOS and are difficult to justify in commercial applications that do not contain RF functions. There have also been proposals to employ on-package air-inductors [32] or bond-wire inductors [33] that feature better quality than on-chip counterparts. However, this requires special packaging consideration, and thus cost, pin count, and integration continues to be a challenge. On the other hand, the bottom plate parasitics of on-chip capacitors limit the overall efficiency of capacitor-based realizations of fully-integrated switching regulators [2]. Nevertheless, recently reported implementations are showing a great promise for achieving higher levels of efficiency than inductor-based counterparts [24].

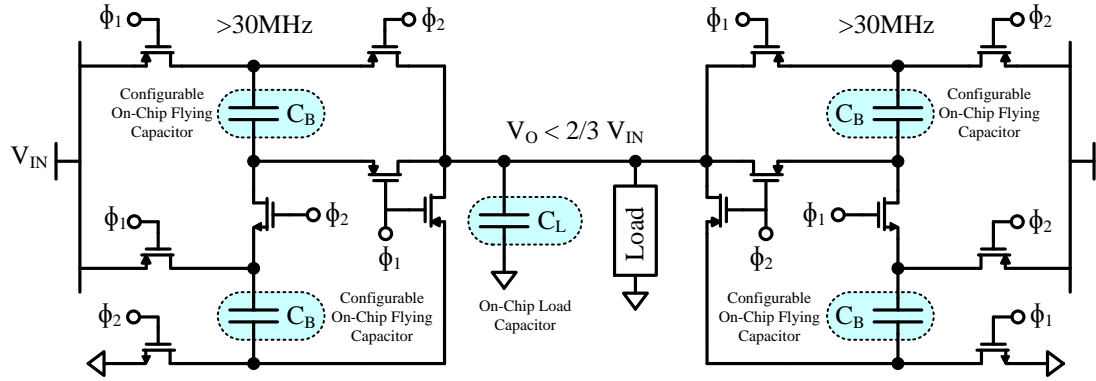


Figure 1.5. Examples of on-chip power regulator topologies: Capacitor-based topology [2]

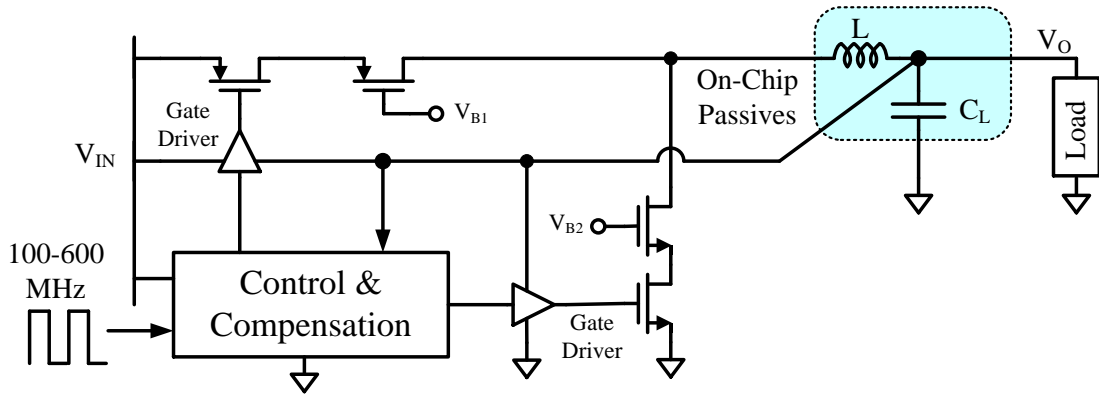


Figure 1.6. Examples of on-chip power regulator topologies: Inductor-based topology [30].

1.3 One-step Power Conversion Schemes

A major limitation of the two-step power conversion approach discussed in the previous section is the degraded efficiency resulting from cascading power converters. For instance, cascading two power converters, each with 80% efficiency, results in an overall efficiency of only 64%. For that reason, single-step switching power conversion schemes that

operate directly from the battery and implemented within the SoC are becoming increasingly popular. In addition to the efficiency advantage of this strategy, it also eliminates the need for a separate PMIC. To avoid the large count of passive components, particularly inductors, SIMO topologies such as the one shown in Fig. 1.7 have been used to implement a large number of efficient power supplies for SoCs in nanometer CMOS technologies [34]. However, due to the high-voltage rating of Li-Ion batteries, special high-voltage transistors must be available in the technology flow to interface with the battery. This constitutes an additional cost beyond standard nanometer CMOS technology nodes. Moreover, although traditional SIMO topologies limit the number of inductors to only one, each power supply continues to require a large off-chip capacitor. This entails the same issues associated with the cost and size of these capacitors as well as the package pins count to interface with them as described in the previous section. Therefore, these topologies still create a tradeoff between cost and efficiency. Furthermore, since traditional SIMO topologies use low switching frequencies to achieve high efficiency, and since they must distribute the energy of a single inductor to many outputs in a sequential manner, their transient performance is typically slow, which limits the ability to dynamically adapt them as the SoC demands. The above limitations are spurring new research that attempts to reduce the output capacitors in single-step SIMO topologies to levels where they can be integrated on chip while preserving their efficiency advantage. This includes dual-frequency SIMO topologies that feature fully-integrated outputs and offer very fast dynamic operation [35]. These topologies can enable the implementation of a large number of highly-efficient power supplies within the SoC without the overhead of off-chip capacitors.

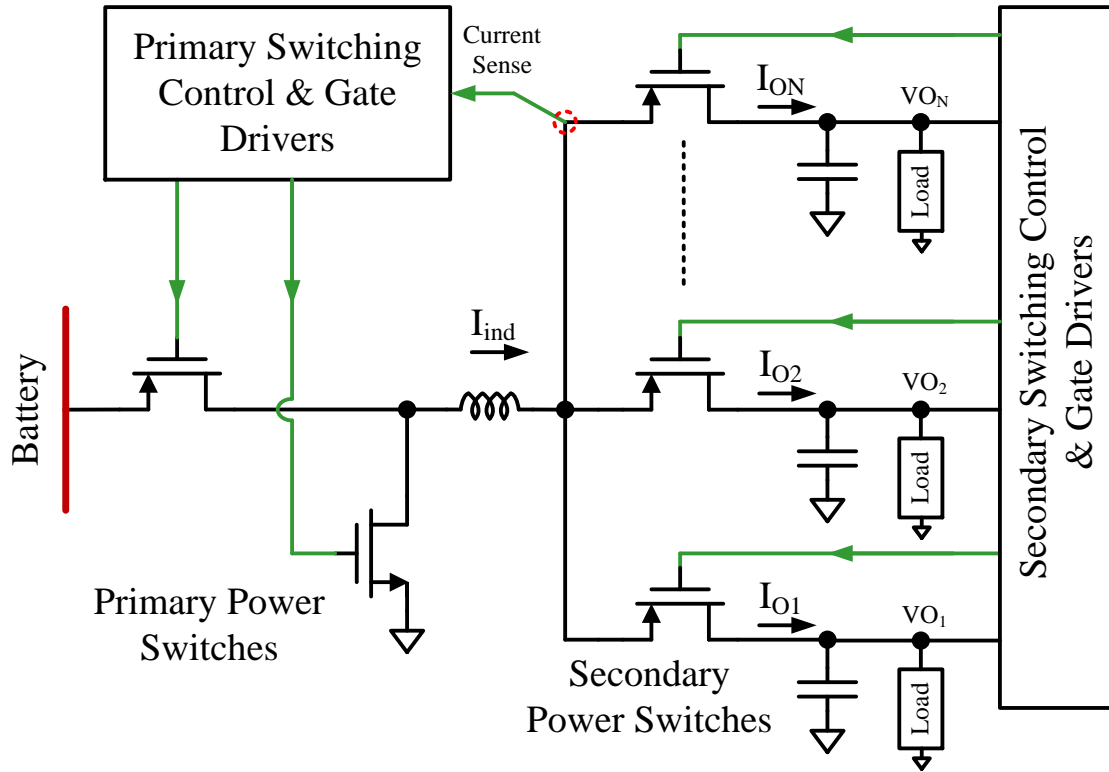


Figure 1.7. A block diagram of a typical SIMO power converter topology

1.4 Thesis Organization

The thesis is organized as follow:

Chapter 2 focuses on the theory of loss analysis of buck converter for low power nanometer CMOS applications. This chapter provides comprehensive analysis and modeling of switching and conduction losses in low-power synchronous buck regulators in both CCM and DCM modes of operation including the case with non-rail gate control of the power

FETs. The analysis takes into account losses that are typically ignored but become critical in low-power operation. It also considers the actual behavior of the regulator in DCM for loss modeling instead of common CCM-based approximations, which leads to more accurate estimation of losses. The provided comprehensive loss formulas can be used by designers to correctly optimize critical parameters in low-power buck regulators, such as the switching frequencies, sizes of the power FETs, realistic budgets for the parasitics associated with the passive components as well as the package so as to achieve the best possible efficiency. The theoretical formulas are verified against an actual buck regulator design implemented in 90nm CMOS technology.

Chapter 3 discusses a fully-integrated buck regulator with on-chip passives in 65nm standard CMOS technology is presented [36]. The proposed regulator switches at 588MHz and uses a 20nH on-chip inductor and a 300pF on-chip output capacitor. It operates from 1.8V input and produces an output in the range between 0.8V to 1.2V with maximum load current of 30mA. In order to reduce the large silicon area overhead of the on-chip inductor, the proposed design employs circuit stuffing where the entire regulator's circuitry is implemented directly underneath the inductor. This includes the input and output capacitance, power train, and control circuits. Thus, the total area of the regulator becomes essentially the area of the on-chip inductor itself, which cuts the regulator's footprint by 50%. Moreover, the proposed regulator employs a self-regulation loop that improves its overall efficiency and ensures the reliability of its low-voltage power transistors while operating from a 1.8V input. The regulator occupies 0.12mm^2 with a peak efficiency of 60%, and achieves up to 13.7% better efficiency than a corresponding LDO. It achieves fast settling

time of 240ns for a 200mV output voltage step, and as short as 40ns for a 20mA load current step.

Chapter 4 presents a 40mA buck regulator operating in the inherently stable Discontinuous Conduction Mode (DCM) for the entire load range is presented [37]. A Pulse Frequency Modulation (PFM) control scheme is implemented using a proposed Hysteretic-Assisted Adaptive Minimum On-Time (HA-AMOT) controller to automatically adapt the regulator to a wide range of operating scenarios in terms of input, output, and passive component values while ensuring compensation-less DCM operation with minimized inductor peak current. Thus, compact silicon area, low quiescent current, high efficiency, and robust performance across all possible scenarios can be achieved without any calibration. Moreover, power-gating is employed in the analog circuits of the proposed controller to further improve efficiency at sub-1mA loads. The regulator is integrated within a low-power microcontroller in 90nm CMOS to power its digital core while allowing maximum flexibility in the powering options of the microcontroller and the choice of the passive components. It occupies 0.1mm^2 and achieves 92% peak efficiency, and 78.5% and 86% efficiency at 200 μA and 40mA loads respectively. It handles an input in the range of 1.8V-4.2V, an output in the range of 0.9V-1.4V, an inductor in the range of 4.7 μH -10 μH , and an output capacitor in the range of 2.2 μF -10 μF without any calibration or re-optimization. The whole thesis concludes in chapter 5 while some new ideas regarding fully integrated DC-DC buck converters are proposed.

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CHAPTER II. ANALYSIS AND MODELING OF LOSSES IN LOW-POWER BUCK REGULATORS

Buck regulators are becoming very popular in low-power System-on-Chip (SoCs), such as microcontrollers, due to their high power conversion efficiency compared to linear counterparts [1]. In these types of SoCs, the maximum load current of the buck regulator is typically less than 50mA, with an output voltage between 0.9V and 1.4V [2]. With such low output power and voltage levels, achieving high efficiency requires careful estimation of the various forms of losses in order to determine the power FET device type and size, the switching frequency, the acceptable accuracy of the passive components, and the routing and package parasitics that can be tolerated. Although several classic loss formulas are readily available in the literature for that purpose [3-5], they are either oversimplified or geared towards high-power high-voltage designs. Thus, they often ignore factors that can be critical in low-power low-voltage designs. For instance, it is common to ignore losses such as transitional losses in the power FETs and dead-time (non-overlap time) body-diode losses. Moreover, since low-power SoCs are usually implemented in low-voltage nanometer CMOS, the buck regulator is typically operated from input voltages that may exceed the gate-to-source voltage rating of its power FETs, and thus, non-rail gate switching using intermediate voltage levels must be employed to preserve device reliability [6], which renders the classic loss formulas inaccurate since they assume rail-to-rail gate switching. Furthermore, with maximum load current of less than 50mA, the regulator operates in DCM most of the time [2], and therefore, using the common CCM-based loss formulas becomes overly pessimistic, and alternative formulas that consider actual DCM operation become necessary for accurate estimation of losses [8]. Additionally, it is also common to simplify gate-drive losses of the

power FETs assuming a lumped gate capacitance without differentiating between C_{gs} (gate-to-source capacitance) and C_{gd} (gate-to-drain capacitance), and ignoring how charging/discharging these parasitic capacitors may change other forms of losses such as transitional and conduction losses in the power FETs. While all the above simplifications and omissions can be appropriate for optimizing high-power high-voltage designs, they can lead to significantly sub-optimal design in low-power applications.

In this chapter, the critical components of switching and conduction losses are studied taking the aforementioned factors into consideration. The loss formulas are derived for the CCM and DCM cases separately assuming non-rail gate switching for the sake of generality, but can also be reduced to cover rail-to-rail gate drive as a special case. The formulas can be used for optimizing buck regulators for the best efficiency and aid with determining the dominant loss mechanisms that must be reduced. The paper is organized as follows: chapter 2.1 and 2.2 study the different switching and conduction loss mechanisms and derive the loss formulas in both CCM and DCM, while chapter 2.3 compares the losses estimated by these formulas to the simulated losses in a buck regulator design in 90nm CMOS. Chapter 2.4 concludes this part of the thesis.

In order to analyze the different losses, the block diagram of a typical buck regulator operating with a switching period T_s , input and output voltages V_{IN} and V_O respectively is shown in Fig. 2.1(a), including all the parasitics critical for losses. The parasitics include the routing and package pin resistances associated with the low-side and high-side power FETs, which are denoted as R_{pls} and R_{phs} respectively; the routing and package pin resistances associated with the switching node, which is denoted as R_{psw} ; and the parasitic resistance associated with the off-chip inductor and capacitor, which are denoted as R_{ind} and R_{esr}

respectively. The figure also shows the gate-to-source and gate-to-drain capacitances associated with the power FETs, the body-diode associated with the low-side power FET, as well as the total parasitic capacitance associated with the switching node. The special symbols used for the power FETs are to emphasize the case where drain-extended power FETs in nanometer CMOS technologies are used to handle high voltage levels across their drain-source terminals (for instance, 1.8V), while their gate-source voltage levels must continue to be restricted by the low-voltage rating of the FETs (for instance, 1.2V). Fig. 2.1(b) and 2.1(c) show the important voltage and current waveforms in the regulator in CCM and DCM modes respectively. The waveforms emphasize the non-rail gate control levels of the power FETs by showing the swing of the gate control signal V_{CP} of the high-side FET between V_{CP-min} and V_{IN} , while showing the swing of the gate control signal V_{CN} of the low-side FET between zero and V_{CN-max} . The waveforms also show the turn-on voltage V_D of the body-diode of the low-side power FET. This diode is turned on by the inductor current during the intentionally-inserted dead-time period T_d at which both the high-side and low-side FETs are kept in an off state to avoid any shoot-through current during transitions. The rise and fall times of all the gate control signals are assumed to be the same and are denoted as T_{tran} , while T_{on} and T_{off} denote the on-time of the high-side and low-side FETs respectively. It is worth noting that both T_{tran} and T_d are typically much smaller than T_{on} and T_{off} . In the DCM scenario in Fig. 2.1(c), the additional period of time at which the inductor current is zero and the low-side FET is turned off is denoted as T_{idle} . To distinguish between

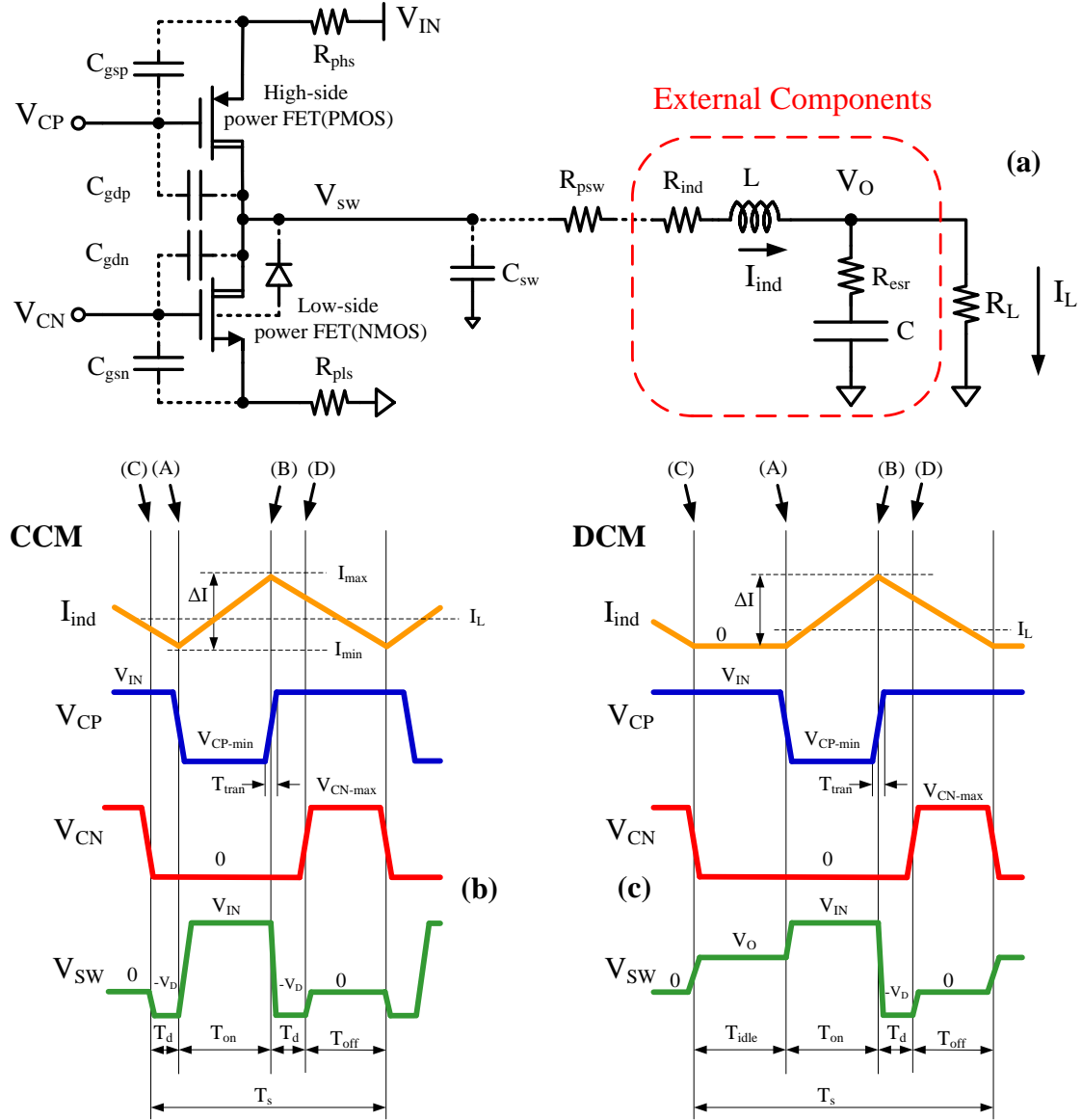


Figure 2.1. (a) A typical buck converter including critical parasitics, and important waveforms in (b) CCM operation, and (c) DCM operation.

the various switching events during the operation of the regulator, these events are denoted in Fig. 2.1(b) and Fig. 2.1(c) as events (A), (B), (C), and (D) for easy reference. Fig. 2.1 will be used frequently throughout the paper while analyzing the various switching and conduction losses.

2.1 Switching Losses Analysis

2.1.1 Transitional Losses

The first source of switching losses that will be considered is the transitional loss across the power FETs as they transition from a fully on state to a fully off state and vice versa. This loss happens due to the finite rise/fall time of the gate control signals of the FETs and occurs regardless of any switching node capacitance, i.e. it is not associated with charging and discharging the switching node capacitance C_{sw} . As shown in Fig. 2.1(a) in the CCM case and Fig. 2.1(b) in the DCM case, the transitional losses for the high-side power FET occur during events (A) and (B), while transitional losses for the low-side power FET occur during events (C) and (D). Fig. 2.2 shows a detailed plot of the control signal at the gate of each power FET along with the voltage across the FET and the current flowing through it during each one of the switching events noted in Fig. 2.1. However, for detailed analysis of transitions, each switching event in Fig. 2.1 is further sub-divided in Fig. 2.2 in order to distinguish between different segments within each transition. It is worth observing that since both T_{tran} and T_d are normally very short compared to the rate of change in the inductor current, it can be safely assumed that during both events (B) and (D) in Fig. 1 the inductor current stays constant at its peak value I_{max} , while during both events (A) and (C) the inductor current stays constant at its trough value I_{min} . Note that while Fig. 2.2 describes the CCM case, it can be used for the DCM case by simply assuming that I_{min} is zero. Starting with the high-side power FET in CCM, Fig. 2.2(a) shows the details of the transition from a fully-off state to a fully-on state (event (A) in Fig. 1(b)). In the first segment of the transition between (A1) and (A2), the gate control signal starts to drop while the FET

continues to be in an off state (the full inductor current continues to flow through the body-diode of the low-side power FET). The total voltage across the drain-source of the high-side FET is maintained at $V_{IN} + V_D$ with no current flow, and thus, no significant transitional losses are incurred across it. In the second segment of the transition between (A2) and (A3), the high-side FET starts to turn on and gradual exchange of current between the body-diode of the low-side FET and the high-side FET starts to take place. The current flow in the high-side FET can be approximated as a linear transition from zero to I_{min} , while the voltage across its drain-source continues to be $V_{IN} + V_D$ (since the diode is still conducting). Therefore, transitional losses will be incurred across the high-side FET during this segment and can be computed by integrating the product of the constant voltage across the FET and its approximately linear current waveform. In the third segment of the transition between (A3) and (A4), the high-side FET would be bearing the full inductor current I_{min} , and the body-diode of the low-side FET would be turned off. The drain-source voltage of the high-side FET starts to rapidly drop from $V_{IN} + V_D$ to almost zero (due to the low on-resistance of the high-side FET), and can be approximated as a linear transition. Thus, transitional losses will be incurred across the high-side FET during this segment and can be computed by integrating the product of the constant current through the FET and its approximately linear drain-source voltage waveform. In the fourth segment of the transition between (A4) and (A5), the high-side FET would be bearing the full inductor current with very small voltage across its drain-source. Losses across the FET in this segment are accounted for in the conduction losses in section III and are not considered part of the transitional losses.

Taking the above discussion into consideration, the total transitional losses in the high-side FET during event (A) take place between (A2) and (A4), and can be written as:

$$P_{\text{tran_HS_A}} = \frac{\lambda_p \times (V_{\text{IN}} + V_{\text{D}}) \times I_{\text{min}} \times T_{\text{tran}}}{2 \times T_s} \quad (2.1)$$

where λ_p is the ratio between the period from (A2) to (A4) and the total gate control transition period T_{tran} . Therefore the value of λ_p can be between 0 and 1. The actual value of λ_p is inversely proportional to the R_{dson} of the high-side FET, which is in turn determined by the FET size, the gate-to-source voltage of the FET when it is turned on, the process corner, and temperature. It is rather easy to determine λ_p through simulations for an existing design. However, since the purpose of the formulas derived in this paper is to aid with initial design decisions, λ_p may not be known in advance. The authors have found that setting λ_p initially to 0.5 is a good starting point for initial estimation of losses, and it can then be tweaked once an initial design is in place to yield more accurate estimation.

The previous analysis applies equally to event (B) shown in Fig. 2.2(b) as the high-side FET transitions from a fully-on to fully-off state, except that the current level is at I_{max} . Therefore, the transitional loss in event (B) can be written as:

$$P_{\text{tran_HS_B}} = \frac{\lambda_p \times (V_{\text{IN}} + V_{\text{D}}) \times I_{\text{max}} \times T_{\text{tran}}}{2 \times T_s} \quad (2.2)$$

Combining the transitional losses from events (A) and (B), and taking into account the relationship between I_{min} , I_{max} , and the load current I_{L} , the total transitional losses across the high-side FET during CCM operation can be written as:

$$P_{\text{tran_HS_CCM}} = \frac{\lambda_p \times (V_{\text{IN}} + V_{\text{D}}) \times I_{\text{L}} \times T_{\text{tran}}}{T_{\text{s}}} \quad (2.3)$$

For low-side FET, the turning on transitional profile during event (D) for CCM is shown in Fig. 2.2(c). The whole event starts from (D1) and ends at (D5). Since the voltage level of the switching node stays at $-V_{\text{D}}$ at the very beginning of (D1), once the gate voltage of the FET (V_{CN}) reaches $V_{\text{T}} - V_{\text{D}}$ at (D2), the FET turns on and it starts to take over the inductor current while the voltage across the FET stays at V_{D} . The loss can be computed by assuming a linear transition in the FET's current in this phase. Starting from event (D3), the FET turns into linear region and the voltage across the FET drops to zero until event (D4). During this phase, the loss can be computed by assuming a linear transition in switching node voltage. Therefore, the transitional loss due to turning on NMOS power FET at event (D) can be derived as:

$$P_{\text{tran_LS_D}} = \frac{\lambda_n \times V_{\text{D}} \times I_{\text{max}} \times T_{\text{tran}}}{2 \times T_{\text{s}}} \quad (2.4)$$

where $0 < \lambda_n < 1$ represent the ratio of the time between (D2) to (D4) over the whole event (D) duration. Again, the value of λ_n is proportional to the R_{dson} of the low-side FET. Note that for low threshold voltage technology, having a diode voltage across the gate and switching node is enough to convert the channel to weak or moderate inversion region. In this scenario, the NMOS channel and its body-diode will provide current simultaneously during the dead-time. Although the transition profile is different comparing to Fig. 2.2(c), a similar conclusion for transitional loss can be derived by applying the same analysis.

The turning off transition of low-side FET during event (C) can be referred to Fig. 2.2(d). The same analysis can be applied to compute the loss during this event and the transitional loss equations are:

$$P_{\text{tran_LS_C}} = \frac{\lambda_n \times V_D \times I_{\text{min}} \times T_{\text{tran}}}{2 \times T_s} \quad (2.5)$$

Therefore, the total transitional loss for low-side power FET during CCM operation is:

$$P_{\text{tran_LS_CCM}} = \frac{\lambda_n \times V_D \times I_L \times T_{\text{tran}}}{T_s} \quad (2.6)$$

By adding equation (2.3) and (2.6), the total transitional loss for CCM operation can be derived as:

$$P_{\text{tran_CCM}} = \lambda \times \frac{(V_{\text{IN}} + 2 \times V_D) \times I_L \times T_{\text{tran}}}{T_s} \quad (2.7)$$

Where λ equals λ_n and λ_p due to the fact that high-side and low-side power FETs are typically sized as 2:1 ratio so that their on resistance (R_{dson}) will be equal to get the optimal efficiency.

For DCM scenarios, the transitional losses only occur during events (B) and (D). The conclusion can be derived by adding equation (2.2) and (2.4) replacing I_{max} with ΔI . Thus, the total transitional loss for DCM operation is:

$$P_{\text{tran_DCM}} = \lambda \times \frac{(V_{\text{IN}} + 2 \times V_{\text{D}}) \times \Delta I \times T_{\text{tran}}}{2 \times T_{\text{s}}} \quad (2.8)$$

Based on equation (2.7) and (2.8), the best way to reduce the transitional loss is to minimize T_{tran} . However, this will cause reliability and EMI issues for the switching regulator. Thus, T_{tran} is typically designed based on the trade-off between the efficiency and reliability requirement.

2.1.2 Gate & Switching Node Capacitance Losses Estimation

The second source of switching losses is the charging and discharging process of the gate and switching node capacitances of the power FETs. The traditional methodology to compute this kind of losses is based on the equation $\frac{1}{2} C (V_f - V_i)^2$, where V_i and V_f are the initial and final voltages across the capacitor and C is the actual capacitance value. However, this equation assumes the energy discharged on capacitor is 100% lost away and becomes invalid once multiple capacitors are interacting together with other types of losses. For example, the amount of energy discharged at the capacitors during turning on/off power FETs can be transferred to reduce the transitional losses. For this purpose, we will derive the formulas for all the losses during the switching event as a system. The total amount of loss $E_{\text{loss}} = E_{\text{in}} - E_{\text{out}} - (E_{\text{stored-f}} - E_{\text{stored-i}})$, where E_{in} and E_{out} represent the amount of energy injected/ejected in-to/out-of the system while $(E_{\text{stored-f}} - E_{\text{stored-i}})$ denotes the net change of energy stored in the system. Moreover, we assume the non-rail switching voltage

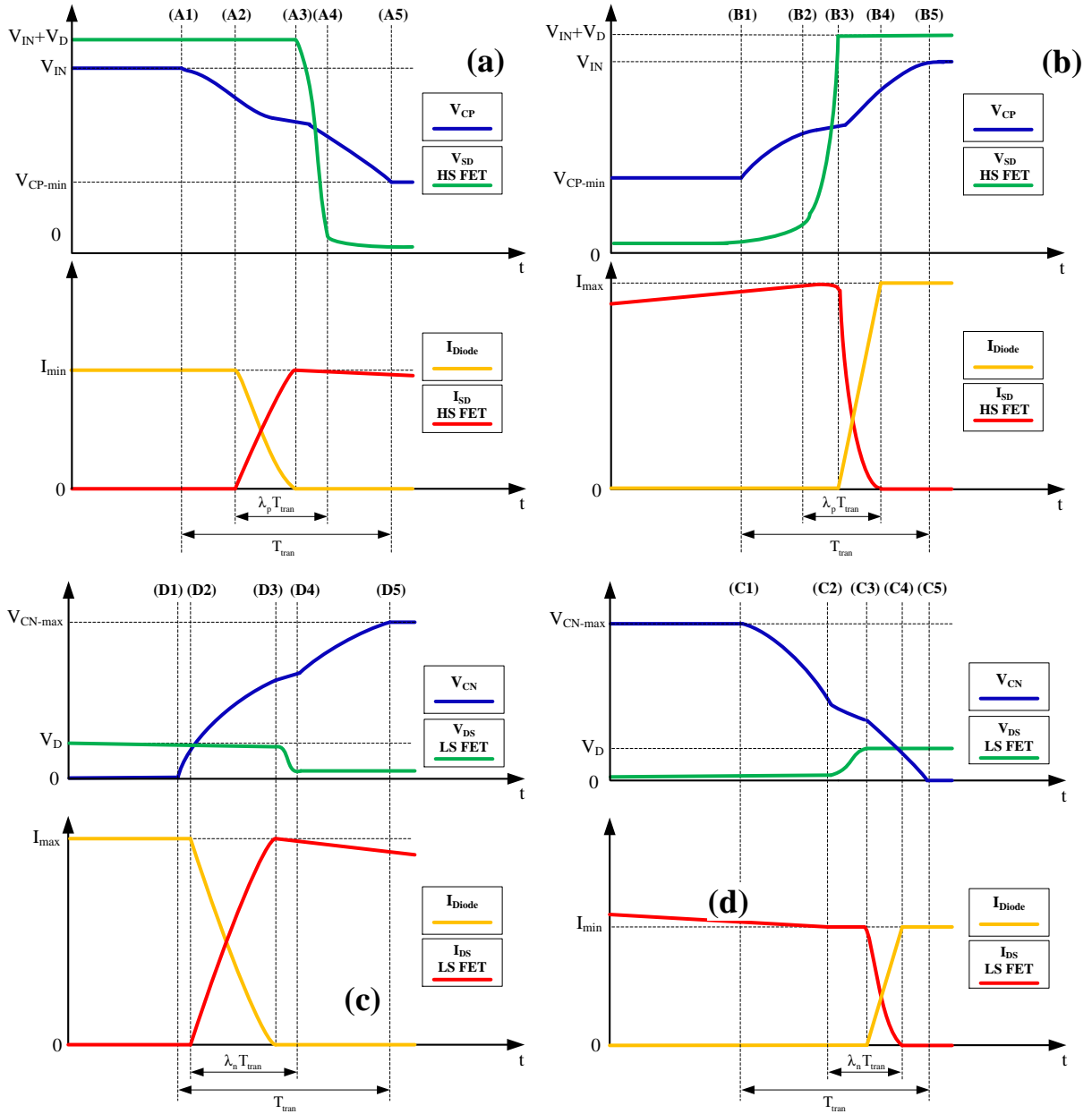


Figure 2.2. A plot of the control signal of each power FET along with the voltage and current across the FET's drain-source terminals during the switching events noted in Fig. 1: (a) high-side FET in event (A), (b) high-side FET in event (B), (c) low-side FET in event (D), and (d) low-side FET in event (C).

V_{gp} and V_{gn} are ideal power supplies so as to simplify the derivation. The detailed notifications can be referred to Fig. 2.4 and 2.5. The event by event charge flow plots for CCM scenarios are shown in Fig 2.4, where all the relevant capacitors per event are detailed as well as the current flow of the related capacitors during the event. And the equations for input, output and stored energy are listed at the right hand side of the each event plot. Note that t_i and t_f represents an initial and final time of the event and it is essentially the transitional time(T_{tran}) of the system.

During event (A) where the high-side FET is turning on, the voltage level of the gate of the high-side FET is discharging to V_{gp} while the switching node is getting charged to V_{in} . By plug in the initial and final voltage level across the FETs' capacitors in to the equations while understanding that $\int_{t_i}^{t_f} (V_{in} - V_{sw}) I_{ind} dt$ is the transitional loss calculated in the previous session. The total capacitive losses during event (A) can be derived as:

$$P_{cap_{ccm}}(A) = \frac{1}{2} \times f_s [C_{gsp} \times \Delta V_{CP}^2 + C_{gdp} \times (\Delta V_{CP} + V_{in} + V_{BD})^2 + C_{gdn} \times (V_{in} + V_{BD})^2 + C_{sw} \times (V_{in} + V_{BD})^2]$$

(2.9)

During event (B) where the high-side FET is turning off, the voltage level of the gate of the high-side FET is charging to V_{in} while the switching node is getting discharged to $-V_{BD}$. Based on the energy flow graph denoted on Fig 2.4 (b) and the energy equations listed, the same approach can be taken. The total capacitive losses during event (B) can be derived as:

$$P_{cap_{ccm}}(B) = \frac{1}{2} f_s [C_{gsp} \times \Delta V_{CP}^2 - C_{gdp} \times [(V_{in} + V_{BD})^2 - \Delta V_{CP}^2] - C_{gdn} \times$$

$$(V_{in} + V_{BD})^2 - C_{sw} \times (V_{in} + V_{BD})^2 \quad (2.10)$$

Note that the reason why switching loss are negative for C_{gdp} , C_{gdn} and C_{sw} is due to the fact that the energy discharged at the switching node is not lost but used to compensate part of the switching loss and transitional loss. This is demonstrated in the Fig 2.4(b) with green color as if the discharged energy is feeding back to the supply.

During event (C) where the low-side FET is turning off, the voltage level of the gate of the low-side FET is discharging to 0 while the switching node is getting discharged to $-V_{BD}$. The same practice can be done and the total capacitive losses during event (C) can be derived as:

$$P_{cap_{ccm}}(C) = \frac{1}{2} f_s [C_{gsn} \times \Delta V_{CN}^2 - C_{gdp} \times V_{BD}^2 + C_{gdn} \times (\Delta V_{CN}^2 - V_{BD}^2) - C_{sw} \times V_{BD}^2] \quad (2.11)$$

Note that the negative loss part is showing again the equation for the same reason as event (B).

During event (D) where the low-side FET is turning on, the voltage level of the gate of the low-side FET is charging to V_{gn} while the switching node is getting charged to zero. Based on the energy loss equations detailed in Fig 2.4(d), the total capacitive losses during event (D) can be derived as:

$$P_{cap_{ccm}}(D) = \frac{1}{2} f_s [C_{gsn} \times \Delta V_{CN}^2 + C_{gdp} \times V_{BD}^2 + C_{gdn} \times (\Delta V_{CN} - V_{BD})^2 + C_{sw} \times V_{BD}^2] \quad (2.12)$$

By combining the equation (2.9) to (2.12), the total capacitive losses in CCM can be derived as:

$$P_{cap_ccm} = f_s [C_{gsp} \times \Delta V_{CP}^2 + C_{gsn} \times \Delta V_{CN}^2 + C_{gdp} \times \Delta V_{CP} \times (\Delta V_{CP} + V_{in} + V_{BD}) + C_{gdn} \times \Delta V_{CN} \times (\Delta V_{CN} - V_{BD})] \quad (2.13)$$

One interesting point in equation (2.13) is the loss due to switching node capacitance is out of the equation. However, the switching node capacitance does affect the loss equation in the sense that higher switching node capacitance increases the turning on/off time of the FETs, which will increase the transitional loss of the system.

The capacitive switching loss for DCM can be analyzed with the same methodology and the detailed current flow per event can be referred to Fig 2.5. Note that only event (A) and (C) are illustrated in the figure due to the fact that the event (B) and (C) have the same charge flow diagram and loss equations as the CCM scenario.

During event (A) where the high-side FET is turning on, the same derivation can be applied as the CCM scenario while understanding the transitional loss is zero due to the fact that the inductor current is zero during the high-side FET turning on period. By referring to Fig 2.5(a) and apply some derivations, the capacitive switching loss in event (A) can be arrived as:

$$P_{cap_dcm}(A) = \frac{1}{2} f_s [C_{gsp} \times \Delta V_{CP}^2 + C_{gdp} \times (\Delta V_{CP} + V_{in} - V_o)^2 + C_{gdn} \times (V_{in} - V_o)^2 + C_{sw} \times (V_{in} + V_o)^2] \quad (2.14)$$

During event (C) where the low-side FET is turning off in DCM scenario, the inductor current will stay at zero while the switching node oscillates until it settles to V_o . During this period, the extra energy needed for switching node to oscillate is provided by the output of the converter since both sides of the FETs are turned off. By referring to the equation listed in the figure and plug in the initial and final voltage level across the FETs' capacitors, the total capacitive losses during event (C) can be derived as:

$$P_{cap_dcm}(C) = \frac{1}{2}f_s[C_{gsn} \times \Delta V_{CN}^2 + C_{gdp} \times V_o^2 + C_{gdn}(\Delta V_{CN} + V_o)^2 + C_{sw} \times V_o^2] \quad (2.15)$$

By combining the equation (2.10), (2.11), (2.14) and (2.15), the total capacitive losses in DCM can be derived as:

$$P_{cap_dcm} = f_s[C_{gsn} \times \Delta V_{CP}^2 + C_{gsn} \times \Delta V_{CN}^2 + C_{gdp} \times \Delta V_{CP} \times (\Delta V_{CP} + V_{in} + V_{BD}) - C_{gdp} \times [(V_o + V_{BD})(\Delta V_{CP} + V_{in}) - V_o^2] + C_{gdn} \times [\Delta V_{CN} \times (\Delta V_{CN} - V_{BD})] + C_{gdn} \times [\Delta V_{CN}(\Delta V_{CN} + V_o) - (V_o + V_{BD})(V_{in} + V_{BD} - V_o)] - C_{sw} \times [V_{in}(V_o + V_{BD}) - V_o^2]] \quad (2.16)$$

Based on the equation, the increasing on switching node capacitance will lead to less capacitive loss. However, this does not count that the increased amount of capacitance will lead to more transitional loss, which will turn out increase the total amount of loss for the system.

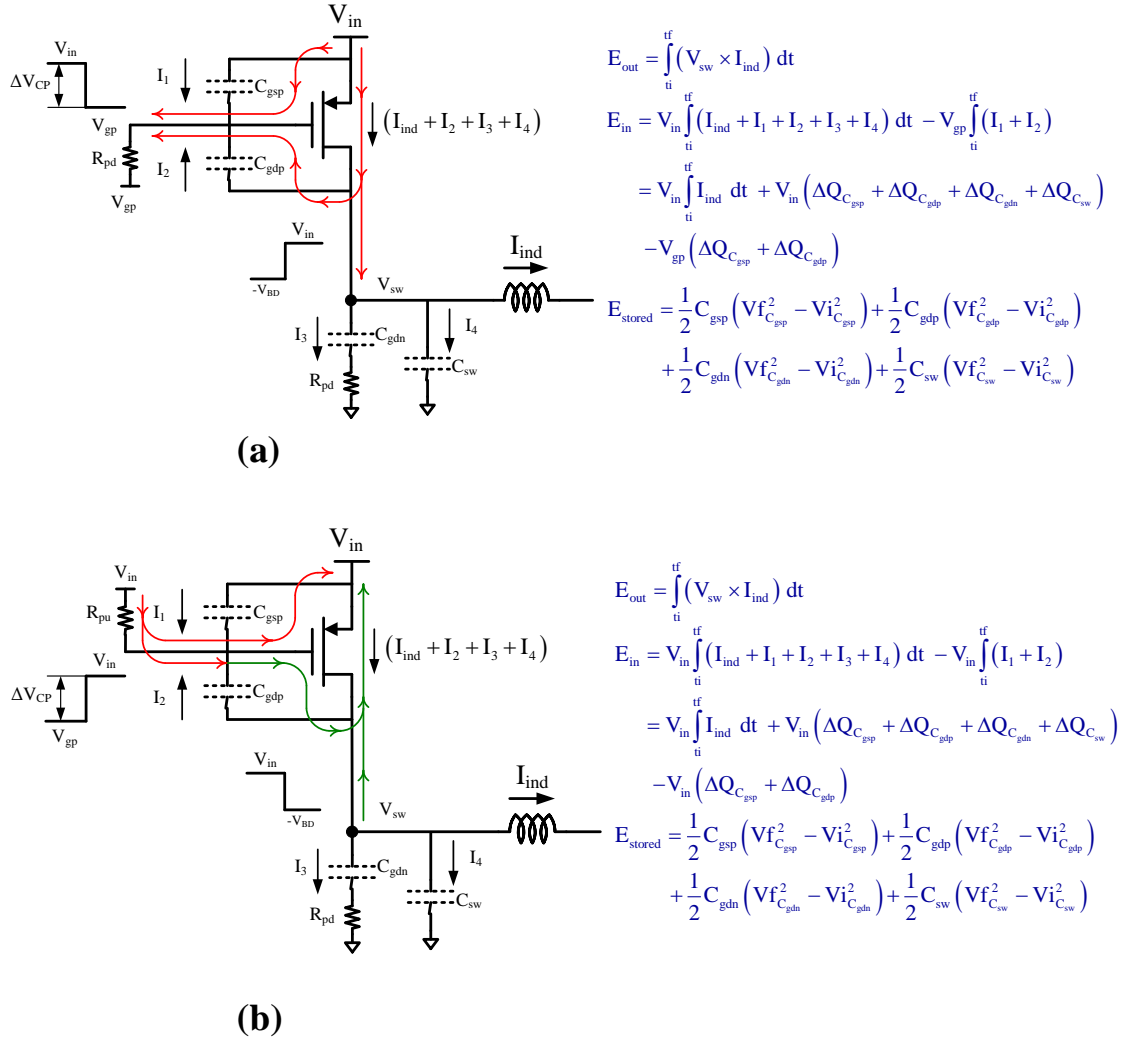


Figure 2.3. Charge flow diagrams and loss equation derivations for CCM operation for

(a) Event A (b) Event B

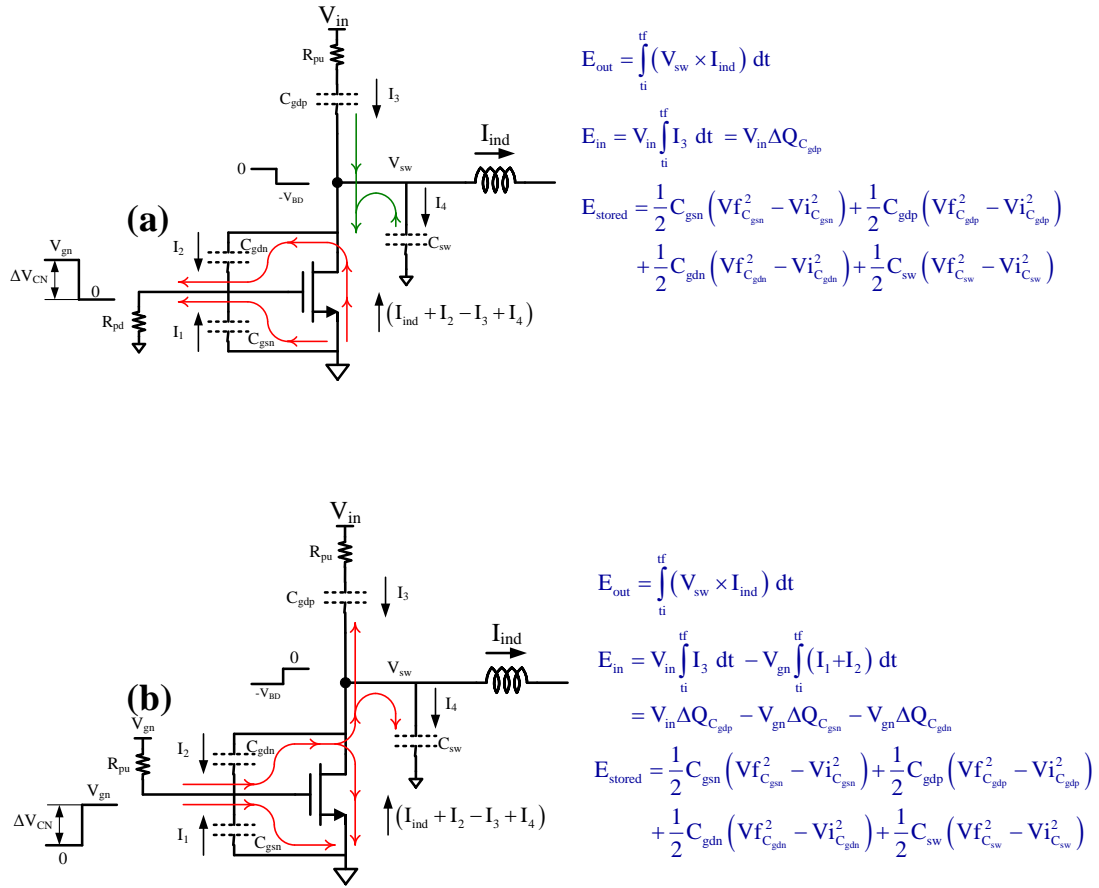


Figure 2.4. Charge flow diagrams and loss equation derivations for CCM operation for

(a) Event C (b) Event D

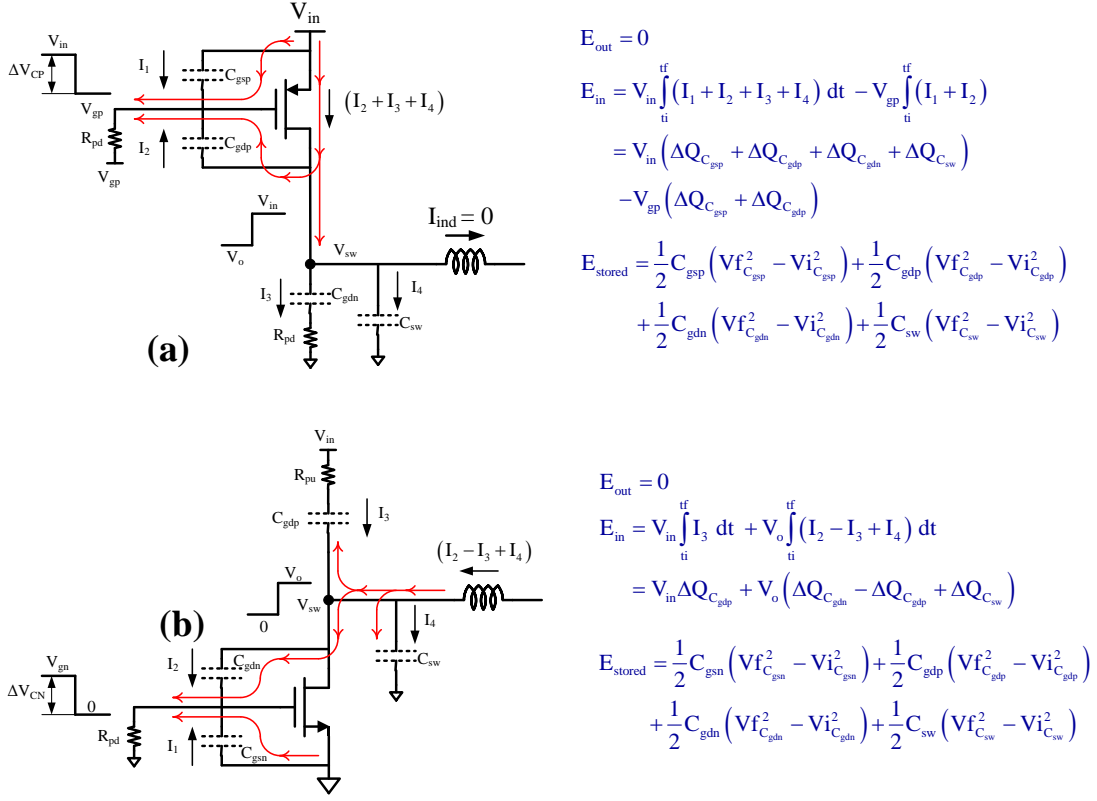


Figure 2.5. Charge flow diagrams and loss equation derivations for DCM operation for

(a) Event A (b) Event D

2.2 Conduction Losses Analysis

2.2.1 Power FETs Conduction Losses Estimation

The conduction losses across the high-side and low-side FETs are estimated only after the FETs have been completely turned on since transitional losses are already accounted for as part of the switching losses. For that purpose, the losses can be estimated as the integral of the square of the current flowing in the FET while it is on, multiplied by its on

resistance. Using the inductor current profile in Fig. 2.1, for CCM scenario, the loss across the high-side FET is $R_{dson-p} \left(I_L^2 + \frac{\Delta I^2}{12} \right) \left(\frac{T_{on}}{T_s} \right)$ while it is $R_{dson-n} \left(I_L^2 + \frac{\Delta I^2}{12} \right) \left(\frac{T_{off}}{T_s} \right)$ for the low-side FET. Combining these losses, and assuming that $R_{dson-p} \approx R_{dson-n} = R_{dson}$ (typically the case), and considering $T_s = T_{on} + T_{off}$, the total conduction loss can be written as:

$$P_{RFET_CCM} = R_{dson} \left(I_L^2 + \frac{\Delta I^2}{12} \right) \quad (2.20)$$

where I_L is the load current of the converter.

For switching regulators working in DCM scenario, the loss across the high-side FET is $R_{dson-p} \left(\frac{\Delta I^2}{3} \right) \left(\frac{T_{on}}{T_s} \right)$, while it is $R_{dson-n} \left(\frac{\Delta I^2}{3} \right) \left(\frac{T_{off}}{T_s} \right)$ for the low-side FET. Combining these losses and taking into account the relationship between T_{on} , T_{off} , and T_s in DCM operation, the total conduction loss due to power FET can be derived as:

$$P_{RFET_DCM} = R_{dson} \left(\frac{2 \times \Delta I \times I_L}{3} \right) \quad (2.21)$$

2.2.2 Parasitics Conduction Losses Estimation

Depending on the cost of the regulator, the resistive loss due to the parasitic can take a relative substantial portion of the total losses. The resistive parasitic associated with power switches is shown in Fig 2.1(a). The conduction loss due to bond-wire/lead-frame at

supply/ground can be computed by replacing R_{dson} with R_{phs} and R_{pls} in Eq. (2.5) and (2.6). The conduction losses due to bond-wire/lead-frame resistance at switching node and across the parasitic resistance of the inductor can be combined and estimated considering that $R_{psw} + R_{ind}$ experiences the full inductor current for the full switching period. And the equivalent series resistance (R_{esr}) of the external capacitor experiences only the difference between the inductor current and the load current. Assuming that $R_{phs} = R_{pls} = R_{psw} = R_p$, the two losses can be combined and written as:

$$P_{Para_CCM} = (2R_p + R_{ind}) \left(I_L^2 + \frac{\Delta I^2}{12} \right) + R_{esr} \times \frac{\Delta I^2}{12} \quad (2.22)$$

$$P_{Para_DCM} = (2R_p + R_{ind} + R_{esr}) \left(\frac{2 \times \Delta I \times I_L}{3} \right) - R_{esr} \times I_L^2 \quad (2.23)$$

Comparing Eq (2.17)~(2.18) and (2.19)~(2.20), it is clear that parasitic resistive losses can add substantially amount of loss to the whole system since for a low cost package and inductor, the total of the parasitic resistance can be comparable to the R_{dson} of the FETs.

2.2.3 Body-Diode Losses Estimation

The last source of conduction loss that will be discussed is the loss across the body-diode of the low-side FET during the dead-time period T_d . The first thing to observe is that as for CCM operation where this diode will turn on twice during the switching period (once at the beginning of T_{on} and another at the beginning of T_{off}), in DCM-only operation, it is turned on only once at the beginning of T_{off} since the inductor current is always zero at the begging of T_{on} in DCM operation. Taking that into account, and considering that the forward

voltage V_D of the diode is more or less constant, and that the inductor current is at its peak/valley, the loss across the diode for CCM and DCM can be written as:

$$P_{Diode_CCM} = V_D \times 2 \times I_L \times \left(\frac{T_d}{T_s}\right) \quad (2.24)$$

$$P_{Diode_DCM} = V_D \times \Delta I \times \left(\frac{T_d}{T_s}\right) \quad (2.25)$$

Note that since T_d is much shorter than the rate of current change in the inductor, the current flow in the diode is assumed to be constant during T_d . Moreover, since T_d is much shorter than T_s , this loss is typically rather small.

2.3 Simulation & Validation

To verify the correctness of the proposed formulas, the power stage of a buck regulator has been designed, including the driver stages and non-overlapping circuitries, with 3V transistors in 90nm CMOS technology. The high-side and low-side power FETs are sized as 2:1 ratio to keep the on resistance close(not that close in the technology not though). Note that the power FETs and drivers are sized differently for CCM and DCM scenarios to roughly balance the conduction and switching losses. To verify the correctness of the proposed formulas on all the scenarios, both the traditional rail-to-rail gate control and non-rail control drivers are designed for CCM and DCM scenarios. For non-rail gate control, the intermediate voltage is implemented as an ideal voltage source at half supply in this paper for

simplicity purpose. However, this can be easily replaced by a low cost LDO in actual design. The detailed information regarding the design parameters and parasitic values can be found in Table 2.1 for CCM scenario and Table 2.2 for DCM scenario.

Due to the complicity of the charge flow during the switching event, it is impossible to extract the exact capacitive switching losses and transitional losses separately during each of the event in simulation. Thus, the proposed methodology to get the total switching losses is to measure the total loss of the system first and subtract the conduction losses of each component (high-side and low-side FETs, diode, inductor DCR and parasitics), which can be acquired with simulation calculator (Cadence ADE calculator).

In order to fully justify the proposed formulas, simulations across different loads and switching frequencies have been completed and summarized. To imitate the most typical scenarios, the CCM operation is modeled as Pulse Width Modulation (PWM) mode. Three different switching frequencies (2MHz, 3MHz, 4MHz) have been simulated across load level of 100mA, 150mA, 200mA, 250mA, and 300mA. For DCM operation, since it is most commonly seen as the application for light load application. Thus, Constant On-Time (COT) architecture has been selected as the operation mode. Three different COT conditions (130nS, 205nS and 290nS High-side FET on time) have been simulated across a load level of 1mA, 5mA, 10mA, and 15mA. The reason for choosing the above conditions is to fully verify the correctness of the proposed formulas under different load level from conduction losses dominating the total losses to switching losses dominating the total losses. For each of the scenario described, both rail-to-rail gate control and non-rail gate control scenarios have been simulated.

For each of the conditions mentioned above, the total conduction losses, switching losses and efficiency have been extracted with Cadence Virtuoso calculator and compared with the calculation results based on the proposed formulas. And the error in percentage is calculated based on:

$$Error = \left| \frac{Calculation - Simulation}{Simulation} \right| \times 100\% \quad (2.26)$$

The comparison between the calculated and simulated conduction losses and switching losses in CCM scenario with different switching frequencies with rail-to-rail gate control has been shown in Fig. 2.8. And the efficiency comparison is detailed in Fig 2.6(a). Based on the plot, the worst case difference between calculation and simulation for conduction loss is less than 6.2%, while the worst case switching loss discrepancy between calculation and simulation is 6.3%. Based on the plot, it can be observed that there is a slight overestimate on switching losses and underestimate on conduction losses with load increasing. This is due to the fact that the diode voltage is a weak function of FET's current (increase with load current) while λ is slightly inversely proportional to FET's current. In the calculation, the author uses the typical diode voltage as 750mV while T_{tran} and λ are only correlated with the simulation at minimum load and the same value are used for the higher load current calculation. This will lead to some overestimation on transitional losses and some underestimation on diode losses. However, the two discrepancies can somehow compensate with each other depending on the dominance of the loss across the load, which lead to the fact that the total efficiency discrepancy between the simulation and calculation is less than 0.18%. Although this can not 100% justify the accuracy of the proposed formulas,

the author consider this methodology is valid since in most of the actual design scenarios, the loss calculation is only the starting point of the design which serves the purpose of finding the optimum operating point and which part of the loss is dominating the total amount of loss. Thus, having typical values as some of the design parameters follows actual usage of the formulas while still getting considerable amount of insight.

Table 2.1 Design parameters for CCM scenario

$V_{IN}(V)$	$V_O(V)$	$L(\mu H)$	$C(\mu F)$	$R_{phs}, R_{pls}, R_{psw}(m\Omega)$	$R_{ind}(m\Omega)$	$R_{esr}(m\Omega)$
3	1.2	4.7	2.2	50	50	30
High-side FET		Low-side FET		High-side FET R_{ds-on}	Low-side FET R_{ds-on}	
$R_{ds-on}(\Omega)$		$R_{ds-on}(\Omega)$		non-rail(Ω)	non-rail(Ω)	
0.125		0.065		0.269	0.131	

Table 2.2 Design parameters for DCM scenario

$V_{IN}(V)$	$V_O(V)$	$L(\mu H)$	$C(\mu F)$	$R_{phs}, R_{pls}, R_{psw}(m\Omega)$	$R_{ind}(m\Omega)$	$R_{esr}(m\Omega)$
3	1.2	4.7	2.2	100	100	30
High-side FET		Low-side FET		High-side FET R_{ds-on}	Low-side FET R_{ds-on}	
$R_{ds-on}(\Omega)$		$R_{ds-on}(\Omega)$		non-rail(Ω)	non-rail(Ω)	
0.375		0.197		0.807	0.394	

The comparison between the calculated and simulated conduction losses and switching losses in CCM scenario with different switching frequencies with non-rail gate control has been shown in Fig. 2.10. And the efficiency comparison is detailed in Fig. 2.7 (a). Based on the plot, the worst case difference between calculation and simulation for conduction loss is less than 8.1%, while the worst case switching loss discrepancy between calculation and simulation is 14.3%. The efficiency difference between the calculation and simulation is less than 1%. The reason for the discrepancy between the calculation and simulation is the same as it is described in the rail-to-rail CCM case.

For DCM scenario, the comparison between the calculated and simulated conduction losses and switching losses in rail-to-rail scenario with different high-side FET on time(T_{on}) has been shown in Fig. 2.9. And the efficiency comparison is detailed in Fig. 2.6(b). The worst case difference between calculation and simulation for conduction loss is less than 9.3%, while the worst case switching loss discrepancy between calculation and simulation is 12.1%. The discrepancy on efficiency between the calculation and simulation is less than 0.79%. Based on the plot, it can be observed that the underestimation and overestimation goes into the opposite way. The rationale behind is different: for COT architecture, the diode voltage and λ is constant across load since the peak inductor current is constant across load. Due to the fact that the IR drop due to the bond-wire parasitic is not considered in the first order calculation, for the same amount of T_{on} , the peak inductor current is slightly smaller in simulation than calculation, this causes the simulated system has higher switching frequency than the calculation by around 5% which will lead to higher switching losses and lower conduction losses in simulation.

The comparison between the calculated and simulated conduction losses and switching losses in DCM scenario with non-rail gate control has been shown in Fig. 2.11. And the efficiency comparison is detailed in Fig. 2.7(b). Based on the plot, the worst case difference between calculation and simulation for conduction loss is less than 12.9%, while the worst case switching loss discrepancy between calculation and simulation is 11.1%. The discrepancy on efficiency between the calculation and simulation is less than 0.63%. The reason for the discrepancy between the calculation and simulation is the same as it is described in the rail-to-rail DCM case.

To demonstrate the difference between the proposed formulas and the formulas illustrated in the state of the art buck regulator loss analysis[4-5]. The switching losses part is plotted with 2MHz, CCM scenario and rail-to-rail gate control in Fig. 2.12 with simulation results, the proposed calculation results and the calculation results based on[4-5]. The proposed formulas better tracks the simulation results by an average of 5.6%

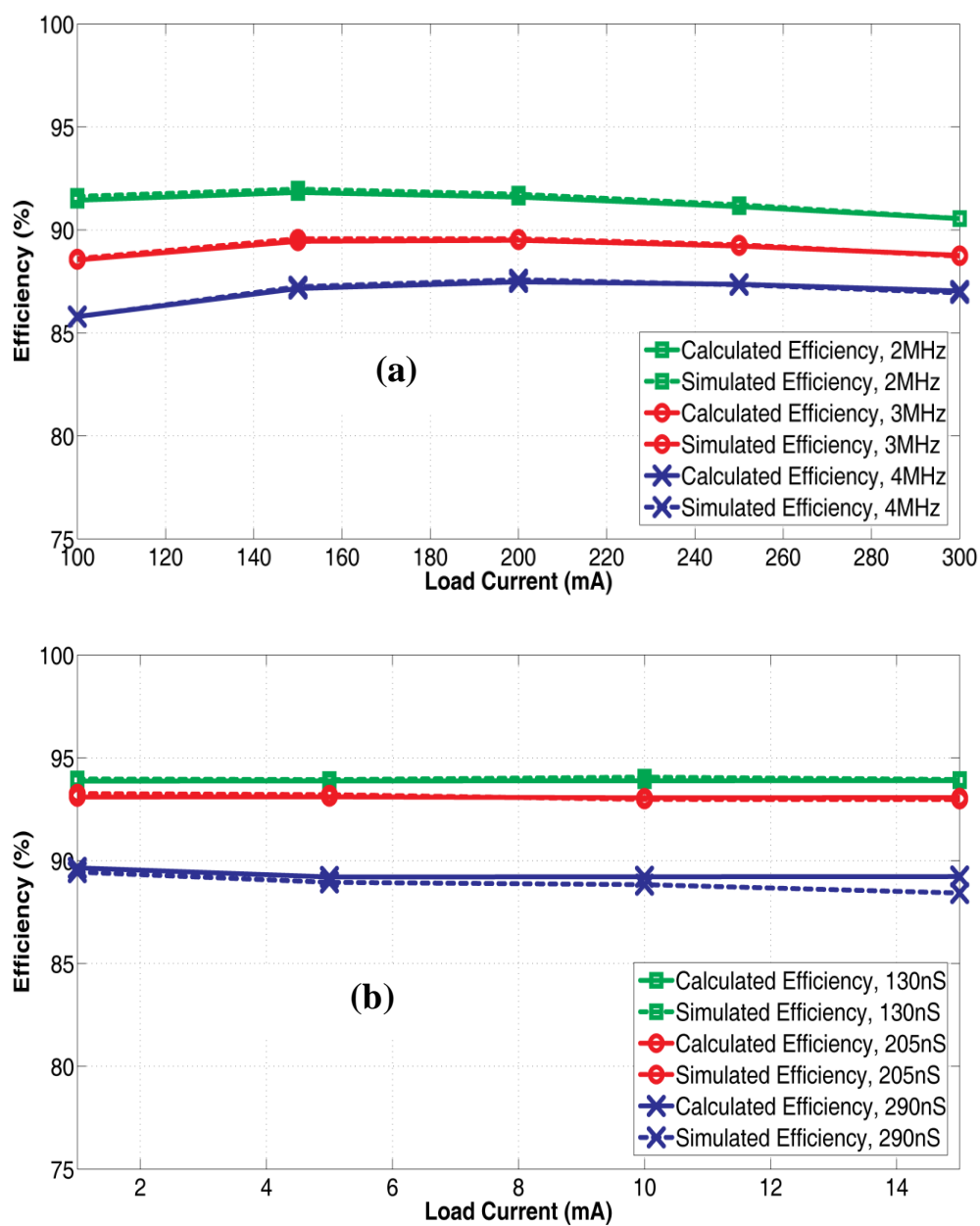


Figure 2.6. The comparison between calculated and simulated power conversion efficiency in CCM and DCM scenarios with rail-to-rail gate control (a) CCM (b) DCM

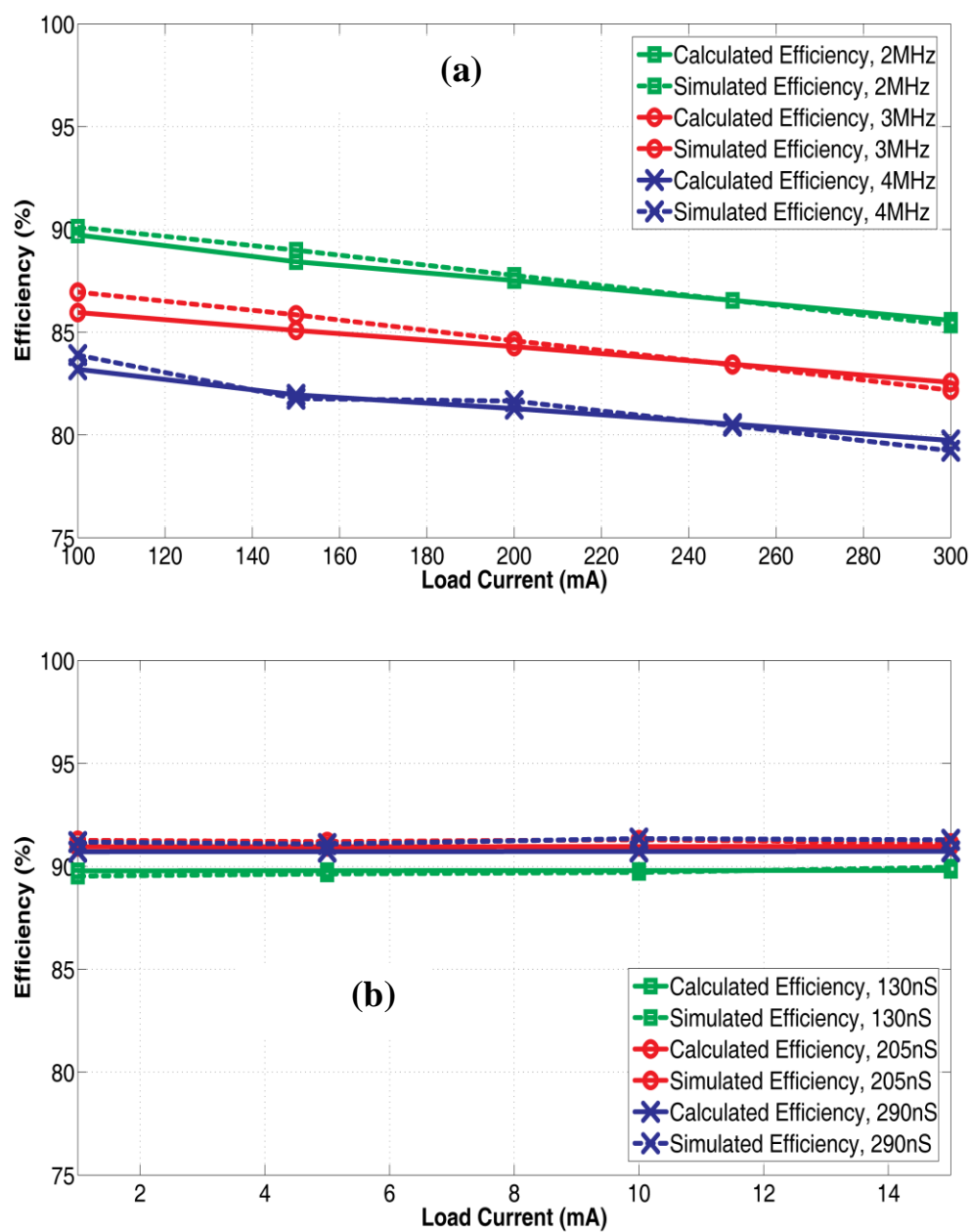


Figure 2.7. The comparison between calculated and simulated power conversion efficiency in CCM and DCM scenarios with non-rail gate control (a) CCM (b) DCM

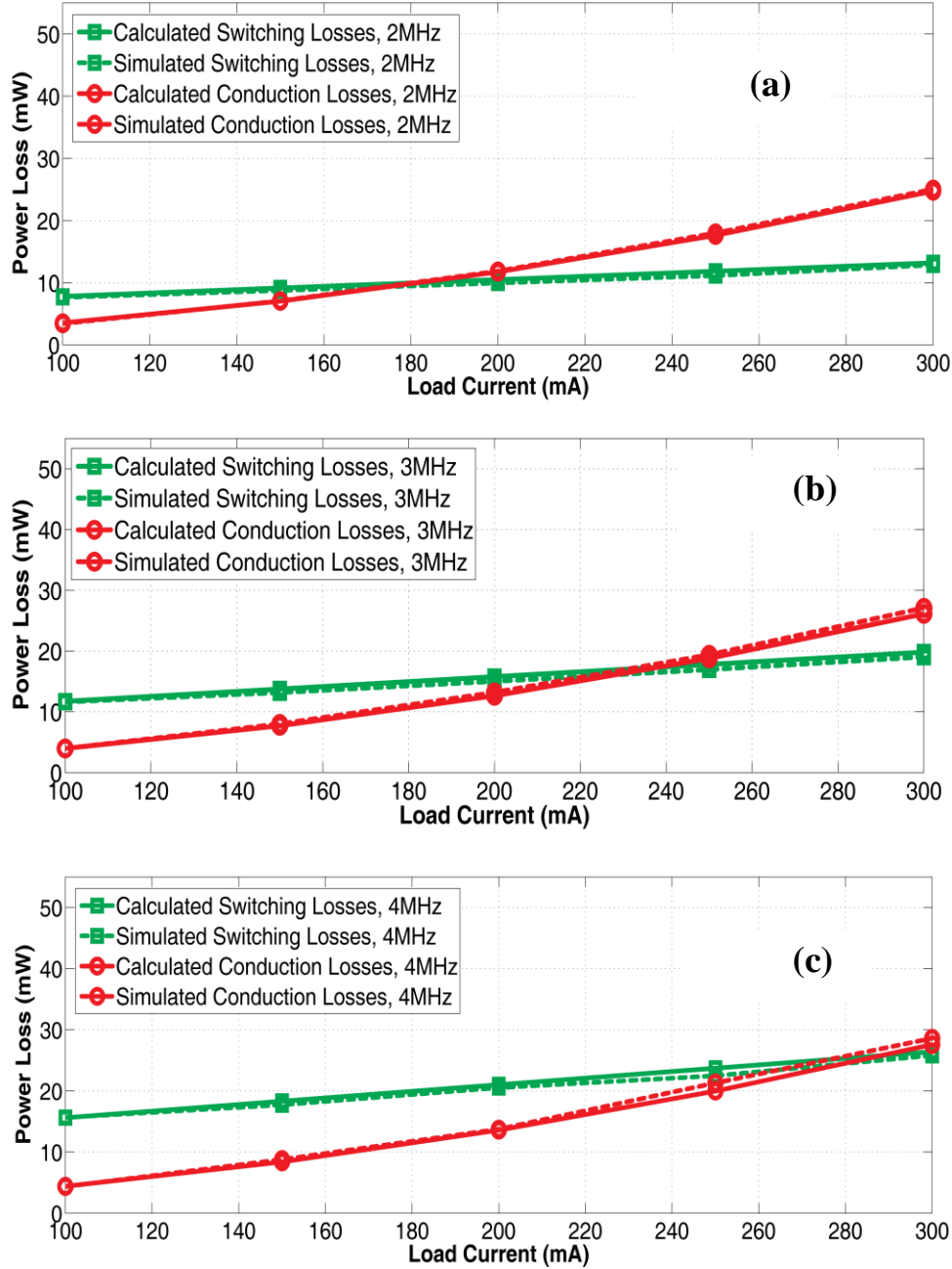


Figure 2.8. The comparison between calculated and simulated switching & conduction losses in CCM scenarios with rail-to-rail gate control: (a) CCM with 2MHz switching frequency (b) CCM with 3MHz switching frequency (c) CCM with 4MHz switching

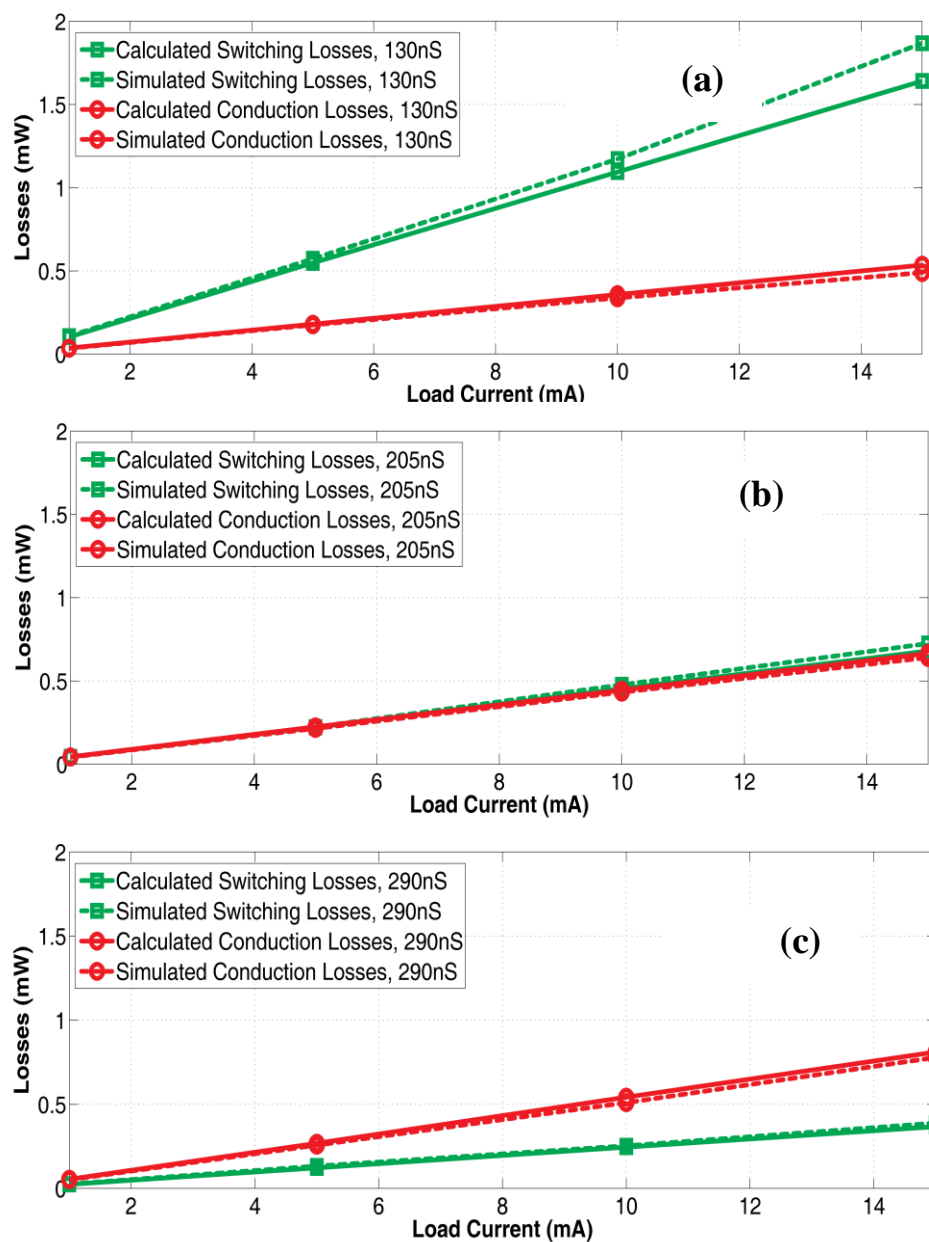


Figure 2.9. The comparison between calculated and simulated switching & conduction losses in DCM scenarios with rail-to-rail gate control: (a) DCM with 130nS Ton (b) DCM with 205nS Ton (c) DCM with 290nS Ton

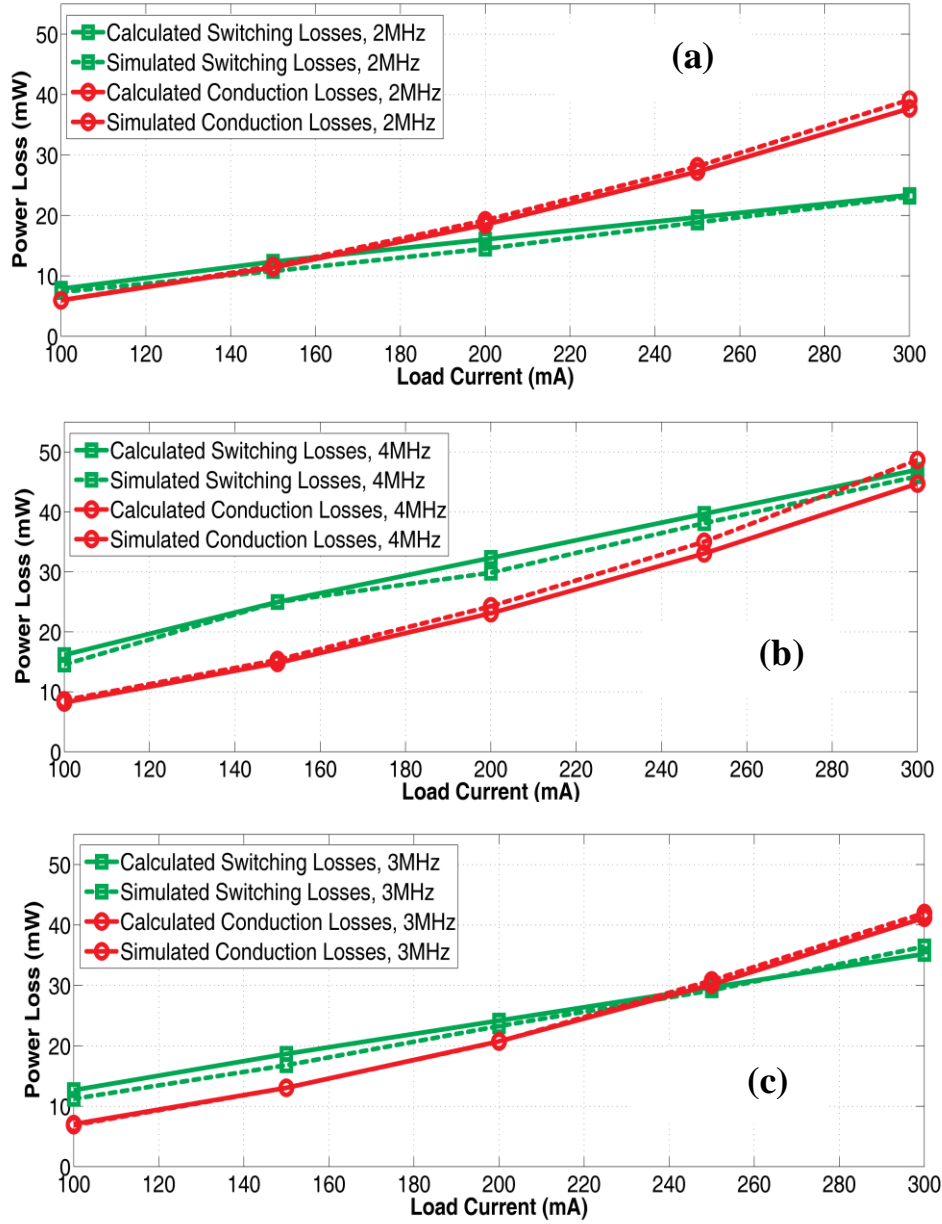


Figure 2.10. The comparison between calculated and simulated switching & conduction losses in CCM scenarios with non-rail gate control: (a) CCM with 2MHz switching frequency (b) CCM with 3MHz switching frequency (c) CCM with 4MHz switching

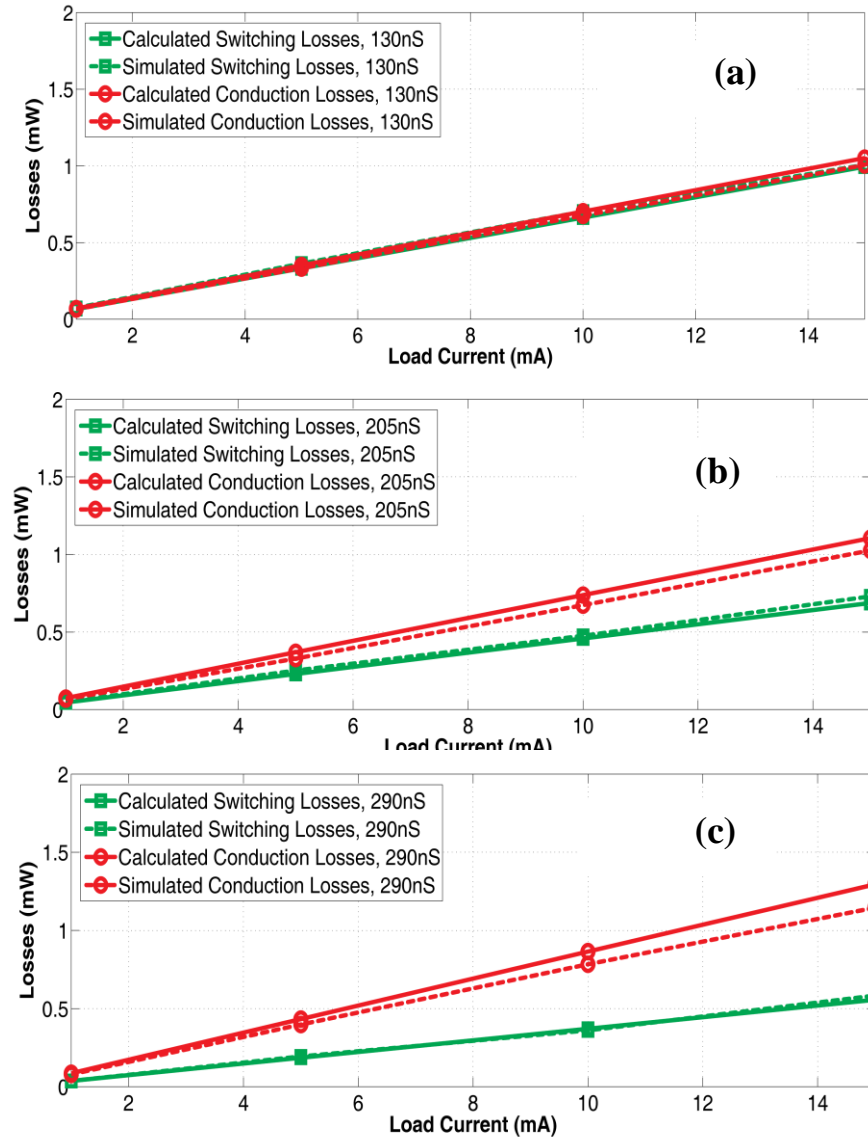


Figure 2.11. The comparison between calculated and simulated switching & conduction losses in DCM scenarios with non-rail gate control: (a) DCM with 130nS T_{on} (b) DCM with 205nS T_{on} (c) DCM with 290nS T_{on}

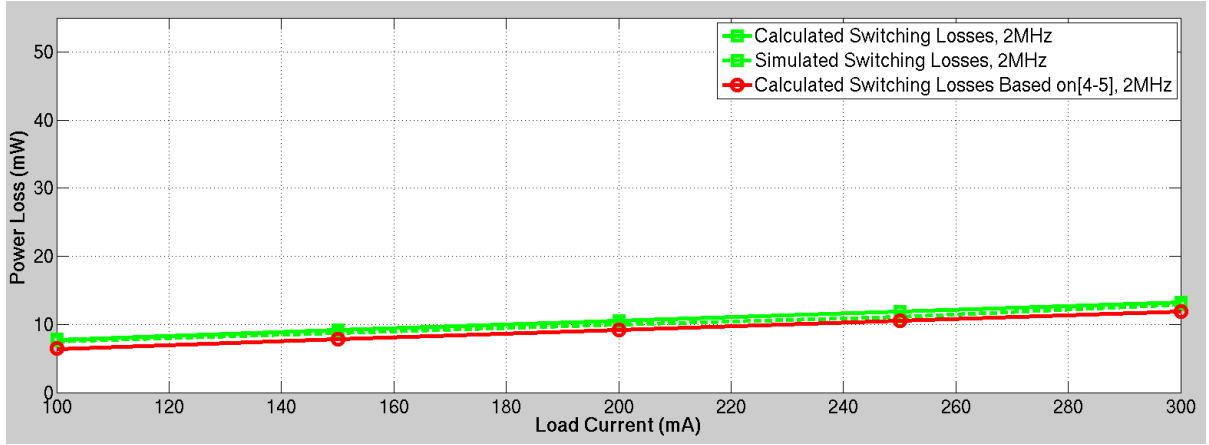


Figure 2.12. The comparison between calculated switching losses with proposed formulas in this thesis, calculated switching losses with formulas proposed in[4-5], simulated switching losses in CCM scenarios at 2MHz switching frequency.

2.4 Conclusion

This chapter presented the derivation of comprehensive formulas for estimating both switching and conduction losses in buck converters operating in CCM/DCM with rail-to-rail as well as non-rail gate control. The formulas can be used to correctly optimize the size of the power FETs as well as estimating the allowed budget for parasitics in order to achieve the best possible efficiency. The formulas have been verified via simulation results and comparison shows the proposed formulas are precise across all the difference scenarios regarding load/switching frequency variations.

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CHAPTER III. A FULLY-INTEGRATED BUCK REGULATOR WITH ON-CHIP PASSIVES AND CIRCUIT STUFFING

As it is discussed in chapter 1, nanometer CMOS mixed-signal SoCs require a large number of independent and well isolated power domains due to the demand for increasing the functional capabilities of these devices while reducing the power consumption and implementation size and cost. Currently, the most commonly-employed strategy in industry to generate multiple adaptive on-chip power supply domains is to use a single conventional switching regulator to generate a shared 1.8V power supply, followed by an array of fully-integrated linear regulators to generate all the necessary on-chip power supply domains. This strategy is particularly attractive in terms of cost as fully-integrated linear regulators require no off-chip passive components or package pins, which allows implementing as many of them as needed with little cost overhead. However, in terms of power efficiency, this strategy is sub-optimal since linear regulators have poor efficiency, particularly if the difference between the input and output voltage is large. In fact, generating 0.8V power supply from 1.8V input would entail only 44% efficiency. Therefore, for the digital loads operating from 1V or less power supply levels, the impact of this poor efficiency is quite significant.

In order to address this problem, there has been some research conducted on the feasibility of replacing these linear regulators with more efficient switching alternatives that employ only on on-chip components to avoid the additional cost associated with off-chip passives [1]. In fact, some recent work demonstrated inductor-based switching regulators with on-chip inductors [2-5], as well as capacitor-based switch-C regulators [6-7]. However, the architecture presented in [2] consumes 1.5mm^2 silicon area plus not able to solve the reliability issue mentioned above(e.g. 1.8V as the input level). The solution presented in [3]

requires SiGe process, which is not commonly used in high-volume, low-cost industrial application. The architecture detailed in [4,5] is able to achieve impressive efficiency. However, the solution requires bond-wire inductance as the power inductor of the regulator. Such a solution requires extra area on bond-pads as well as extra cost on the bonding process. Moreover, such architecture is only compatible with type of packages that contains relative high inductance(e.g. 3nH or above). Therefore, the type of packages(e.g. BGA) with less than 1nH bond-wire will not be compatible with the architecture.

In this chapter, we present a 588MHz switching regulator that employs only on-chip inductor and capacitors and is implemented in standard 65nm CMOS technology without any special process flow for on-chip passives. The presented regulator is designed to operate from a 1.8V input to generate an output that can be adapted between 0.8V to 1.2V and delivers a maximum of 30mA load current. The solution to each of the issues mentioned above will be discussed separately in the section of proposed architecture and circuit implementation.

3.1 Feasibility Analysis and Optimization

Before discussing buck regulator design, we need to understand the limitations and requirement to integrate the inductor and capacitor on silicon. By plug in the basic formulas for buck regulators, the minimum inductor value needed to maintain Continuous Conduction Mode(CCM) for a given input/output/load can be represented as[1]:

$$L_{min} = \frac{(1 - V_{OUT}/V_{IN}) \times V_{IN}}{2 \times f_s \times I_L} \quad (3.1)$$

Where V_{IN} and V_{OUT} is the input/output voltage of the regulator; f_s is the switching frequency of the regulator; and I_L is the load. Moreover, based on the choice made in eq. (3.1), the minimum capacitance required to maintain the output voltage ripple is:

$$C_{min} = \frac{1}{8 \times f_s \times \left(\frac{V_{ripple}}{2 \times I_L} - R_{ESR} \right)} \quad (3.2)$$

Where R_{ESR} is the Effective Series Resistance(ESR) of the output capacitance. Note that for both on chip capacitors and modern multi-layer ceramic capacitors, the ESR is typically small enough to be neglected(e.g. around 10m Ohm) during the ripple calculation.

Due to the inversely proportional relationship between passive components and switching frequency in eq. (3.1) and eq. (3.2), increasing the switching frequency of the buck regulator is the most effective method for reducing the size of the passive components and particularly that of the inductor. However, this is rarely used in traditional analog power CMOS technologies due to the large feature size and high threshold voltage of transistors in these technologies. In order to maintain the high efficiency for the converters, the most commonly seen buck regulators have been using switching frequencies limited to the range of 0.5Mhz to 4Mhz[8].

The recent nanometer CMOS technologies provide good opportunities to power converters to increase the switching frequency while maintain the same efficiency. This is due to the fact that nanometer CMOS technologies have transistors with smaller feature size and low threshold voltage.

In order to verify the feasibility of implementing the fully integrated buck regulator with nanometer CMOS technologies, the two major components of power losses in the power transistors are considered: switching loss and conduction loss[8]:

$$P_{loss} = C_{eq} \times V_{IN}^2 \times f_s + \left(I_L^2 + \frac{\Delta I^2}{12} \right) \times R_{ON} \quad (3.3)$$

$$R_{ON} = \frac{L}{\mu \times C_{ox} \times W \times (V_{gs} - V_T)} \quad (3.4)$$

$$C_{eq} = \alpha \times W \times L \times C_{ox} \quad (3.5)$$

Where C_{eq} is the total equivalent capacitance at the gate of transistor while α is the ratio factor; ΔI is the peak to peak inductor current and R_{ON} is the “on” resistance of the power transistor. Here we assume the high-side and low-side power transistors are sized around 2: 1 so there R_{ON} can be considered the same for both power transistors. The Table 3.1 shows a power loss comparison between 0.35 μ m and 65nm technologies assuming the same input, output, load condition, and most importantly the same R_{ON} to ensure the same conduction losses. By refereeing to the table, the switching frequency in the 65nm process can be

increased by a factor of 60 while maintaining the same power conversion efficiency. Thus, the on-chip inductor size can be reduced to 10nH~20nH with operating frequency around 60MHz to 180MHz.

Table 3.1. Loss and passive components comparison between 0.35 μ m and 65nm technologies

Technology	0.35 μ m	65nm
Threshold Voltage	1.1V	0.4V
Feature Size	0.35 μ m	65 m
Switching frequency for same power loss(assume $V_{IN} = 1.8$ V)	Typical 1~3Mhz	60~180MHz
Passive Components	2.2uH,1uF	20nH, 5nF

In order to calculate the optimized operating point of the regulator, we first plug $V_{IN} = 1.8V$, $V_{OUT} = 0.9V$ in eq. (3.1) while assuming we can maintain CCM operation for the regulator under the minimum load condition at 20 mA. Therefore, the relationship between the minimum inductor required and switching frequency can be computed as:

$$f_s \times L \geq 11.25 \text{ Hz} \times H \quad (3.6)$$

The above equation confirms the inverse relationship between the switching frequency and the inductor. By choosing the optimized switching frequency, we can calculate the size of the power FET of the regulator so as to achieve the best efficiency. Moreover, since the on-chip inductor typically has relative low Q than the off-chip ones, the parasitic resistor associated with the inductor also needs to be taken into account as part of the loss formulas. Another design boundary for choosing the optimized inductor value is, if the inductor size is too large,

the area overhead comparing to the linear regulator will massively reduce the attractiveness of the solution; if the inductor size is chosen to be too small, the very high switching frequency(e.g. beyond 1 GHz) loop design will be very tough and less robust. By assuming the parasitic resistor associated with the on-chip inductor is roughly 0.5 Ohm/nH, we can plug in the parameter into the eq. 2.X. and eq. 2.X. to compute the conduction losses and switching losses of the proposed regulator:

$$P_{loss_cond} = \left(I_L^2 + \frac{\Delta I^2}{12} \right) \times (R_{ON} + R_{ind}) \quad (3.7)$$

$$P_{loss_sw} = C_{eq} \times V_{IN}^2 \times f_s \quad (3.8)$$

$$R_{ind} = \frac{6}{f_s} \times 10^8 \quad (3.9)$$

By plug in eq. (3.9) into eq. (3.7) and combine eq. (3.7) and eq. (3.8), the total loss of the regulator can be derived as:

$$P_{loss} = \left(I_L^2 + \frac{\Delta I^2}{12} \right) \times \left(R_{ON} + \frac{6}{f_s} \times 10^8 \right) + C_{eq} \times V_{IN}^2 \times f_s \quad (3.10)$$

Here the value of R_{ON} and C_{eq} is determined by how the high-side and low-side power FETs are sized and typically, these two parameter is inversely proportional to each other. Thus, the total loss for a specific load will be a function of switching frequency and the size of the power FET. By assuming we can always find the optimum size of the power FETs at a specific load. The plot for total loss versus frequency at 20mA with optimized power FETs

size is shown in Fig. (3.1). Note that the calculation is based on the assumption that the power FETs will be cascaded. Thus, the switching loss formula will not be rail-to-rail switching formula expressed in eq. (3.10).

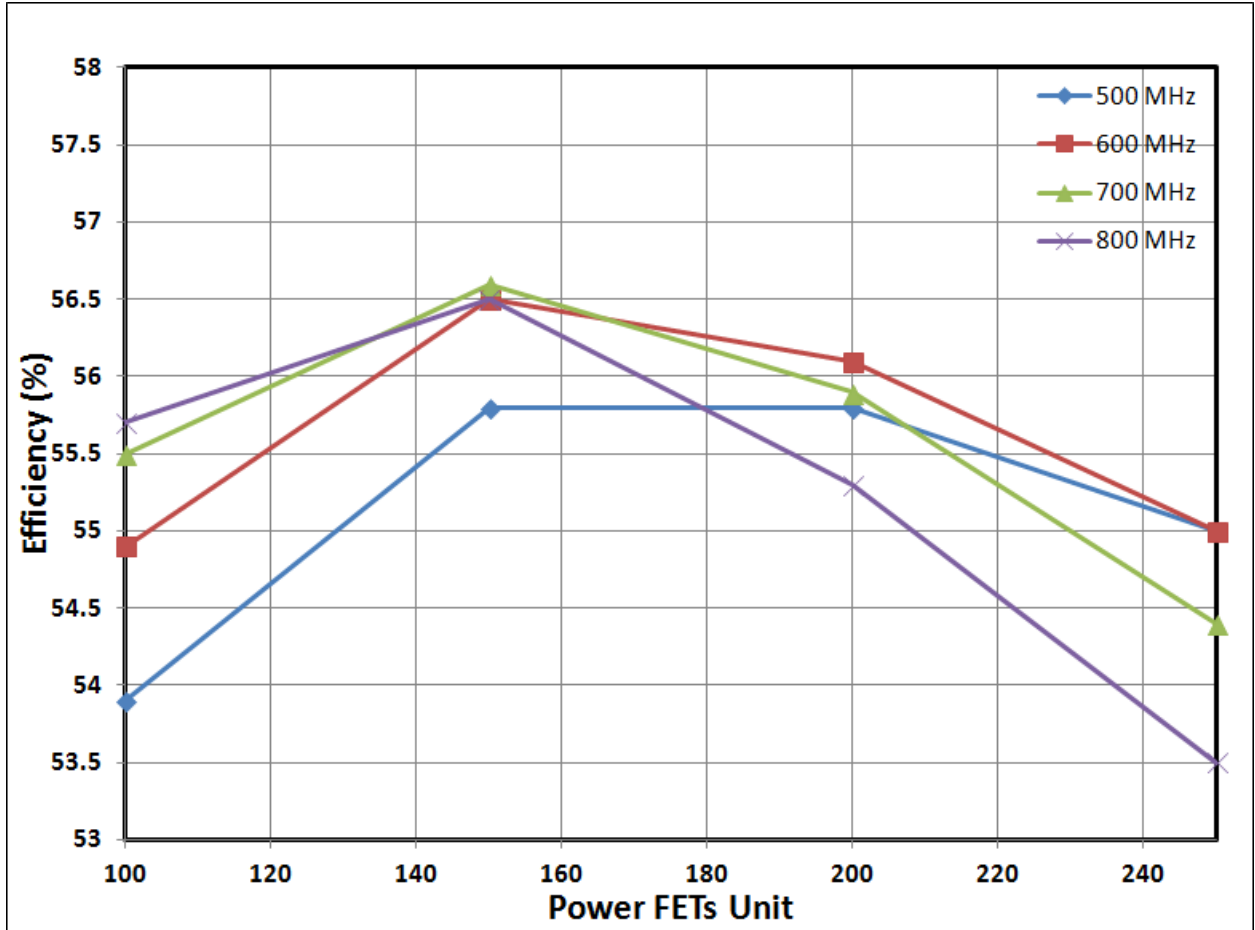


Figure 3.1. The calculated efficiency of the regulator with different power FETs size under different switching frequency

Based on the above plot, we can find out that under the optimized power FETs size, the calculated efficiency of the regulator increases when the switching frequency increases from 500MHz to 600MHz. However, after 600MHz, the calculated efficiency does not further increase. Considering the increased complicity with respect to the increased frequency, we choose 600MHz as the operating frequency of the proposed fully-integrated

buck regulator. Moreover, the capacitive coupling and magnetic coupling will both become worse for the inductor at higher switching frequency. For switching frequency equal or less than 500MHz, the silicon area overhead on the inductor by itself will be larger than 24nH, which makes the proposed solution less attractive.

3.2 Proposed Architecture

Fig. 3.2 shows a block diagram of the proposed fully-integrated buck regulator. The architecture employs a voltage mode Pulse Width Modulation (PWM) control scheme with 588MHz switching frequency. The choice of this frequency is based on analyzing the switching and conduction losses of the regulator, the minimum values of the inductor and capacitor that would be needed, and the complexity of designing the control loop at such high speed, which has been discussed in the previous section of the paper. At such frequency it can be shown using standard buck regulator design equations [8] that an inductor of 20nH will maintain Continuous Conduction Mode (CCM) of operation down to 20mA, and combined with a 300pF output capacitor will produce 60mV of output ripple voltage. With these values, the LC tank pole is located at around 65MHz. To achieve a high DC loop gain while ensuring the stability of the converter, type-I compensation is employed [9], where the error amplifier has 50dB of DC gain, and an output pole at about 10kHz. This ensures that the regulator's control loop is a first order loop with a DC gain of 65dB, a dominant pole at 10kHz, a unity gain frequency of about 10MHz, and a phase margin of almost 90 degrees. Compared to other types of compensation, type-I has the advantage of requiring minimal

passive components (a single 5pF capacitor), and thus is much more area efficient. Although type-I compensation reduces the bandwidth of the regulator's loop more than other types, the starting high switching frequency and wide bandwidth of the proposed regulator justifies using type-I compensation in order to reduce silicon area. Moreover, even with type-I compensation, the proposed buck regulator still achieves 20~50 times wider bandwidth than corresponding fully-integrated linear regulators [9], and therefore features significantly faster dynamic operation.

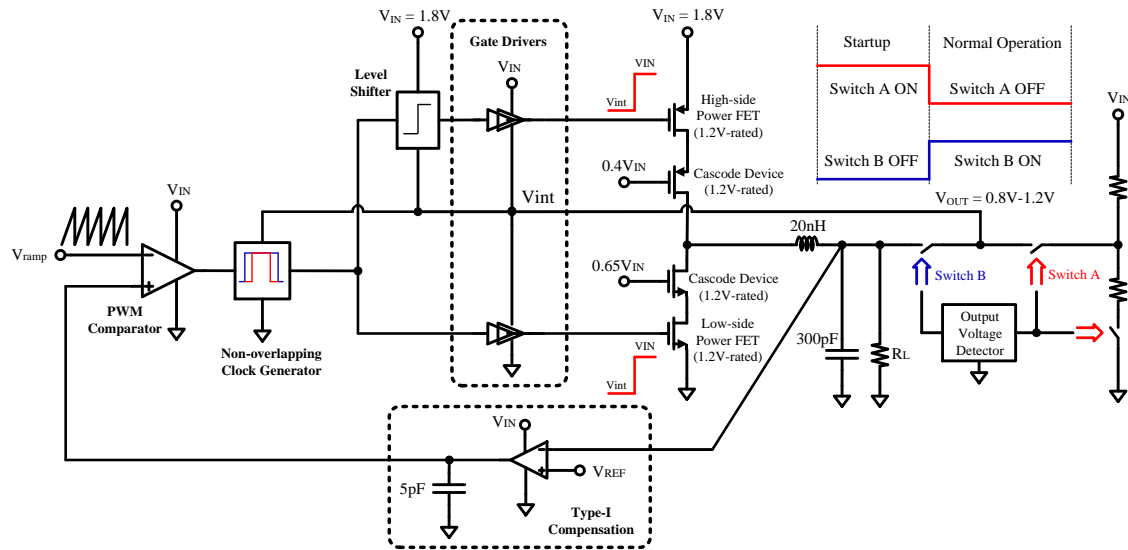


Figure 3.2. Top level block diagram for proposed buck regulator showing the self-regulation scheme, loop compensation, and the cascoded power switches.

3.3 Circuit Implementation

3.3.1 Power Train and Self-Regulation

Switching losses contribute significantly to the overall losses of the proposed regulator due to the high switching frequency. Therefore, the high-side and low-side power FETs are chosen to be 1.2V-rated transistors available in standard 65nm technology. These transistors have small gate capacitance, and thus employing them minimizes the switching losses. However, due to their low voltage rating, interfacing with 1.8V input becomes a challenge. To maintain the reliability of the gate-source junction of these transistors, the gate-drive signal is designed to switch between V_{int} and 1.8V for the high-side FET, and between 0V and V_{int} for the low-side FET, where V_{int} ranges from 0.8V to 1.2V. This ensures that the voltage across the gate-source junctions never exceeds the 1.2V rating of the transistors. To maintain the reliability of the gate-drain and drain-source junctions, two additional 1.2V-rated transistors are cascoded with the power FETs as shown in Fig. 3.2. The top cascode transistor has a gate bias of $(0.4 \times V_{\text{IN}})$, while the bottom cascode transistor has a gate bias of $(0.65 \times V_{\text{IN}})$. This guarantees that the gate-drain and drain-source voltages of the power FETs never exceed 1.2V under all switching conditions. The reliability of the cascode transistors themselves are maintained since the drain-bulk junction of the 1.2V-rated transistors can handle 1.8V.

The above scheme, however, requires an additional power supply V_{int} in order to operate the gate-drive circuits. This power supply is preferred to be efficient so as not to lose the benefit of reducing the switching losses, which results from limiting the swing of the gate control signals to $(V_{\text{IN}} - V_{\text{int}})$ and (V_{int}) for the high-side and low-side power FETs respectively. This limited swing reduces the switching losses by a factor of ~ 4 compared to

rail-to-rail switching from 1.8V input, and the benefit of that would be lost if V_{int} is implemented inefficiently (i.e. by using a linear regulator from the input). To preserve the efficiency benefit, and to also eliminate the area overhead of an extra power supply, the proposed regulator employs a self-regulation loop where its own efficient output serves as V_{int} . Nonetheless, this entails potential startup issues when the output of the regulator is not yet at the proper voltage level. To resolve this, a potential divider from the input is used to operate the gate-drive circuits during startup, and once the output of the regulator reaches its proper level, the regulator activates the self-regulation loop for normal operation as shown in Fig. 3.1. The output voltage detector is implemented using a comparator with a 200mV hysteretic band and a SR latch.

3.3.2 Compensator

Fig. 3.3 shows the simplified schematic of the proposed compensator. This compensator is essentially a current mirror based OTA with cascaded output. The input of the compensator is a differential pair (MN_1 and MN_2) while the output node will be connected to the input of the PWM comparator. The functionality of this block is to: a) provide enough gain to the system so that the DC error of the system is minimized (e.g. 60dB loop gain is equivalent to 1mV DC error); b) Create a dominant pole at the node V_{PWM} so as to stabilize the system. As it is discussed in the previous section, the pole location at node V_{PWM} is at 10kHz with 50dB DC gain. Since the compensator is operated under the supply voltage, all the transistors implemented are 1.8V rating devices so as to meet the reliability requirement.

3.3.3 PWM Comparator

Fig. 3.4 and 3.5 shows the schematic of the proposed PWM comparator and its buffer stages. This comparator is intended to generate the control pulse width by comparing the signal between the ramp generator and the output of the compensator, generating the pulse for the non-overlap generator. Thus, it requires relative fast speed of the comparator. In order to mitigate this issue, 1.2V-rated transistors are used for all the devices that are in the signal path to reduce the parasitic capacitance with the intermediate supply voltage as the supply. To ensure the headroom as well as the DC common mode of the operation, the supply of the input stage of the PWM comparator is 1.8V with input transistor bulk tied to source. The proposed PWM comparator is a fully-differential current mirror based comparator. This type of architecture has the nature of high bandwidth and great noise immunity, which is the best fit for the application as a PWM comparator. The buffer stage of the comparator is composed of a differential to single-ended converter and its corresponding buffers. This converter is implemented so as to provide high gain to generate the pulse for the non-overlap generator from the differential signal coming out of the PWM comparator.

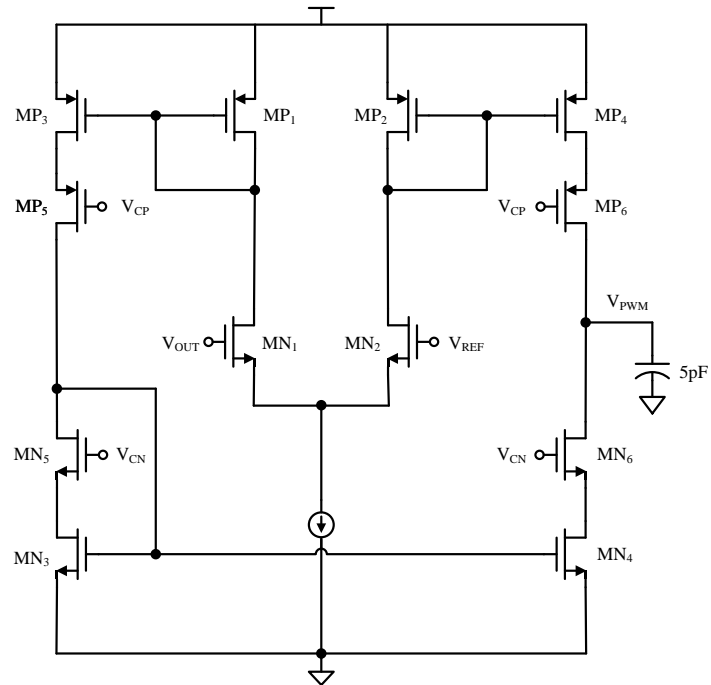


Figure 3.3. Schematic of the proposed compensator of the fully-integrated buck regulator

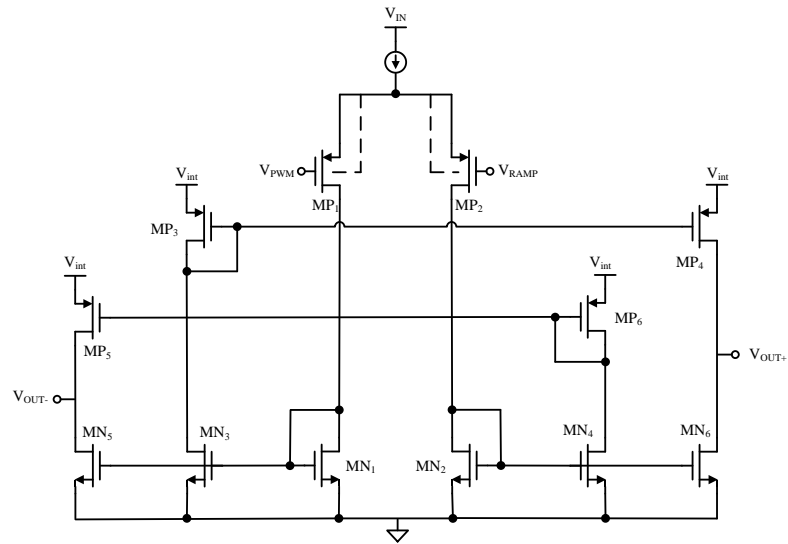


Figure 3.4. Schematic of the proposed PWM comparator of the fully-integrated buck

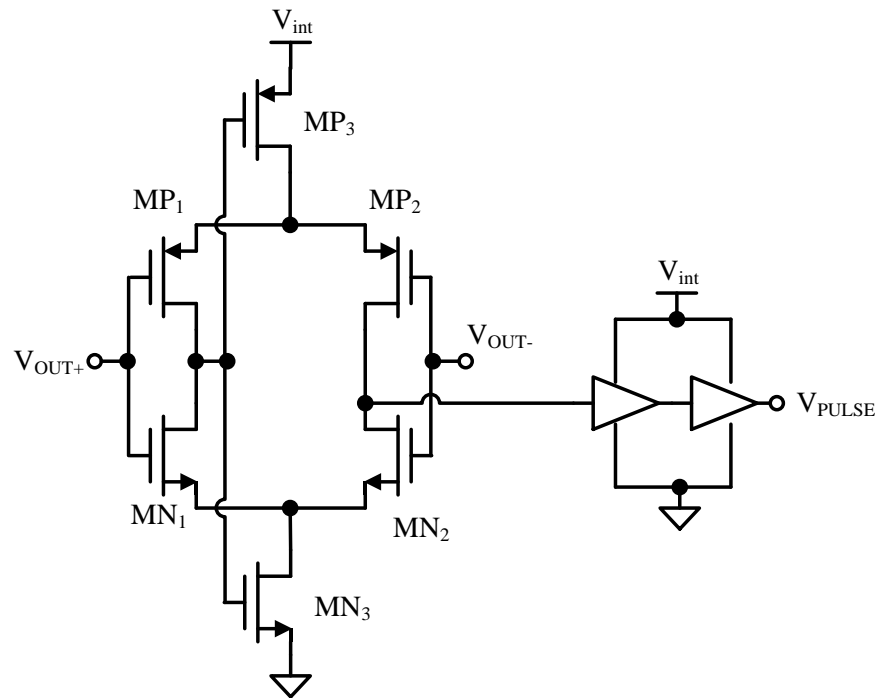


Figure 3.5. Schematic of the proposed buffer stage of the PWM comparator

3.3.4 Dynamic Level Shifter

Due to the proposed non-rail-to-rail control topology for the buck regulator. The driver signal of the high-side power FET has to be between V_{int} and V_{IN} while the output signal of the non-overlap generator is between 0 and V_{int} . Thus, there has to be a level shifter boosting up both the low-end and high-end levels of the signal. The schematic of the proposed dynamic level shifter is shown in Fig. 3.6. This level shifter is implemented so as to generate the gate control voltage of the high-side power FET. Comparing the traditional level shifter that is only capable of changing the voltage level to one of the rails[10], the proposed dynamic level shifter is able to boosting both rails by adding AC coupled capacitors at the input of the circuit.

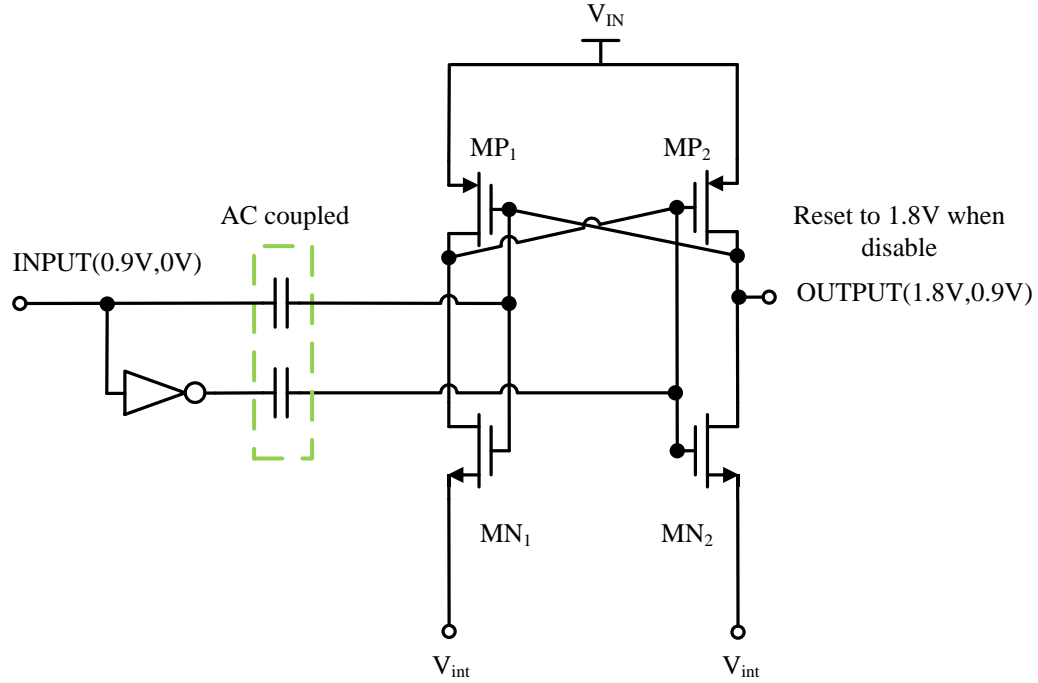


Figure 3.6. The schematic of the proposed dynamic level shifter

3.4 On-Chip Inductor Design and Modeling

The on-chip inductor employed by the proposed regulator is designed using the top copper metal layer (Metal-6) available in the process, which is thicker than all the lower metal layers and farthest from the substrate. This allows for lower parasitic resistance and capacitance, and thus better inductor quality factor (Q). The process parameters are used within an electromagnetic simulator, Agilent Advance Design System (ADS), to arrive at an inductor design that maximizes Q at the target switching frequency of 588MHz. The inductor

is designed with a square inner core of $116\mu\text{m}$ and outer core of $350\mu\text{m}$. It contains 8.5 turns, with the width of each winding at $12\mu\text{m}$ and the spacing between the windings at $2\mu\text{m}$. Instead of the classic 9-elements inductor model that is typically used for modeling small inductors in RF circuits [11], we propose using the 3-section lumped circuit model shown in Fig. 3.7 to model the behavior of the inductor. This enables more accurate modeling of the capacitive and resistive parasitics between the inductor and the substrate, particularly when the inductor is used for power circuits where it has larger value and longer winding length and width. With the aid of ADS, the model parameters for each section of the model can be computed and are listed in Table 3.2 while the ADS S-parameter simulation result is shown in Fig 3.8. As shown, the total series resistance of the inductor is 7.8Ω , which is large enough to dominate the losses in the proposed regulator. Note that this series resistance can be reduced by stacking other thick metal layers that may be available in some special flavors of 65nm technology. However, only one metal layer is used in this design to maintain the standard process flow. Since only the top metal layer is utilized for implementing the inductor, the proposed design leverages the area directly underneath the inductor to implement the rest of the regulator's circuitry. This significantly reduces the total area of the regulator and enables it to compete with linear regulators counterparts. Implementing capacitors underneath on-chip inductors was explored in Voltage Controlled Oscillators (VCO) [12]. Buck regulators share some features with VCOs, particularly that one side of the inductor is always connected directly to the output capacitor. Thus, the output capacitor can be stuffed underneath the on-chip inductor without much impact on efficiency due to magnetic coupling. Moreover, since the operating frequency of the proposed regulator is much lower than RF frequencies, the inductor generates much less magnetic flux. This can be

leveraged to stuff other active circuits such as the power FETs, input capacitor, and control circuits underneath the inductor as well. The full layout of the proposed regulator is shown in Fig. 3.9, where the input and output capacitors and all active circuits are stuffed underneath the windings of the inductor. The core area of the inductor is left empty to avoid excessive losses since the magnetic flux will be concentrated at the center of the core area. With this layout strategy, the area of the regulators is reduced by 50%. Note that the on-chip 270pF input capacitor is needed to mitigate the ringing that occurs at the regulator's input due to the interaction between the high switching frequency and the parasitic inductance associated with the input power pins.

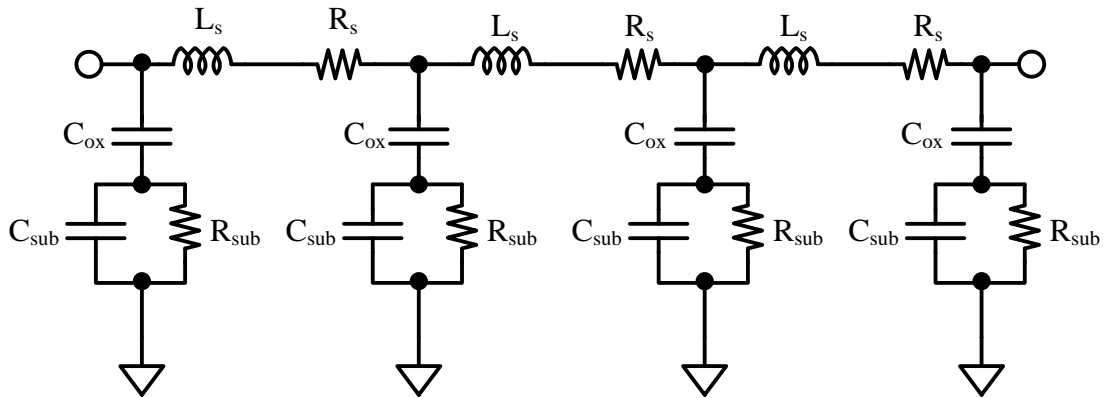


Figure 3.7. Three-segment lumped circuit model of the on-chip inductor.

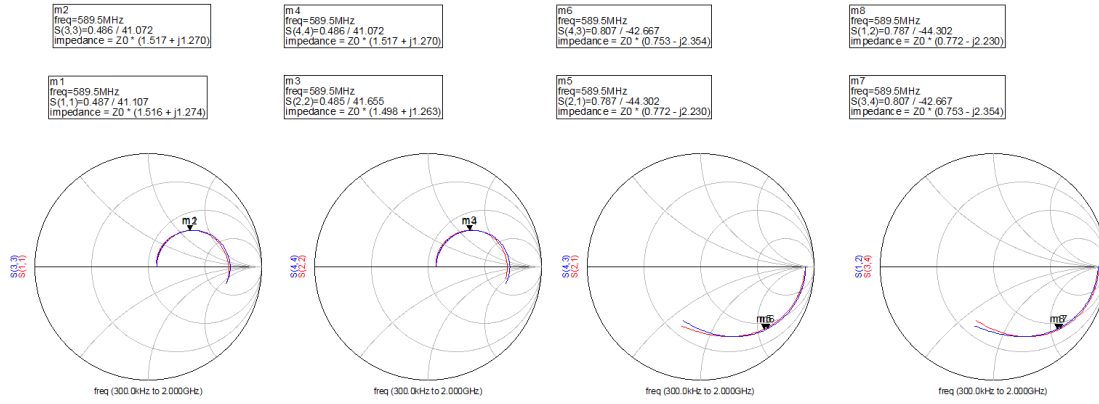


Figure 3.8. Proposed Inductor S-Parameter Simulation Results: Red Curve Inductor, Blue Curve ideal elements

Table 3.2. Design Parameter for On-Chip Inductor

Item	Value
L_s	6.6nH each, 19.8nH in total
R_s	2.6 Ω each, 7.8 Ω in total
C_{ox}	311fF
C_{sub}	11fF
R_{sub}	50 Ω
Q factor	8.4@588Mhz
Resonant Frequency	1.8Ghz
Area	0.12 mm ²

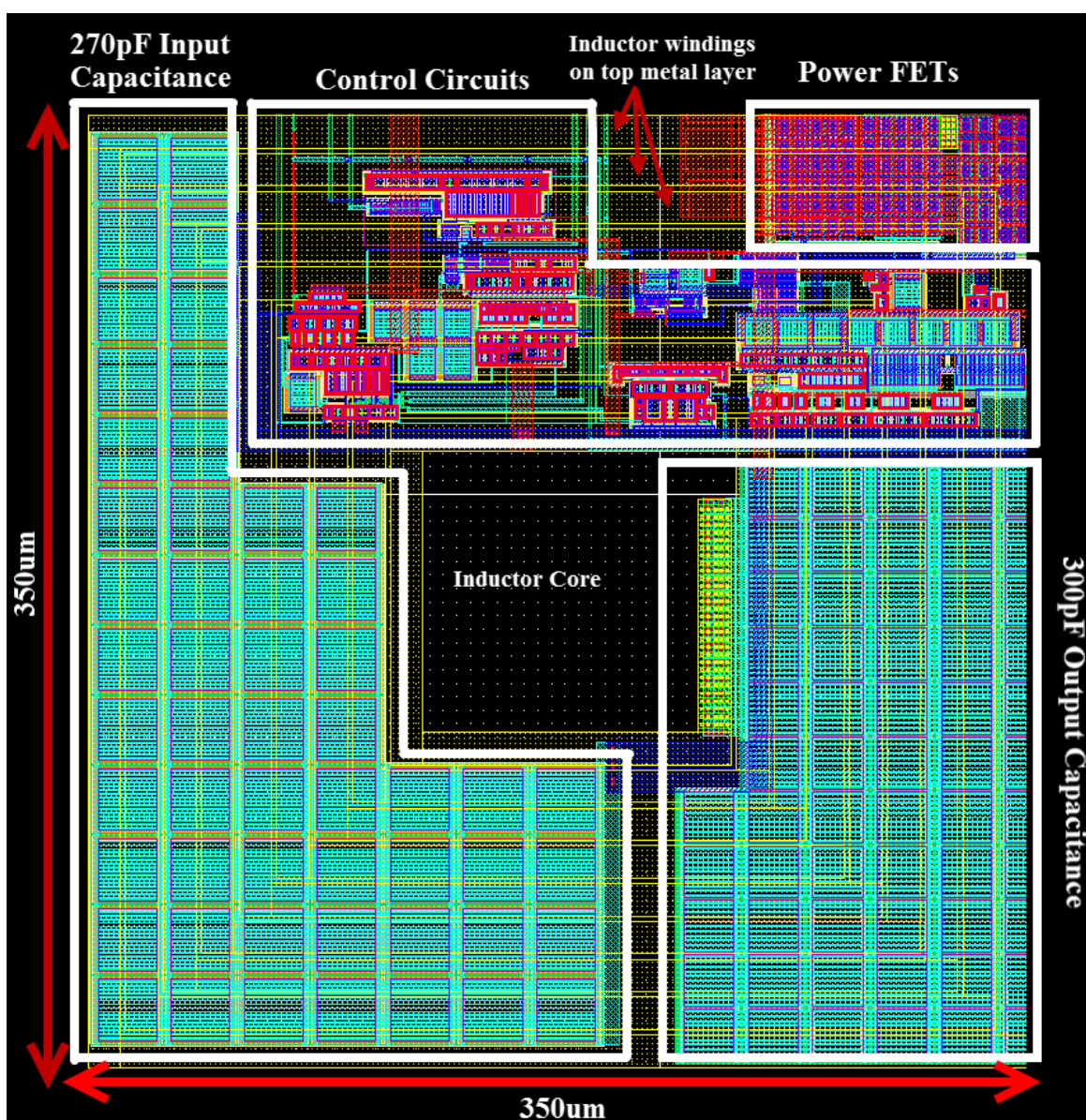


Figure 3.9. The layout of proposed buck regulator with circuit stuffing.

3.5 Experimental Results

The proposed regulator has been implemented in standard 65nm CMOS process and extracted layout simulations have been performed. This includes the extracted 3-section model of the inductor and all package parasitics. The simulated efficiency of the regulator versus load current and output voltage and how they compare to a linear regulator are shown in Fig. 3.10. At 1.8V input and 20mA load current, the regulator achieves 13.7% and 10% efficiency improvement over a linear regulator at 0.8V and 0.9V output voltage respectively. The dynamic performance of the regulator is shown in Fig. 3.11. The regulator starts up with the gate drive circuits operating from a potential divider from the input as shown in Fig. 3.2, and then switches to the self-regulation loop as described above. The regulator's response shows a settling time of less than 40ns for a positive 20mA load step and about 120ns for a negative 20mA load step, both with overshoot/undershoot of less than 150mV. The dynamic voltage scaling response of the regulator shows less than 240ns settling time for a 200mV output voltage step. This fast dynamic performance is attributed to the high switching frequency and bandwidth of the regulator. The peak-to-peak output voltage ripple of the regulator is shown to be about 60mV. This ripple voltage is well within $\pm 5\%$ of the output voltage, which is the typical requirement for digital loads that this regulator is targeting.

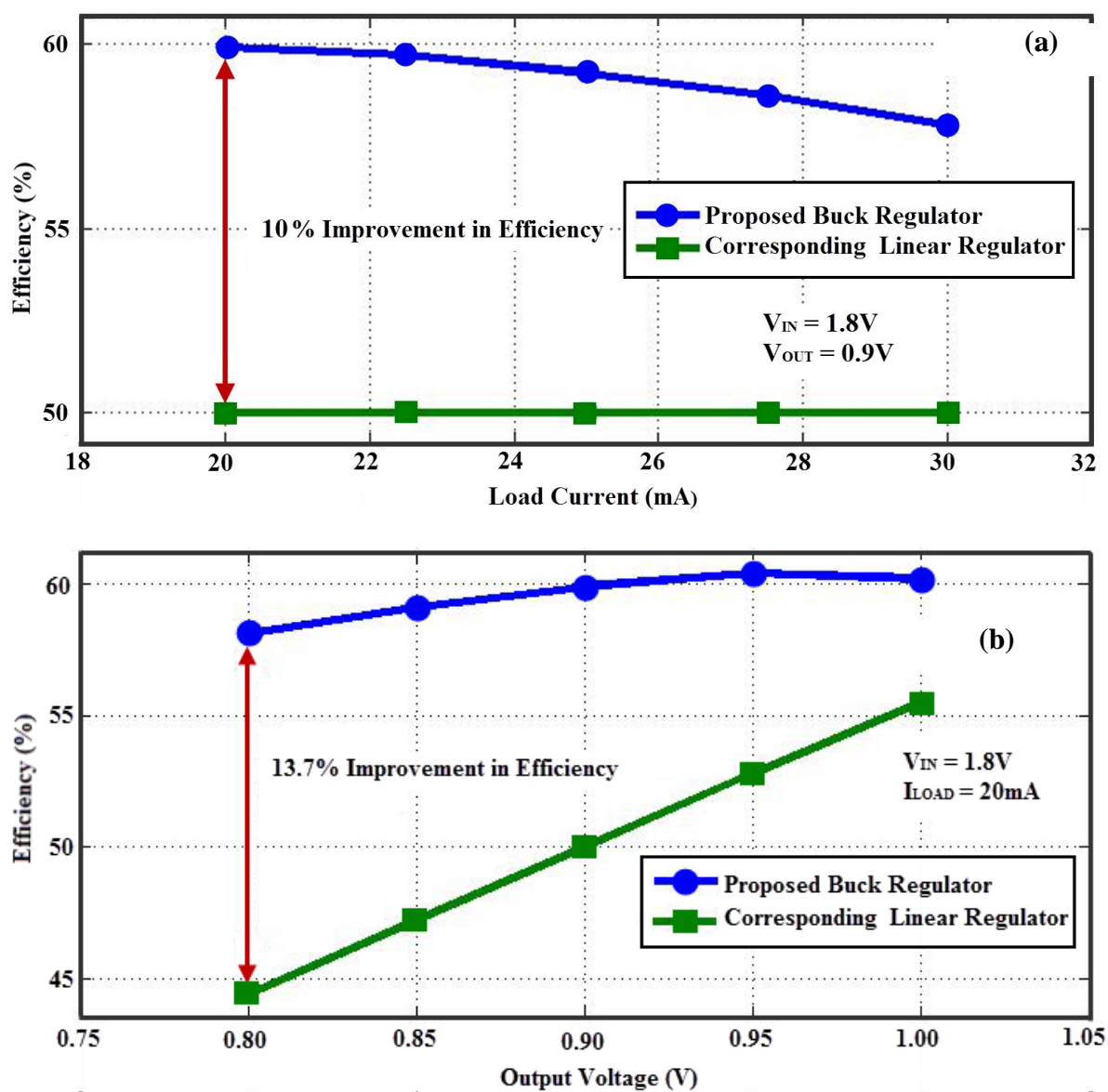


Figure 3.10. The simulated efficiency of the extracted layout of the proposed regulator: a) versus load current, and b) versus output voltage.

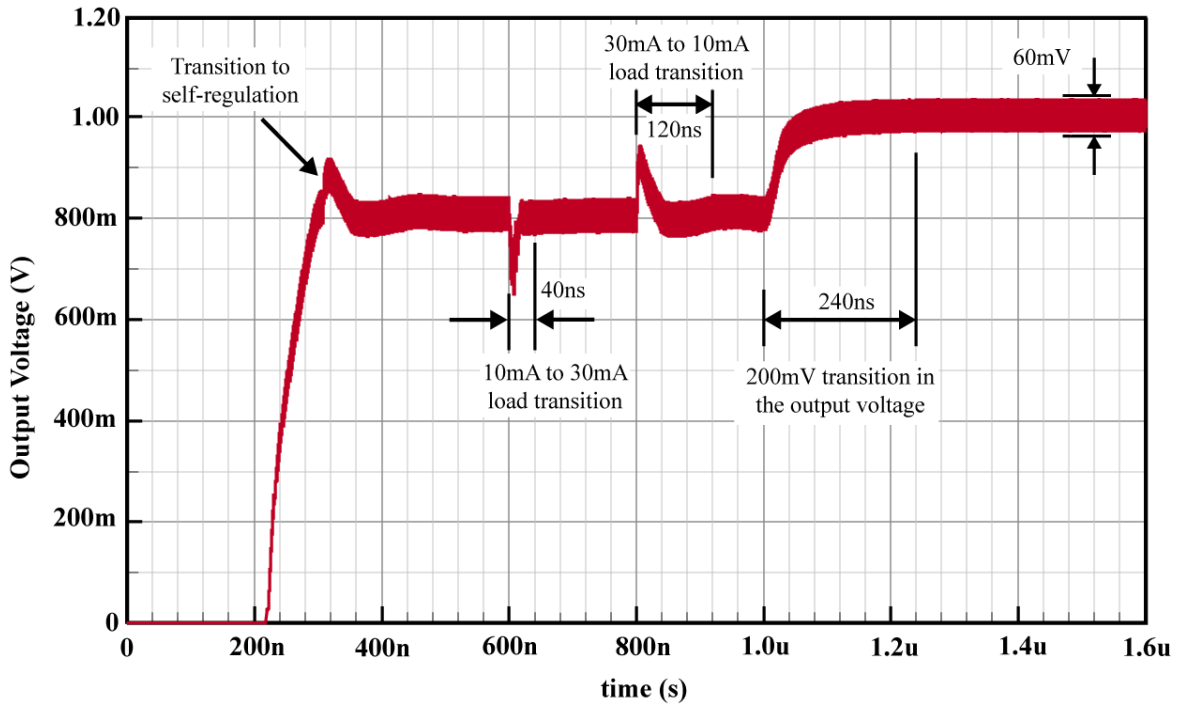


Figure 3.11. Transient response of the extracted layout of the proposed regulator showing response to load/output voltage steps and self-regulation transition.

3.6 Conclusion

In this chapter, we present a 588MHz switching regulator that employs only on-chip inductor and capacitors and is implemented in standard 65nm CMOS technology without any special process flow for on-chip passives. The presented regulator is designed to operate from a 1.8V input to generate an output that can be adapted between 0.8V to 1.2V and delivers a maximum of 30mA load current. To circumvent the large silicon area associated with the on-chip inductor, the presented regulator utilizes the full silicon area of the on-chip inductor by stuffing the rest of the regulator's circuitry directly underneath the inductor. This includes the power train, input and output decoupling capacitors, and the control circuits.

With this circuit stuffing strategy, the regulator's area is reduced to essentially the area of the on-chip inductor, which corresponds to cutting the total area of the regulator by 50%. To enable switching at 588MHz with low switching losses, low-voltage 1.2V core transistors are used as power switches. To ensure the reliability of these transistors with a 1.8V input, an intermediate 0.9V power supply is used to operate the gate drive circuits of the power switches. The proposed regulator employs a self-regulation scheme where its own efficient output is used to power the gate drive circuits, which eliminates the overhead of implementing an additional power supply and improves the overall power efficiency of the regulator. The proposed regulator delivers up to 13.7% better efficiency than a corresponding LDO and features fast dynamic response with settling time of 240ns for a 200mV output voltage step, and as short as 40ns for a 20mA load current step. It can be used in low-power micro-controllers to implement on-chip power supplies for digital loads with better efficiency than LDOs and reduced area compared to other switching regulators with on-chip passives.

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CHAPTER IV. A DCM-ONLY BUCK REGULATOR WITH HYSTERETIC-ASSISTED ADAPTIVE MINIMUM On-TIME CONTROL FOR LOW-POWER MICROCONTROLLERS

Microcontrollers are central to many power-sensitive industrial and consumer applications, each of which has different requirements in terms of powering options and the passive components they can accommodate. Thus, power-efficient microcontrollers that can support a wide range of potential operating scenarios with minimal customization overhead are in an ever increasing demand. Since the internal power regulators within a microcontroller typically determine how the microcontroller may be powered and most of the passive components needed, they represent a critical component of microcontroller design. To reduce power consumption, the latest trend in microcontrollers is to integrate a buck regulator to efficiently deliver power to the digital core. Such regulator is typically required to support up to a 40mA load, and provide an output between 0.9V and 1.4V that can be adapted based on the desired performance and power consumption of the digital core [1-3]. Moreover, since microcontrollers spend over 50% of their operation time in idle and low-power modes, the regulator must maintain high power conversion efficiency even at loads as low as 200 μ A. Furthermore, to support multiple powering options for the microcontroller, such as an external on-board regulator, a single Li-Ion battery, or up to two button-cell batteries, the regulator must be able to handle inputs between 1.8V and 4.2V. Additionally, to accommodate varying size and cost limitations in different applications, the regulator must be able to support a wide selection of off-chip passives in terms of value, tolerance, and footprint without calibration, or re-optimization in order to minimize system integration cost. Finally, it

should constitute a small overhead in terms of the microcontroller's silicon area and implementation cost.

To meet the above requirements, this paper presents a 40mA, buck regulator with voltage-mode Hysteretic-Assisted Adaptive Minimum Constant On-Time (HA-AMOT) control [4] that results in robust performance across a wide range of input, output, and passive components values without calibration or trimming. The proposed regulator operates in AMOT mode with minimized inductor peak current towards the lower end of the load range and automatically transitions to hysteretic mode towards the higher end of the range when the inductor peak current is insufficient to sustain the load in DCM. When in hysteretic mode, it always operates right at the border of DCM, and thus continues to minimize the inductor peak current and enables optimized efficiency with the smallest possible power switch. As a result, DCM operation (i.e. no loop compensation) with minimized inductor peak current (i.e. low losses) is ensured across the entire load range. The AMOT and hysteretic modes utilize the same circuits interchangeably, so effectively only a single controller is implemented, resulting in compact silicon area and low quiescent current. Moreover, power-gating is employed to further reduce quiescent current to enhance efficiency at sub-1mA loads. The thesis is organized as follows: section 4.1 discusses the limitations of existing schemes in handling a wide range of operating scenarios in DCM; section 4.2 and 4.3 present the proposed scheme and its circuit implementation; section 4.4 presents the experimental results.

4.1 Limitations of Existing Control Schemes in Handling a Wide Range of Operating Scenarios in DCM

With a maximum load of only 40mA, forcing the regulator to operate in the inherently stable DCM [5] for the entire load range is logical as it eliminates the need for loop compensation, and thus reduces silicon area and quiescent current. Combining that with PFM control [6-9], or PWM with segmented power switches [10] helps in preserving high light-load efficiency by scaling the switching losses with the load. Power and clock-gating may also be used to further reduce quiescent and enhance light-load efficiency [6-7, 11-12]. A popular PFM scheme is the Constant On-Time (COT) controller [6-9], which turns on the regulator's high-side power switch for a constant on-time (T_{on}) once the output voltage drops below a reference level. However, handling a wide range of input, output, and inductor values is quite difficult with such scheme due to the strong dependency of the inductor peak current on these parameters. Thus, ensuring DCM (i.e. inductor peak current is at least double the load current [5]) under all possible operating scenarios inevitably results in excessive inductor peak current in some scenarios, leading to degraded efficiency unless the controller is recalibrated based on the scenario. Conventional Adaptive COT (ACOT) control can partially solve this problem by making the on-time inversely proportional to the difference between the input and output voltages [13]. This produces a constant inductor peak current regardless of input and output voltages, and thus automatically eliminates excessive inductor peak current due to that. However, it fails to automatically adapt to a wide range of inductor values, and thus excessive inductor peak current continues to be a challenge. Current-mode control similar to [10, 14] may seem to offer a solution to this problem as they directly control the inductor peak current regardless of the operating scenario. However, in addition to the

complexity, area and power overhead of inductor current sensing, the inductor peak current will typically exhibit large errors due to random mismatches, inaccurate on-chip elements, and variability in the control loop's delay. Accounting for these errors while ensuring DCM in all scenarios still leads to excessive inductor peak current, especially in scenarios with maximum input, minimum output, and minimum inductor. Voltage-mode hysteretic controllers in DCM can maintain a minimized inductor peak current for any load regardless of the input, output, and inductor values as they always operate at the border of DCM. However, as will be detailed in section 4.2, they result in much degraded efficiency towards the lower end of the load range due to excessively high switching frequency.

4.2 Proposed Control Scheme

In a conventional ACOT controller, shown in Fig. 4.1a, the constant on-time T_{on} is inversely proportional to the difference between the input V_{in} and the output V_o [13]. Thus, for a given inductor L , setting T_{on} such that the inductor peak current I_p is exactly twice the maximum load current I_{Lmax} ensures DCM operation for the entire load range with the minimum possible I_p regardless of V_{in} and V_o . However, if a wide range of inductor values must be supported, ensuring DCM requires setting T_{on} long enough such that $I_p = 2I_{Lmax}(L_{max}/L)$, where L_{max} is the maximum possible inductor, and L is the actual inductor being used. Thus, when the minimum possible inductor L_{min} is used, I_p becomes $2I_{Lmax}(L_{max}/L_{min})$, which is excessive if the inductor range to be supported is wide, leading to degraded efficiency. To avoid that, we propose minimizing T_{on} such that $I_p = 2I_{Lmax}$

when the minimum possible inductor is used [4]. In this case, the controller is termed Adaptive Minimum Constant On-Time (AMOT) [4]. Such controller produces the minimum possible constant I_p to maintain DCM for the entire load range when $L = L_{\min}$, but for $L > L_{\min}$, it fails to maintain DCM towards the higher end of the load range due to insufficient I_p , which forces the inductor into Continuous Conduction Mode (CCM). For the AMOT controller alone, I_p and the switching frequency f_s of the regulator for a given inductor $L > L_{\min}$ and load current I_L can be represented by:

$$I_p = \left(\frac{V_{in} - V_o}{L} \right) T_{on} = \frac{2 I_{Lmax} L_{\min}}{L} \quad (4.1)$$

$$f_s = \frac{(V_{in} - V_o) V_o L}{2 V_{in} L_{\min}^2 I_{Lmax}^2} I_L \quad (4.2)$$

Eqs. (4.1) and (4.2) are plotted in Fig. 1c versus load current up to 40mA, and with 4.7 μ H and 10 μ H inductors, which are the desired minimum and maximum inductors respectively. The equations are valid only for loads below $(L_{\min}/L)I_{Lmax}$ (DCM operation), and show that I_p is constant, while f_s scales linearly with load as desired for reducing switching losses at light loads. For loads over $(L_{\min}/L)I_{Lmax}$, the inductor moves into CCM, and for output capacitors with small estimated series resistance R_{esr} (ceramic capacitors),

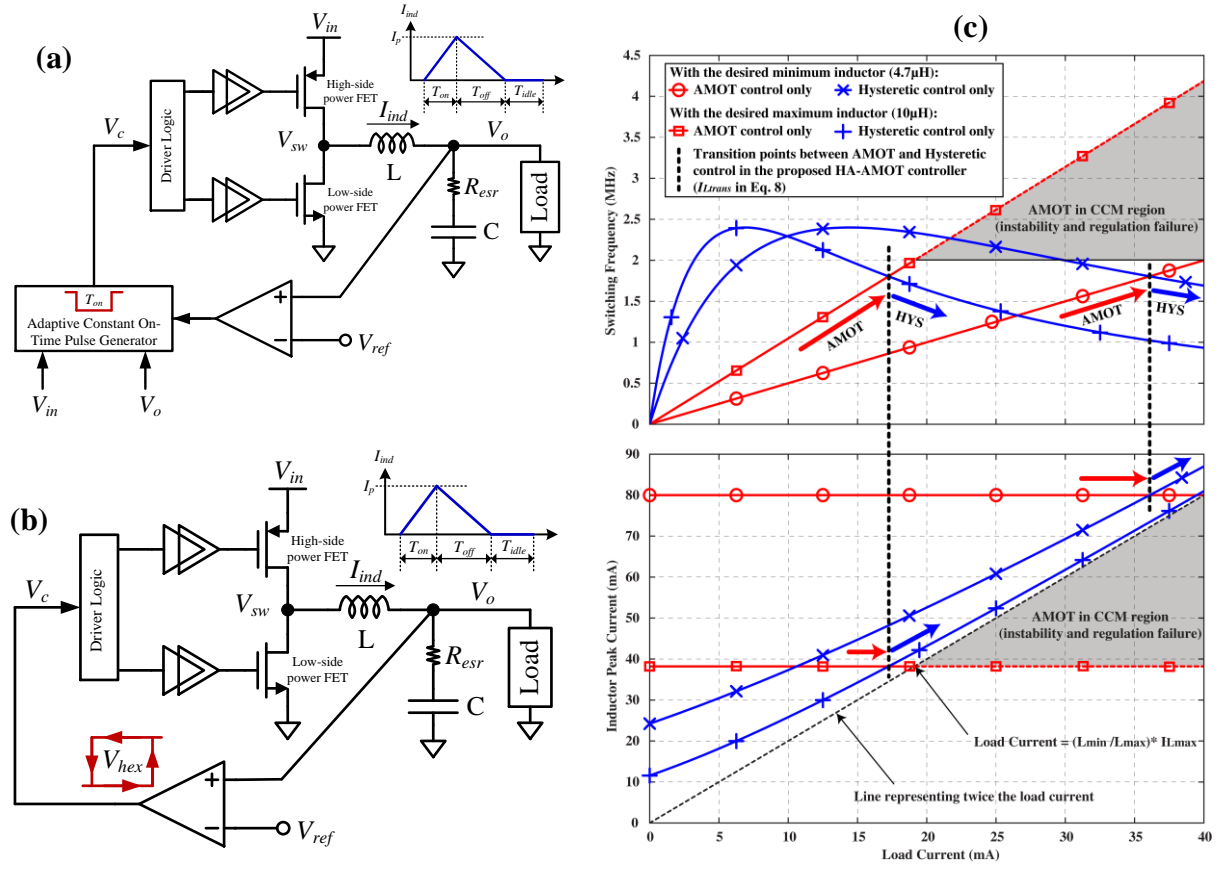


Figure 4.1. Conventional controllers operating in DCM: (a) ACOT, and (b) Voltage-mode hysteretic. (c) Simulated inductor peak current and switching frequency versus load for the AMOT controller alone, hysteretic controller alone, and the transition between them in the proposed Hysteretic-Assisted AMOT controller.

instability and regulation failure occur due to the phase shift between the output voltage and the inductor current [15], and loop compensation with additional passives must be used to ensure proper functionality in CCM.

To address the above limitation, we propose assisting the AMOT controller with a hysteretic controller towards the higher end of the load range to prevent the inductor from moving into CCM, which requires a close study of hysteretic operation in DCM. A conventional voltage-mode hysteretic controller, shown in Fig. 4.1b, relies on a hysteretic comparator to turn on the high-side power FET once the output voltage drops below the

lower bound of the hysteretic band, and turns it off once the output voltage increases above the higher bound of the hysteretic band. Assuming DCM operation, the inductor peak current is determined by solving the quadratic equation:

$$\left(\frac{1}{2 \alpha_1 C}\right) I_p^2 - \left(\frac{I_L}{\alpha_1 C} - R_{\text{esr}}\right) I_p - V_{\text{He}} = 0 \quad (4.3)$$

where V_{He} is the effective hysteretic band of the comparator, $\alpha_1 = (V_{\text{in}} - V_o)/L$ is the charging rate of the inductor, and C is the output capacitor. V_{He} can be further represented as:

$$V_{\text{He}} = V_{\text{Hex}} + \left(\frac{\alpha_1}{2C}\right) t_d^2 + \left(\frac{I_L}{2C}\right) t_d \quad (4.4)$$

where V_{Hex} is the explicit portion of the hysteretic band, while the rest is the implicit portion due to the comparator's delay t_d . Solving Eq. (4.3), I_p can be represented as:

$$I_p = (I_L - \alpha_1 R_{\text{esr}} C) \left[1 - \sqrt{1 + \frac{2 \alpha_1 C V_{\text{He}}}{(I_L - \alpha_1 R_{\text{esr}} C)^2}} \right] \quad \text{for } I_L \leq \alpha_1 R_{\text{esr}} C$$

$$I_p = (I_L - \alpha_1 R_{\text{esr}} C) \left[1 + \sqrt{1 + \frac{2 \alpha_1 C V_{\text{He}}}{(I_L - \alpha_1 R_{\text{esr}} C)^2}} \right] \quad \text{for } I_L > \alpha_1 R_{\text{esr}} C \quad (4.5)$$

while the switching frequency can be represented by:

$$f_s = \frac{2 \alpha_1}{\left(1 + \frac{\alpha_1}{\alpha_2}\right) I_p^2} I_L \quad (4.6)$$

where $\alpha_2 = V_o/L$ is the discharging rate of the inductor. To guarantee DCM operation, the inductor peak current must be at least twice the maximum load current under all conditions. By making $I_p = 2I_{L\text{max}}$ and $I_L = I_{L\text{max}}$ in Eq. (4.3), the effective hysteretic band of the comparator must meet the following condition in order to maintain DCM operation:

$$V_{\text{He}} \geq 2 I_{L\text{max}} R_{\text{esr}} \quad (4.7)$$

If V_{He} is less than the limit in Eq. (4.7), the inductor moves into CCM for loads above $V_{He}/2R_{esr}$, and instability and regulation failure occur for small values of R_{esr} . Similar to the AMOT case, the inductor peak current and the switching frequency with the hysteretic controller alone are plotted versus load in Fig. 4.1c with the same inductor values as the AMOT case.

By inspecting the plot and Eq. (4.5), it can be seen that the inductor peak current has a quasi-linear relationship with the load, where the inductor peak current is always very close to twice the load current, i.e. border of DCM and CCM. In fact, this relation becomes exact in the ideal case with $R_{esr} = 0$ and $V_{He} = 0$. This allows the controller to ensure DCM operation for any load with minimal excessive inductor peak current irrespective of the wide range of input, output, and inductor values. However, according to Eq. (4.6), this quasi-linear relation between the inductor peak current and the load yields a switching frequency that increases as the load drops, before it starts to decrease again towards the very low end of the load range when the term $\left(\frac{2\alpha_1 C V_H}{(I_L - \alpha_1 R_{esr} C)^2}\right)$ in Eq. (4.5) becomes larger than unity and the relation between the inductor peak current and the load slightly deviates from its linear form. This behavior results in excessively high switching frequencies in the lower end of the load range as shown in Fig. 4.1c, leading to much degraded efficiency. Moreover, at the lower end of the load range, the inductor peak current becomes more sensitive to the input, output, and inductor values, which is highly undesirable if the a wide range of these parameters must be supported.

Comparing the behavior of the AMOT and voltage-mode hysteretic controllers, it can be seen that the hysteretic controller is superior to AMOT towards the high end of the load

range as it maintains DCM operation with no loop compensation while producing minimal excessive inductor peak current. On the other hand, the AMOT controller is superior towards the lower end of the load range as it results in much lower switching frequencies, and thus lower switching losses, which dominate at light loads. In order to leverage the best of both controllers, we propose implementing a scheme that transitions automatically between the two control modes at the load point at which the switching frequency produced by both modes is identical as shown by the arrows in Fig. 4.1c. This point serves as an ideal transition point since below it, the hysteretic controller results in higher switching frequency than AMOT, while slightly above it, the AMOT controller moves into CCM when an inductor close the maximum is used.

To realize the proposed scheme with automatic transition and without the overhead of building two separate controllers, the Hysteretic-Assisted AMOT (HA-AMOT) controller in Fig. 4.2a is proposed. In this implementation, a single-threshold control comparator (explicit hysteresis $V_{Hex} = 0$) is used along with an adaptive AMOT pulse generator with a pulse width adapted to the input and output voltages to produce the constant inductor peak current I_p in Eq. (4.1). To understand the operation of the controller, we will initially assume zero R_{esr} and comparator delay t_d for simplicity, and start at loads less than $(I_p/2)$. In this case, as shown in Fig. 4.2b, once the output voltage drops below V_{ref} , the control comparator toggles its state and activates the pulse generator. Since the inductor current starts from zero (DCM), the output voltage drops further before it starts to recover, and due to charge conservation, it recovers back to V_{ref} when the inductor current reaches exactly twice the load current. At this point, the control comparator toggles its state one more time before the

inductor current reaches I_p , and the observation logic concludes that the inductor has enough current to sustain the load in DCM, and allows the on-time pulse unaltered. Thus, the operation of the controller is essentially identical to the AMOT controller described by Eq. (4.1) and (4.2). As the load current increases, the operation remains the same until the load exceeds $(I_p/2)$. In this case, as shown in Fig. 4.2b, the comparator doesn't toggle its state by the end of the on-time pulse, implying that I_p is insufficient to sustain the load in DCM, and the inductor will have to move into CCM. To prevent this scenario, the observation logic intervenes and extends the on-time pulse (by simply ignoring it) until the comparator toggles its state, then immediately terminates the pulse. Thus, for loads above $(I_p/2)$, the observation logic's action effectively transforms the AMOT control to hysteretic since it ensures that the on-time pulse width is extended such that the inductor peak current is always equal to twice the load current (border of DCM and CCM). For non-zero R_{esr} and t_d , the operation is the same, except that the actual load point I_{Ltrans} at which transition from the AMOT mode to the hysteretic mode happens drops below $(I_p/2)$ and becomes:

$$I_{Ltrans} = \frac{I_p}{2} \left[\frac{1 + \left(\frac{V_{in} - V_o}{I_{Lmax} L_{min}} \right) R_{esr} C}{1 + \left(\frac{V_{in} - V_o}{2 I_{Lmax} L_{min}} \right) t_d} \right] \quad (4.8)$$

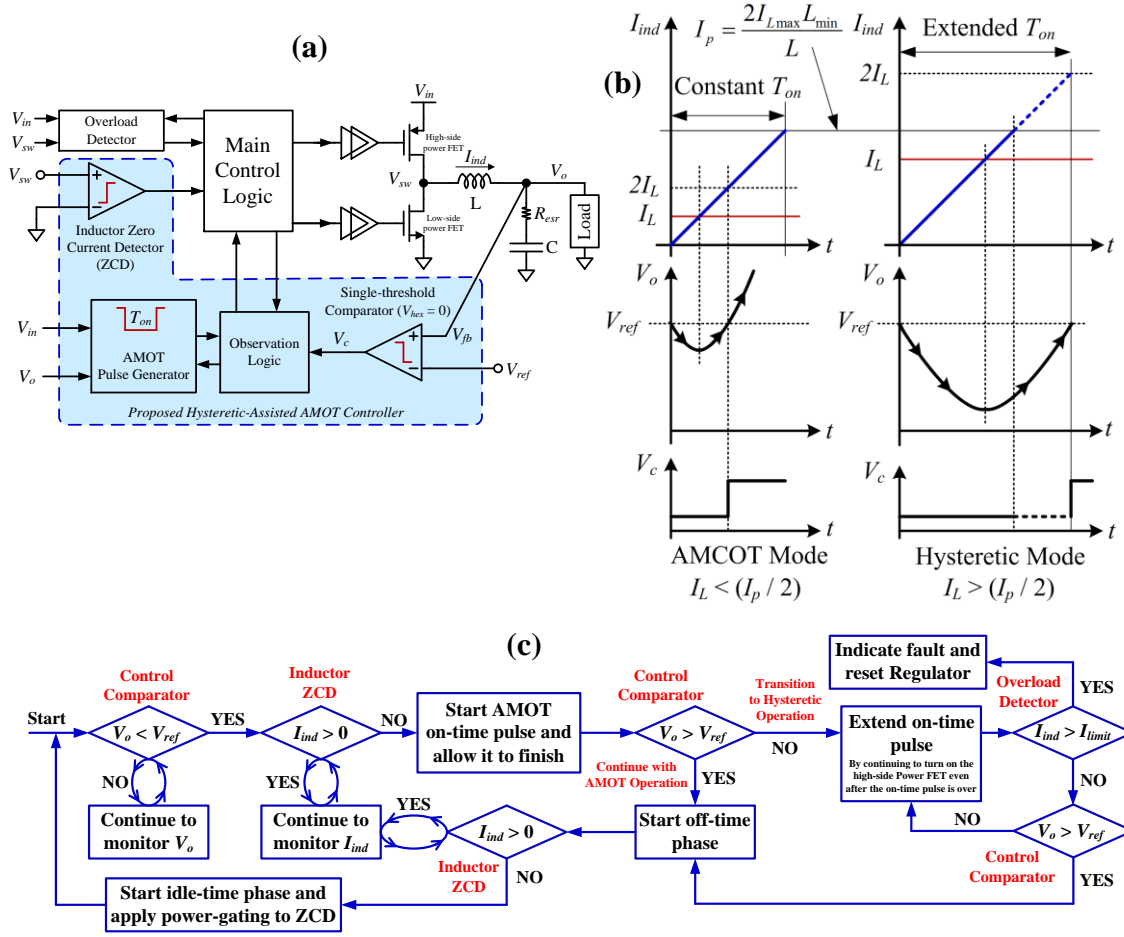


Figure 4.2. (a) Block diagram of the proposed HA-AMCOT controller, (b) Important signals showing the operation of the controller when the load current is less than, or higher than half the constant inductor peak current, and (c) A complete flow chart describing the operation.

For loads above this point, the controller operates in hysteretic mode following Eqs. (4.4)-(4.6), except that $V_{Hex} = 0$. Thus, the effective hysteretic band V_{He} becomes only a function of t_d , which must be designed to ensure that V_{He} satisfies Eq. (4.7).

The above description of the operation of the proposed controller suggests that DCM operation is always guaranteed in steady-state. However, if the load changes during the off-time from a value less than I_{Ltrans} to a value higher than I_{Ltrans} , the inductor may move into CCM for at least one switching cycle, which can lead to instability. To prevent this scenario, the inductor Zero-Current-Detector (ZCD), which is required anyway in DCM for turning off the low-side switch during idle-time, is used by the main control logic to disallow the observation logic from ever triggering a new on-time pulse unless the inductor current is zero. The detector is implemented using a comparator that continuously observes the switching node voltage during the off time. Moreover, in short-circuit or overload conditions, the on-time pulse must be prevented from being extended to where the inductor current reaches damaging levels. Thus, an overload detector is implemented by sensing the high-side FET current as the on-time being extended, and if the inductor current reaches I_{limit} , the regulator is reset and a fault condition is indicated. A complete flow chart describing the operation of the proposed controller is shown in Fig. 4.2c.

In addition to the advantages described earlier of transitioning between AMOT and hysteretic modes as a function of load, the specific implementation in Fig. 4.2 offers additional notable advantages. First, it eliminates the need for two separate controllers since the same circuits are used interchangeably in the AMOT and hysteretic modes. Second, all the circuit blocks in Fig. 4.2a are anyway necessary blocks in conventional ACOT controllers operating in DCM. Minimizing the on-time in order to implement the AMOT mode, and the observation logic that transforms it to a hysteretic mode for loads above I_{Ltrans} constitute insignificant overhead in terms of silicon area or quiescent current beyond a standard ACOT controller. Third, despite the fact that the transition between the two control modes is a

unnecessary circuits during that phase. This includes the ZCD comparator, where its bias current is turned off during the idle-time phase as it is not needed except during the off-time phase. However, to ensure it is ready by the start of the off-time phase, its bias current is turned back on earlier at the start of the on-time phase, and a 20ns blanking time at the start of the off-time phase is applied to prevent any false triggering of the controller as the comparator wakes up. Power-gating is also applied to the AMOT pulse generator and the control comparator, where their bias current is reduced during the off-time and idle-time phases since high performance is not required from these circuits during these phases.

In terms of circuit implementation, the most critical circuit blocks in the proposed controller are the adaptive AMOT pulse generator and the control comparator, which are discussed in details in the following two sub-sections.

4.3.1 Adaptive Minimum Constant On-time Pulse Generator

The AMOT pulse generator is shown in Fig. 4.3a, where a two-stage amplifier composed of a current-mirror OTA and a source-follower, is powered from the input of the regulator V_{in} , and is connected in a unity feedback configuration to reproduce the regulator's output voltage V_o at node "X". As a result, the current flowing in the resistance R_{amcot} becomes proportional to the difference between the input and output voltages. This current is mirrored to charge a capacitor C_{amcot} through the switch S_{21} once the pulse generator is triggered by the regulator's control comparator to start the on-time phase. Once V_{amcot} crosses the reference $V_{refamcot}$, the AMOT comparator is triggered, and C_{amcot} is discharged through deactivating the switch S_{21} and activating the switch S_{22} . Moreover, the AMOT

comparator is power-gated through the switch S_{pg} in order to reduce the quiescent current. It is worth noting that the transistor M_{sf} is implemented using a low-voltage, low-threshold PMOS device with its bulk connected to the source to ensure that node “X” tracks the regulator’s output down to 0.9V with no headroom issues. With this implementation, the on-time T_{on} can be rewritten as:

$$T_{on} = \frac{V_{refamot} R_{amot} C_{amot}}{V_{in} - V_o} \quad (4.9)$$

Therefore, meeting the inductor peak current value set by Eq. (4.1) can be ensured through the following equation, which must be met under all process and temperature corners:

$$V_{refamot} R_{amot} C_{amot} \geq 2 I_{Lmax} L_{min} \quad (4.10)$$

Compared to other ACOT pulse generator implementations, such as in [13], this circuit offers two important advantages. First, it generates a pulse that is inversely proportional to the difference between the input and output voltages down to very low output voltage levels. Second, the accuracy of the pulse width can be greatly improved by using a high-speed AMOT comparator, but without significant average quiescent current overhead due to the employed power-gating. A shortcoming that is worth noting, however, is that due to process and temperature variations in R_{amcot} , the inductor peak current may exceed its desired value in Eq. (4.1). Nonetheless, since the microcontroller has a readily available

trimmed bandgap, the same trimming code is used to minimize the variations in R_{amcot} in order to circumvent this shortcoming.

4.3.2 Control Comparator

The proposed control comparator is shown in Fig. 4.3b [16], where it has a resistor-loaded, low-gain pre-amplifier stage (to maximize speed), followed by a conventional differential to single-ended stage (to provide high gain). The pre-amplifier is composed of a static GM stage (i.e. always enabled) and a power-gated GM stage that is enabled during the on-time phase to maximize speed, and disabled during the off-time and idle-time phases to reduce the average quiescent current. This dynamic power-gating causes significant charge injection at the gates of the input differential pair, which produces glitches on the reference voltage V_{ref} . This is problematic since the reference voltage is shared by many other circuits in the microcontroller [17]. To mitigate this issue, a minimum size isolation switch S_{is} and a holding capacitor C_h are introduced. At the end of the on-time phase, S_{is} is immediately turned off, while power-gating is enabled by turning off the switches $S_{11} - S_{13}$ after a slight delay T_{nvl} (2~5ns). Thus, the reference voltage is isolated from the input differential pair when power-gating is enabled, and any charge injection is stored on C_h . At the start of the on-time phase, power-gating is immediately disabled by turning on the switches $S_{11} - S_{13}$, while S_{is} is turned back on after a delay of T_{nvl} . Thus, any previously-held charge on C_h is discharged by the opposite charge injection action, leading to minimal disturbance to the reference voltage. The delay time t_d of the comparator is designed so that V_{He} satisfies Eq. (4.7) to ensure DCM operation. To avoid false triggering due to noise and lack of explicit hysteresis, a blanking time is enforced by the Observation Logic to latch the comparator's output for ~50ns after each triggering event.

4.4 Measurement Results

The proposed HA-AMOT buck regulator is implemented in a 90nm standard CMOS process as part of a low-power low-cost microcontroller system. Fig. 4.4 shows the die photo of the part that contains the converter, where double bonding is utilized to minimize the resistive wire-bonding parasitics at the input, ground, and switching nodes of the converter. The total area of the converter is 0.1mm^2 , out of which 0.04 mm^2 is occupied by the power switches and their drivers. Due to layout restrictions imposed by other circuits in the microcontroller, the converter had to be placed $100\mu\text{m}$ away from the I/O ring, which slightly degrades efficiency due to metal routing. The key performance metrics of the regulator and the range of input, output, and passive components it is characterized with are summarized in Table 4.1. To verify its ability to automatically adapt to a wide range of operating scenarios while maintaining DCM, the regulator is tested under multiple load currents with various combinations of input, output, and inductor values, including the extremes. All measurements are performed with the minimum output capacitance ($2.2\mu\text{F}$) since it produces the largest output voltage ripple. Otherwise, the output capacitor has little impact on the performance of the regulator.

Fig. 4.5 shows the transient measurement results of the inductor current I_{ind} , the output voltage V_o , and the switching node V_{sw} under different load currents and with the two extremes of the inductor range. As shown, DCM operation is preserved up to the maximum load current (40mA) for the two inductor extremes. In the case of $4.7\mu\text{H}$ inductor, it can be seen that the inductor peak current stays constant and the switching frequency increases as

the load current goes from 1mA to 10mA (Fig. 4.5a and 4.5b), which indicates AMOT operation mode. Moreover, it can be seen that the inductor peak current increases and the

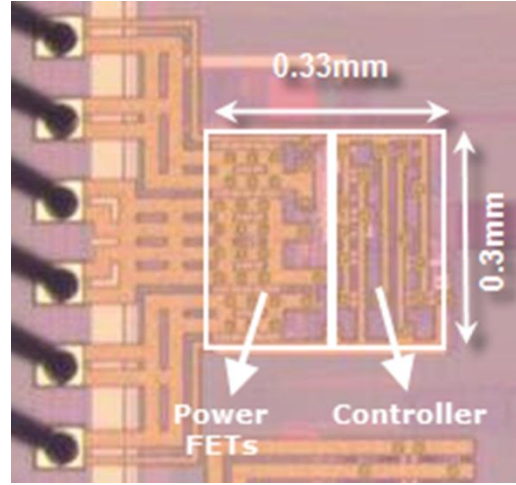


Figure 4.4. Die photo of the proposed HA-AMOT regulator showing double bonding at the input ground rails, as well as the switching node.

Table 4.1. Performance Summary

Parameter	Value	Parameter	Value
Input Voltage	1.8V-4.2V	Output Voltage	0.9V-1.4V
Min. Inductor (1210-size) Part # LQH32PN4R7NNOL	4.7 μ H with 180m Ω DCR	Min. Capacitor (0603-size)	2.2 μ F with 20m Ω ESR
Max. Inductor (1210-size) Part # ELJ-PA100KF2	10 μ H with 350m Ω DCR	Max. Capacitor (0603-size)	10 μ F with 5m Ω ESR
Load Current	≤ 40 mA	High-side and low-side FETs (single 4.2V-tolerant PMOS and NMOS respectively)	On-Resistance $\sim 0.9\Omega$ -2.1 Ω Across the entire range of PVT
Inductor Peak Current	≤ 120 mA	Ripple Voltage	≤ 30 mV
Quiescent Current (Power-Gating Enabled)	12 μ A	Quiescent Current (Power-Gating Disabled)	50 μ A
Control Comparator	Delay time (t_d) ≤ 20 ns Offset ≤ 7 mV	Zero Current Detector (ZCD)	Delay time ≤ 15 ns Offset ≤ 3 mV
Peak Efficiency	92% @ 5mA Load 1.8V input, 1.4V Output, 10 μ H Ind.	Typical Efficiency	78.5% @ 200 μ A Load 86% @ 40mA Load 3.3V input, 1.2V Output, 4.7 μ H Ind.
Maximum Switching Frequency (MHz)	2.5 @ 25mA Load 4.2V input, 1.4V Output, 10 μ F Cap.	Typical Switching Frequency (MHz)	~ 1 @ >20 mA Load 3.3V input, 1.2V Output, 2.2 μ F Cap.
Technology	5-Metal 90nm Digital CMOS	Total Converter Area	0.1mm ²

switching frequency decreases as the load current goes from 20mA to 40mA (Fig. 4.5c and 4.5d), which is consistent with the hysteretic operation mode. The same behavior is observed with a 10 μ H inductor (Fig. 4.5e through 4.5h), except that the hysteretic mode takes over at an earlier point in the load current range (less than 10mA). It is worth noting that in the hysteretic mode, the inductor operates slightly deeper in DCM rather than at the border of DCM and CCM. This is because as shown in Eq. 8, for non-zero R_{esr} and t_d , the transition between the AMOT and hysteretic modes occurs slightly earlier than the ideal case. To gain better visibility into the operation of the regulator, Fig. 4.6 shows the measured steady-state inductor peak current I_p versus the load with 4.7 μ H and 10 μ H inductors and various combinations of input and output voltages. As shown, at very light loads, the inductor peak current is constant, which is consistent with AMOT operation. Moreover, the largest inductor peak current in AMOT mode is very close to twice the maximum load current (80mA) required for DCM. Otherwise, it is always less than that. This is consistent with the AMOT scheme designed following Eq. (4.1), i.e. minimal excessive inductor peak current. Moreover, for a given inductor, the variation in the inductor peak current is limited to about $\pm 12.5\%$ despite the wide range of input and output voltages, which is a result of the adaptive operation of the AMOT pulse generator. Furthermore, for a given inductor, the transition from the AMOT to hysteretic mode shifts to higher load points as the difference between the input and output voltages decreases, which is consistent with Eq. (4.8). This transition also drops to lower load points for higher inductor values as the starting inductor peak current is lower. It is worth noting that when the input is 1.8V and the output is 1.4V, the voltage drop across the high-side power switch ($\sim 200\text{mV}$) becomes a significant portion of the overall voltage across the switch and the inductor (400mV). As a result, the inductor's charging rate

drops below its ideal value, leading to lower than normal inductor peak current in this scenario. This behavior contributes to the $\pm 12.5\%$ spread in the inductor peak current observed in the AMOT mode at light loads. It also causes the inductor peak current in the hysteretic mode at higher loads to be a weaker function of the load. This impact is clearly seen in Fig. 4.6, particularly with low inductor values. Nonetheless, this behavior has no impact on the regulator's operation as the hysteretic mode of the controller ensures enough inductor peak current to sustain the load in DCM.

The power conversion efficiency of the proposed converter versus load current is measured under various operating scenarios as shown in Fig. 4.7. For a given inductor, the best efficiency is achieved at minimum input and maximum output because this scenario yields the lowest switching losses (due to lower input voltage), the lowest conduction losses (due to lower inductor peak current), and the highest output power for a given load. Moreover, for a given input and output voltage combination, a larger inductor yields worse efficiency at sub-1mA loads as it results in lower inductor peak current, and thus higher switching frequencies. Since switching losses dominate at sub-1mA loads, higher switching frequencies yield lower efficiency. This behavior is reversed at higher loads since conduction losses dominate, and therefore, a larger inductor yields better efficiency due to the lower inductor peak current.

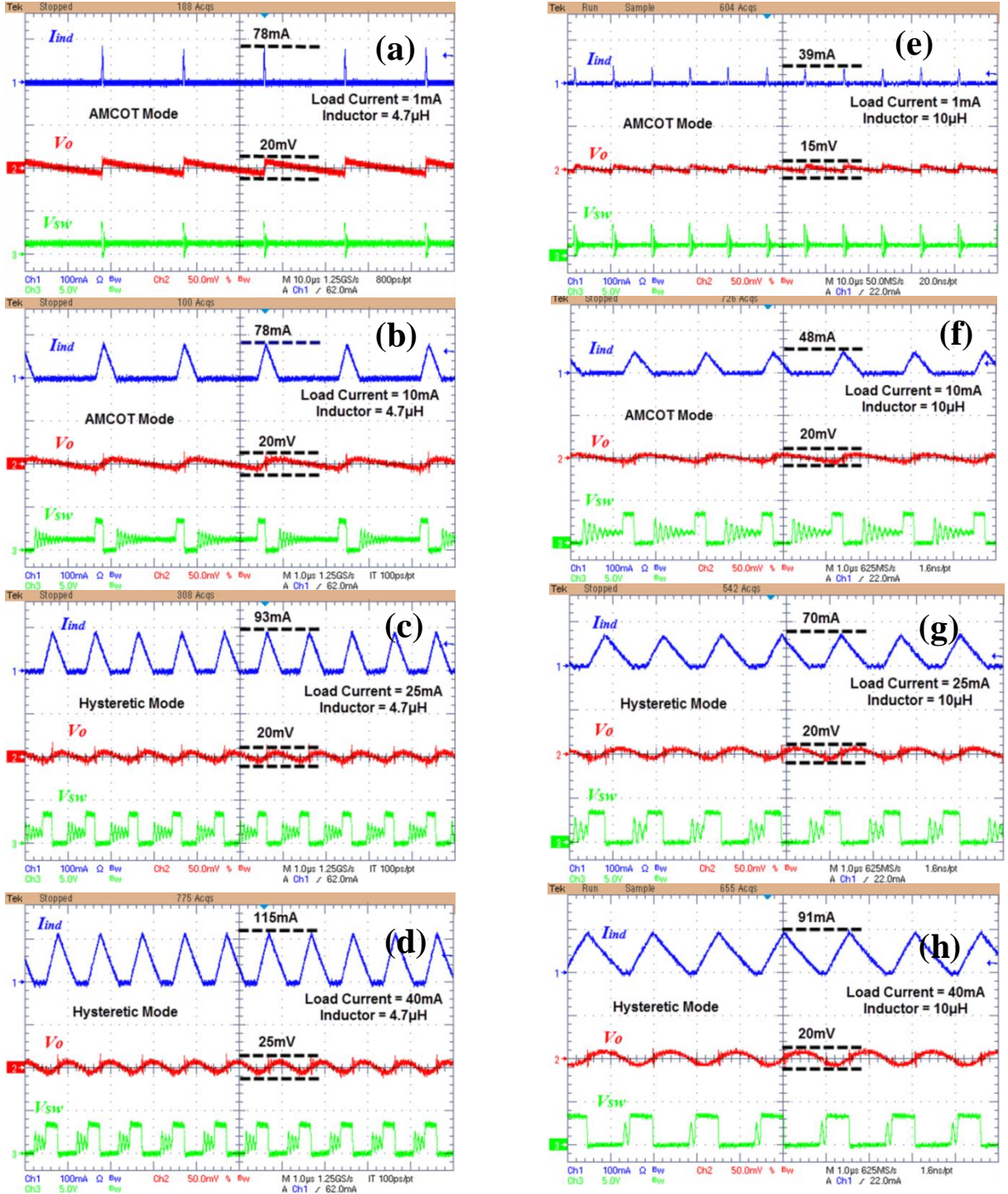


Figure 4.5. Transient measurements showing inductor current, output voltage, and switching node of the proposed regulator with 3.3V input voltage, 1.2V output voltage, and various load currents. (a), (b), (c), and (d) show the results with a 4.7 μ H inductor, while (e), (f), (g), and (h) show the results with a 10 μ H inductor.

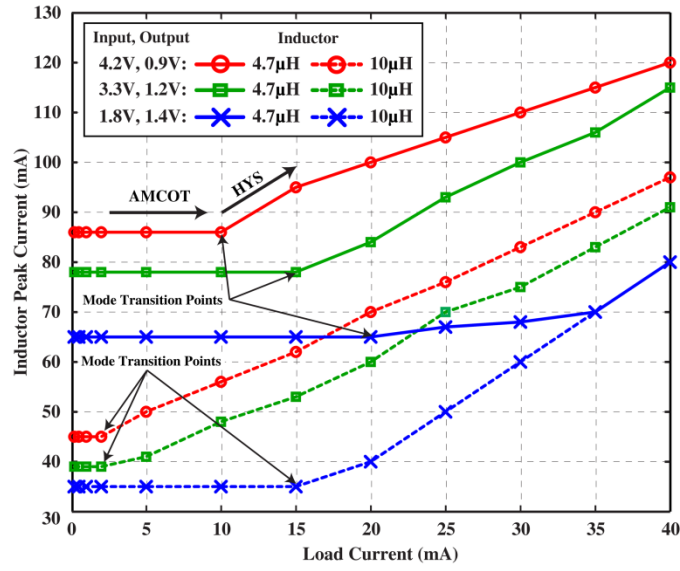


Figure 4.6. Measured inductor peak current versus load for various scenarios showing the transition points between the AMOT and hysteretic modes.

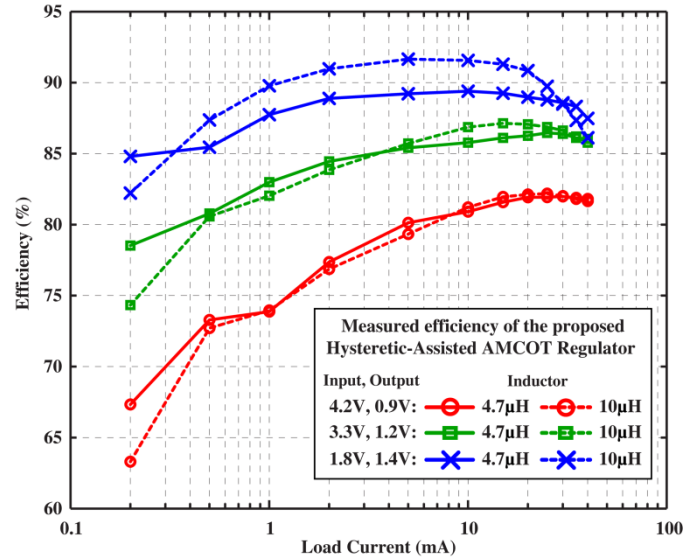
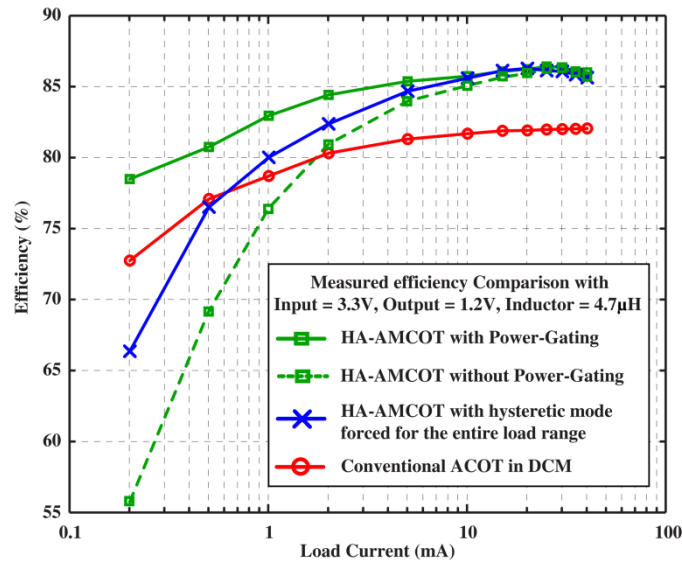


Figure 4.7. The measured efficiency versus load current of the proposed HA-AMOT regulator for various operating scenarios.



4.8. Comparison between the measured without power-gating, with hysteric mode forced across the entire load range (pure hysteric operation), and with the on-time modified to operate as a conventional ACOT controller in DCM.

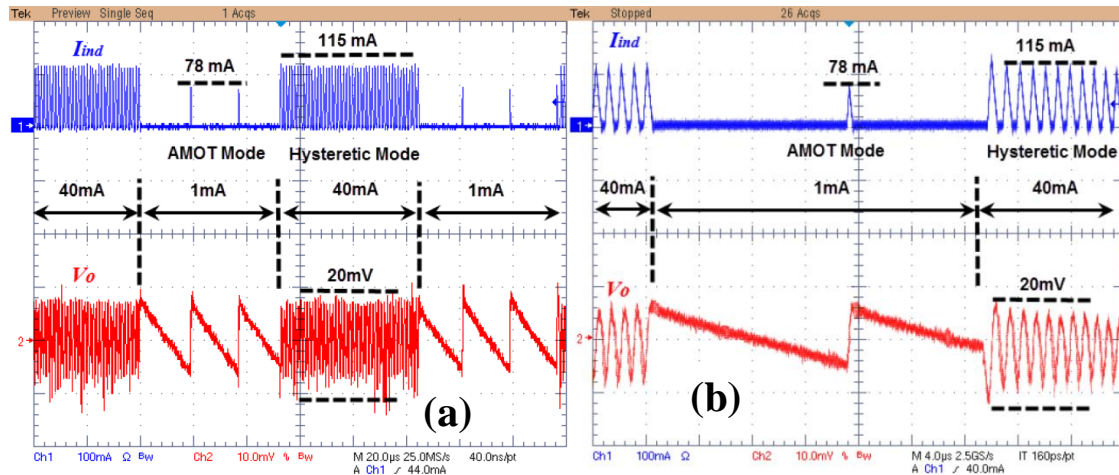


Figure 4.9. The regulator's response to a 1mA to 40mA load step with 3.3V input, 1.2V output, and 4.7 μ H inductor: (a) with a 20 μ s time scale, and (b) with a 4 μ s time scale and more frequent load efficiency using the HA-AMOT control with and **Figure**

To further demonstrate the advantages of the proposed HA-AMOT scheme, test modes were built into the regulator to force it to operate in pure hysteretic mode for the entire load range, or to increase the on-time to convert the proposed controller to a conventional ACOT controller, where as defined in section 4.2, the inductor peak current is large enough to ensure DCM for the entire load range when the maximum inductor is used. Additionally, to highlight the effectiveness of the power-gating strategy described in section 4.3, a test mode is designed to disable power-gating within the HA-AMOT controller. Fig. 8 shows a comparison between the measured efficiency versus load current for the aforementioned test modes. As shown, the proposed HA-AMOT scheme offers about 5% better efficiency across all loads compared to the conventional ACOT mode. It also offers over 12.5% better efficiency at 200 μ A load compared to the hysteretic mode alone. These results demonstrate that combining the AMOT and hysteretic modes as proposed, and automatically transitioning between them as a function of load indeed maintains DCM for a wide range of operating scenarios while yielding better efficiency than using conventional ACOT or hysteretic schemes alone. Moreover, the implemented power-gating results in efficiency improvement across all loads in general, but in particular, it results in over 22% improvement at 200 μ A load. This is due to a 75% reduction in the quiescent current when power-gating is enabled as reported in Table 4.1. The dynamic response of the regulator has also been tested for a 1mA-40mA-1mA load step. As shown in Fig. 4.9, the switching frequency increases for the higher load as expected from PFM operation, while DCM is preserved during transition. Moreover, the inductor peak current increases as expected when the controller moves from the AMOT mode at 1mA to the hysteretic mode at 40mA.

Various key performance aspects of the proposed regulator are compared to other relevant published work in Table 4.2. For objective comparison, efficiency is compared with the closest possible input, output, and inductor reported in the references in the 0-40mA load range. The exact operating conditions are reported in the table for each reference. Since some of the other references are targeting much heavier loads than 40mA, comparison of efficiency and quiescent current is done with the performance reported using the light-load controllers in these references. It is important to note that information about the physical footprint of the inductor is necessary for a fair comparison between different regulators as a smaller footprint results in larger series resistance (DCR) and lower efficiency. This information is reported only in [6], and in comparison, the proposed regulator offers comparable efficiency with a much smaller inductor footprint. Other notable features of the proposed regulator include the wide range of input voltage and passive components values compared to other work. It also offers a small die area, which is attributed to two factors. First, the AMOT and hysteretic modes utilize the same circuit blocks. Second, operating close to the DCM-CCM border towards the high end of the load range enables optimizing efficiency with the smallest possible power switches.

Table 4.2 Performance Comparison with other Published Work

	Proposed Work	[6]	[7]	[10]	
Technology	90nm	45nm	0.25um	0.18um	
Light-load Control Method	Voltage-Mode HA-AMCOT (PFM)	Voltage-Mode COT (PFM)	Voltage-Mode Digitally- Controlled COT (PFM)	Digitally-Controlled Current- Mode (PWM) with Dynamic Power FET Segmentation	
Max Load (mA)	40	15 with only light-load controller	40 with only light-load controller	60 with only light-load controller	
Quiescent Current (μA)	12	Not Reported	4	250 (at 50mA load)	
Die Area (mm ²)	0.1	2.25 includes an additional PWM controller for loads > 15mA	2 includes an additional PWM controller for loads > 40mA	3.375 same controller for all loads	
Controller Area (mm ²)	0.06	0.07 (includes an additional PWM controller for loads > 15mA)	Not Reported	0.077	
Input Voltage Range (V)	1.8-4.2	2.8-4.2	2.8-5.5	2.7-4.2	
Output Voltage Range (V)	0.9-1.4	0.4-1.2	1-1.8	1-1.8	
^(*) Inductor Range (μH)	4.7-10 (3.2mm x 2.5 mm)	10 (10mm x 10mm)	47 (footprint not reported)	2 (footprint not reported)	
Output Capacitor Range (μF)	2.2-10	2	4.7	4.7	
Efficiency (%)	^(*) Conditions	V _{in} = 3.3V, V _o = 1.2V, L = 4.7μH, DCR = 180mΩ	V _{in} = 3V, V _o = 1V, L = 10μH, DCR = Not Reported	V _{in} = 4V, V _o = 1.5V, L = 10μH, DCR = Not Reported	V _{in} = 3.6V, V _o = 1.8V, L = 2μH, DCR = Not Reported
	IL = 200μA	78.5	82	77	Not Reported
	IL = 1mA	83	83.5	80.5	75
	IL = 10mA	85.7	87	85	75
	IL = 40mA	85.6	87.3 (with PWM)	87	75
	Peak (0-40mA load)	86.2	87.4	88	75

(*) Inductors used in this work have much smaller footprint than in [6], which results in larger DCR and larger conduction losses, hence slightly lower efficiency.

4.5 Conclusion

A Hysteretic-Assisted Adaptive Constant On-Time control scheme for buck regulators in low-power microcontrollers has been presented. The proposed scheme forces DCM-only operation for the entire load range, and thus stability is guaranteed with no loop compensation. It automatically adapts itself to a wide range of operating scenarios such that DCM operation is always maintained with the minimum possible inductor peak current for a given load. As a result, losses are minimized and high efficiency can be achieved for a wide range of input and output voltages and passive components. A power-gating scheme is implemented in all the analog blocks of the controller to reduce the quiescent current by 75%, which results in 22% efficiency improvement at 200 μ A load. The proposed scheme yields better efficiency across the entire load range than conventional ACOT or hysteretic

control alone. The regulator allows low-power microcontrollers to handle a wider range of potential applications through supporting various powering options and passive component selections.

4.6 References

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CHAPTER V. CONCLUSION

In this thesis, we have discussed several topics on power conversion schemes for low power application in nanometer CMOS technology, from theory to circuit's implementations.

In chapter 2, we provide comprehensive analysis and modeling of switching and conduction losses in low-power synchronous buck regulators in both CCM and DCM modes of operation including the case with non-rail gate control of the power FETs.

In chapter 3, a fully-integrated buck regulator with on-chip passives in 65nm standard CMOS technology is presented. The proposed regulator switches at 588MHz and uses a 20nH on-chip inductor and a 300pF on-chip output capacitor. It operates from 1.8V input and produces an output in the range between 0.8V to 1.2V with maximum load current of 30mA.

In chapter 4, we present a 40mA buck regulator operating in the inherently stable Discontinuous Conduction Mode (DCM) for the entire load range. A Pulse Frequency Modulation (PFM) control scheme is implemented using a proposed Hysteretic-Assisted Adaptive Minimum On-Time (HA-AMOT) controller to automatically adapt the regulator to a wide range of operating scenarios in terms of input, output, and passive component values while ensuring compensation-less DCM operation with minimized inductor peak current.

In this chapter, we will present some new ideas on fully integrated buck regulator for improved performance and lower cost.

5.1 Fully Integrated DC-DC Buck Converter in DCM/PFM Scenario

In chapter 3, we have discussed and proposed a fully integrated DC-DC buck converter operating in CCM scenario with on-chip passives to replace linear regulators in nanometer mixed-signal SoC so as to improve the power/thermal efficiency of the whole chip. However, several conditions have to be met so as to achieve the purpose of the work. First of all, a high frequency clock(~ 500 MHz) is required so as to support the voltage mode, PWM operation. Such a requirement may increase the total overhead of the SoC since not all the SoCs can provide such a clock at this particular frequency without any overhead. Second, a relative high quality on-chip inductor is needed so as to maintain the power efficiency of the regulator. To implement such an on-chip inductor, we need at least one thick metal layer or several metal layers to stack, as well as some doping limitation on the substrate to reduce the eddy current effect. Those requirements may not be applicable to all the process. Lastly, the buck converter operating in CCM scenario can not achieve good power efficiency at light load condition due to excessive switching losses at sub 5mA. Moreover, during the phase when NMOS powerFET is on, the inductor current will flow back into the powerFET once the load is less than 20mA, which also degrade the power efficiency of the converter. In this chapter, we will briefly discuss the feasibility of building a fully integrated DC-DC buck converter in DCM scenario to mitigate the issues discussed above.

Based on the discussion above showing the potential issues with the proposed fully integrated buck regulator operating in CCM scenario, having the buck converter operating in DCM/PFM scenario has several advantages.

First of all, the DCM/PFM buck regulator is famous for its light load efficiency improvement over CCM/PWM buck regulator. The reason is the DCM/PFM buck regulator is operating with fixed on-time while the switching frequency is scalable with respect to the load. In such case, the switching frequency can be tremendously reduced once the load drops below sub 1mA. Thus, the switching losses and conduction losses of the converter can be re-balanced so as to achieve the optimum power efficiency across a much wider range in the proposed specification.

Second, the DCM/PFM buck regulator does not require a clock for its operation. The only timing related block is a timer for the on-time pulse generator, which can be implemented with a R-C timer or I-C timer. Although there is published work on DC-DC buck regulator with internal clock generator for CCM/PWM scenario [1], such a clock generator requires at least two comparators which is very difficult to implement (power consumption is too high) if the frequency of the regulator is higher than 100 MHz. Thus, having a buck regulator working around 100 MHz without clock is the best choice for both power efficiency and silicon area overhead.

Finally, the size/value of the on-chip inductor can be reduced with DCM/PFM buck regulator [2]. Based on the limitation of the process of the proposed buck regulator discussed in chapter 3, the DCR of the on-chip inductor is more than 7 Ohm, which dominates the power loss of the whole regulator. The best way to reduce the DCR of the on-chip inductor is to reduce the value/size of the inductor since the DCR is mainly due to the winding of the inductor. By operating the buck regulator in DCM/PFM scenario, both area and inductor related power loss can be reduced, which is a big factor why DCM/PFM buck regulator is advantageous for such an application.

However, there are several technique difficulties to implement a fully integrated DCM/PFM buck regulator. First of all, the DCM/PFM buck regulator relies on a much bigger output capacitor to reduce the voltage ripple comparing to a CCM/PWM buck regulator in similar scenario. Thus, it may require the process to have high density poly-nwell capacitor so as to mitigate the area overhead. Second, DCM/PFM buck regulator requires a zero current detector(ZCD) to turn off low-side PowerFET when inductor current drops to zero. For a high frequency DCM/PFM buck regulator, such ZCD needs to have a delay that is less than a fraction of nano second since the frequency of operation is beyond 100 MHz. Such a fast ZCD is very difficult to implement with limited power budget. Finally, DCM/PFM buck regulator is much more noisy than its CCM/PWM counterpart due to EMI(the switching node oscillates during the idle time). The noise may get coupled to other blocks inside the SoC, causing performance degradation or even functionality failure of other blocks.

In conclusion, a fully integrated DCM/PFM buck regulator is very attractive due to several features discussed above, which have the potential to further improve the power efficiency of the system while reducing the overhead. However, there are several technical difficulties in the meanwhile which need special attention as well as technical solutions.

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