A simple bandgap reference based on V_{GO} extraction with single-temperature trimming

by

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The student author, whose presentation of the scholarship herein was approved by the program of study committee, is solely responsible for the content of this thesis. The Graduate College will ensure this thesis is globally accessible and will not permit alterations after a degree is conferred.

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DEDICATION

To my family, professors and friends

who have supported me during my college studies.

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LIST OF ACRONYMS

OP AMP	Operational Amplifier
BJT	Bipolar Junction Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PMOS	P-type MOSFET
NMOS	N-type MOSFET
PTAT	Proportional to Absolute Temperature
CTAT	Complementary to Absolute Temperature
TC	Temperature Coefficient
SoC	System on Chip

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ABSTRACT

Bandgap references are widely used in analog and mixed-signal systems to provide temperature-independent voltage or current reference. In traditional bandgap structure, the base-emitter voltage V_{BE} of a diode is used to generate a complementary to absolute temperature (CTAT) voltage, which reduces as temperature increases. The base-emitter voltage difference ΔV_{BE} between two diodes with the same current but different emitter areas supplies a proportional to absolute temperature (PTAT) voltage. With the proper adjustment of the coefficients of V_{BE} and ΔV_{BE} in a voltage summer, the temperature dependency of the summed voltage can be mostly canceled out and the output voltage can achieve a relative temperature-constant property. However, even though the linear terms of temperature-dependent components in PTAT and CTAT expressions can be canceled out, there are still some high order terms left, which still affect temperature dependency. For this reason, a first-order bandgap reference with only PTAT and CTAT linear term compensation cannot achieve a sufficiently low temperature coefficient (TC), normally ranging from 10ppm/°C to over 100ppm/°C. To achieve higher precision and lower TC, the high order terms also need to be considered and compensated by some techniques. This thesis study describes the development of a high order bandgap structure, including the initial thinking, design flow, equation derivation, circuit implementation, and simulation result.

CHAPTER 1. INTRODUCTION

1.1 Bandgap Reference Overview

The goal of a voltage reference is to generate a stable voltage that is ideally independent of changes in temperature and other external factors (https://www.allaboutcircuits.com/technical-articles/introduction-to-bandgap-voltage-references/). Unfortunately, environment temperature can affect the properties of the different components within a circuit, such as the base-emitter voltage of a BJT. Base-emitter voltage has a nearly linear relationship with absolute temperature and exhibits a temperature coefficient of about –2mV°/C, which will affect the circuit output. Without improving the device in the material level and achieving a smaller temperature coefficient, we need to somehow compensate for this negative temperature coefficient. For example, if we can generate a voltage that has a linear relationship with temperature and exhibits a temperature coefficient of about +2mV°/C, then we can compensate the temperature-induced variation introduced by the base-emitter junction. In 1964, Hibiber [1] observed that two diodes biased at different current densities can provide a temperature-independent voltage (Figure 1.1). A year later, Widlar [2] showed that the base-emitter voltages of two BJTs biased at different current densities had a difference that is proportional to absolute temperature (PTAT), and in 1971 introduced the first bandgap circuit. In 1973 and 1974, Kujik [3] (Figure 1.2) and Brokaw [4] proposed another two bandgap structures with higher precision. Nevertheless, it has remained a crucial problem for high precision applications regarding how to acquire a high precision bandgap reference.

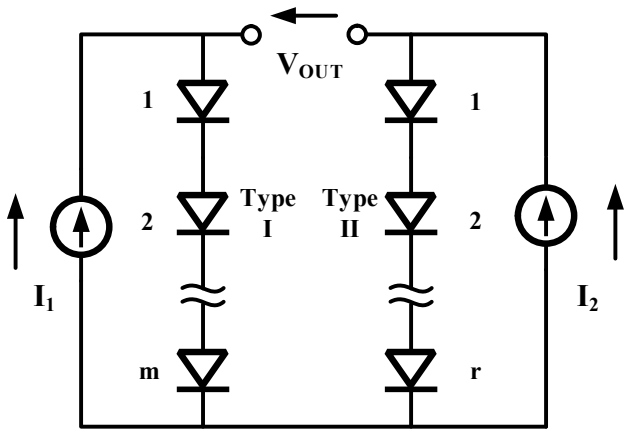

Figure 1.1. Hibiber's Two Diode Structure

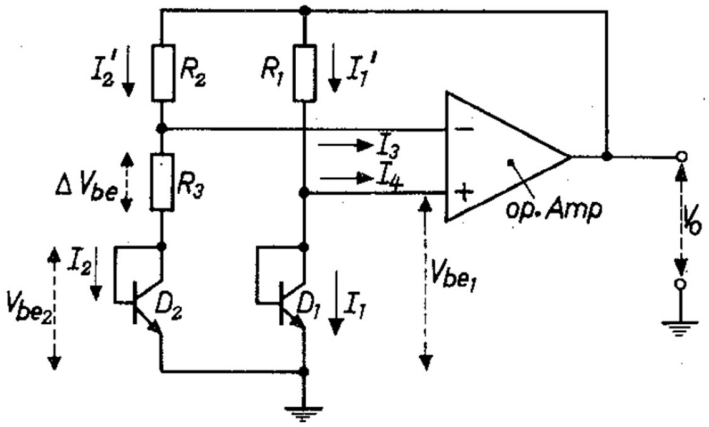

Figure 1.2. Kujik's Bandgap Structure

1.2 Bandgap Theory Review

As we know, the I-V relationship for a diode-connected BJT can be expressed as

$$I_C(T) = I_S(T)e^{\frac{qV_{BE}}{kT}} = J_{SX}AT^{\eta}e^{-\frac{qV_G(T)}{kT}}e^{\frac{qV_{BE}}{kT}} \quad (1)$$

where J_{SX} is current density, A is the junction area, η is a process-dependent parameter, k and q are physical constants, and $V_G(T)$ is the silicon bandgap voltage with change of temperature. If we rearrange Eq. (1), the base-emitter voltage V_{BE} change with temperature and at a particular temperature T_r can be expressed as

$$\begin{aligned} V_{BE}(T) &= \frac{kT}{q}\ln\frac{I_C(T)}{I_S(T)} \\ V_{BE}(T_r) &= \frac{kT_r}{q}\ln\frac{I_C(T_r)}{I_S(T_r)} \end{aligned}. \tag{2}$$

Where T_r is reference temperature, and is chosen at room temperature here. By subtracting these two equations and rearrange the result, we can get

$$\begin{aligned} V_{BE}(T) - \frac{T}{T_r}V_{BE}(T_r) &= \frac{kT}{q}\left(\ln\frac{I_C(T)}{I_S(T)} - \ln\frac{I_C(T_r)}{I_S(T_r)}\right) \\ V_{BE}(T) &= \frac{T}{T_r}V_{BE}(T_r) + \frac{kT}{q}\left(\ln\frac{I_C(T)}{I_S(T)}\frac{I_S(T_r)}{I_C(T_r)}\right) \end{aligned}. \tag{3}$$

By replacing the I_S with the expression (1), we can get a new equation such as

$$V_{BE}(T) = V_G(T) - \frac{T}{T_r}V_G(T_r) + \frac{T}{T_r}V_{BE}(T_r) - \eta\frac{kT}{q}\ln\left(\frac{T}{T_r}\right) + \frac{kT}{q}\ln\left[\frac{I_C(T)}{I_C(T_r)}\right]. \tag{4}$$

In 1980, Tsividis [5] introduced an accurate analysis of temperature effects in I_C-V_{BE} characteristics. Tsividis posited there are three terms in V_{BE}, including: (1) a constant term, V_{GOr}, which is the extrapolated bandgap voltage at 0 K; (2) a linear term which is proportional to temperature (CTAT); and (3) a nonlinear higher-order term (curvature).

In Tsividis's paper, the assumed variable V_{GOr} is the intersection of temperature at 0K with a linear function that passes through the actual bandgap voltage $V_G(T)$ at temperature T_r as a tangent line (Figure 1.3). Based on this assumption, the bandgap voltage $V_G(T)$ can be written as

$$\begin{aligned} V_G(T) &\approx V_{GOr} + \varepsilon_r T \\ V_G(T_r) &\approx V_{GOr} + \varepsilon_r T_r \end{aligned}. \tag{5}$$

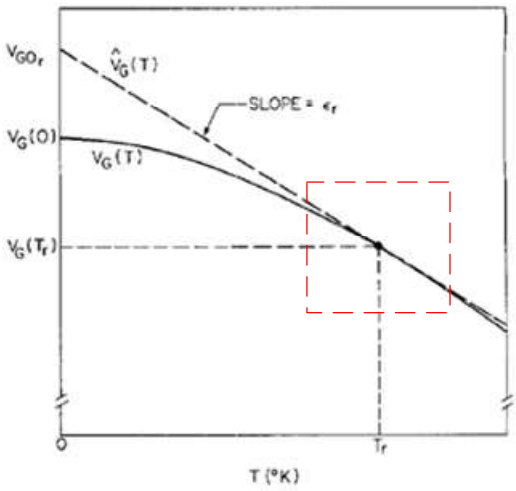

Figure 1.3. The Extrapolated Bandgap Voltage V_{GOr}

One factor that needs to be noticed is the value of V_{GOr} is not unique, but depends on the reference temperature T_r, at which the straight line is tangent to the curve. Figure 1.3 shows that the approximation straight line fits the original bandgap voltage $V_G(T)$ curve around the reference temperature T_r, but has a poor accuracy at 0K, which is due to the nonlinearity of bandgap voltage $V_G(T)$ at low temperature. In a given temperature range, this error alone can cause several to over 10 ppm/°C temperature coefficient. Nevertheless, the tangent line approximation is simple and is widely used in the literature and in industry.

By using the approximation of $V_G(T)$ and $V_G(T_r)$ in expression (5), Eq. (4) can be changed as

$$V_{BE}(T) \approx V_{GOr} + \left[V_{BE}(T_r) - V_{GOr}\right]\frac{T}{T_r} - \eta\frac{kT}{q}\ln\left(\frac{T}{T_r}\right) + \frac{kT}{q}\ln\left[\frac{I_C(T)}{I_C(T_r)}\right]. \quad (6)$$

Eq. (6) is a widely used V_{BE} expression for the curvature compensation technique. In Eq. (6), the first term V_{GOr} is a constant value with respect to temperature T. The second term is a linear CTAT term and can be easily compensated by a PTAT voltage. The remaining two terms

are high order non-linear function of T, which are not easy to be removed. The question of how to obtain a precision bandgap reference can then be transferred to how to extract an accurate V_{GOr} and how to cancel the high order terms. Notice that in Eq. (6) there are two high order nonlinear terms (the third and fourth terms) and, if the collector current I_C of the BJT is proportional to T^{δ}, the two terms can be further simplified into a single Tln(T) term, leading to a simplified equation

$$V_{BE}(T) \approx V_{GOr} + \left[V_{BE}(T_r) - V_{GOr}\right]\frac{T}{T_r} - (\eta - \delta)\frac{kT}{q}\ln\left(\frac{T}{T_r}\right). \tag{7}$$

However, as mentioned previously, the linear assumption of Eq. (5) is not very accurate since there are still some high order residues following up with the linear term, as well as some errors from different sources. Instead of the tangent line, if we use a best combination of a constant value, a PTAT term, and a high order Tln(T) term to approximate the $V_G(T)$ curve in the interested temperature range, we can re-write the $V_G(T)$ expression as follows:

$$V_G(T) = V_{GO1} + aT + bT\ln(T/T_r) + \varepsilon(T). \tag{8}$$

where $\varepsilon(T)$ is the difference between $V_G(T)$ and the 3-term best fit curve. For the $V_G(T)$ curve as illustrated in Figure 1.3, the value of a is slightly dependent on the reference temperature T_r, but V_{GO1} and b are both relatively constant with respect to commonly used T_r. In fact, V_{GO1} is very close to $V_G(0) = 1.16$. Similarly, the term $\varepsilon(T)$ is numerically evaluated to be very small over any commonly used temperature ranges and, if ignored, only causes an error in the order of magnitude of 0.3 to 0.5 ppm/C in the extraction output.

By substituting this new equation into Eq. (4), we can get a new equation for V_{BE} that can be written as

$$V_{BE}(T) = V_{GO1} + \varepsilon(T) + \left[V_{BE}(T_r) - V_{GO1} - \varepsilon(T_r)\right]\frac{T}{T_r} - [\eta - \delta - b\frac{q}{k}]\frac{kT}{q}\ln\left(\frac{T}{T_r}\right) . \quad (9)$$

After applying a PTAT trimming on the linear term and a curvature correction on TlnT term, there will be only the $V_{GO1} + \varepsilon(T)$ term remaining, which has a less than 0.5 ppm/°C temperature coefficient. However, in this implementation we use simple on-chip cancellation circuit, which will not be perfect. This will lead to additional errors due to non-idealities in the simple circuit. Our goal is to limit these errors to be only a few times the ideal case errors. Thus, our trimming target is V_{GO1} instead of $V_{GO} + \varepsilon(T)$, and the reference output voltage is about a few ppm/°C over typical temperature ranges. Bandgap reference trimming will be discussed in next section.

1.3 Bandgap Reference Trimming

The output of the bandgap reference will vary from chip to chip because of process variation. Due to process variation, the bandgap circuit is not operating with the designed current or voltage. It will produce a different value and curvature over temperature. Trimming adjusts the resistor value and, hence, the current flowing through it, and eventually makes the reference voltage and temperature performance back to the design intent (https://www.allaboutcircuits.com/ technical-articles/introduction-to-bandgap-voltage-references/). Normally, a binary distributed resistor ladder is applied for trimming. By setting the different trimming code, the resistor value changes, respectively, so that the trimming target can then be achieved. Based on the precision of the trimming target or the design complexity of the circuit, the number of trimming steps may vary a lot. Trimming is commonly used at two different temperatures or multiple different temperatures. However, comparing to trimming at two temperatures [7], or at multiple different temperatures [10], which consumes more time and

measurement cost, just trimming at room temperature can be a lot easier and cheaper as well. To achieve a goal with simplicity as the priority, a single temperature trimming method is adopted. In industry, digital calibration and trimming with laser are also used, but will not be introduced in this thesis.

1.4 Curvature Correction Approaches

As mentioned in Section 1.2, to extract a relatively temperature constant V_{GO1}, the high order TlnT term in the V_{BE} equation, which behaves like a curvature, has to be canceled out. Some curvature correction approaches were introduced in [6-8]. Andreou et al. [6] introduced a curvature compensated bandgap reference that is introduced by adding a CTAT current to it. The CTAT current is generated by another bandgap reference. However, adding an additional bandgap reference requires more diodes and op-amps and makes the structure complex. A sub-ppm/°C precision bandgap reference was introduced by Liu [7]. In that structure, five op-amps have been used which consumes die area and power. Furthermore, they can introduce more offset errors that can propagate to reference output. Based on the analysis of bandgap reference error sources introduced by Ge et al. [8], the op-amp offset has the highest error contribution among all error sources. Due to its non-PTAT property, it cannot be removed by PTAT trimming. Chopping and autozeroing techniques that can remove offset errors have been introduced by Enz et al. [9]. A bandgap reference using the chopping technique to remove op-amp offset was proposed in [8]. However, new errors which can degrade circuit performance are introduced. For example, the input impedance of the regulating op-amp in the bandgap core is reduced due to chopping and can result in current errors in the diodes. Moreover, small voltage ripples appear when either one of the two techniques is applied and further filtering methods are needed. Therefore, this contradiction indicates that a simple structure with the minimum number of op-amps is appreciated.

A simpler structure to extract V_{GO1} was proposed in this thesis study. A Gm-cell based voltage summer was implemented and a simple voltage-to-current converter was used. The number of op-amps used were reduced significantly without sacrificing the temperature drift performance too much. A single temperature trimming method was explained as a way to trim out PTAT errors in V_{BE} and calibrate the summer's gain.

The remainder of the thesis is organized as follows: Chapter 2 shows the previous work, the motivation for improvement, and the proposed structure; Chapter 3 gives some reviews of mismatch and offset, and shows how offset affects the performance of the proposed bandgap reference, and the solution and offset optimization are presented at the end of Chapter 3; A single temperature trimming method is implemented in Chapter 4, with details of the proposed trimming method listed step by step as well as the limitations of its use presented at the end of the chapter. Chapter 5 provides a discussion as well as suggestions about directions for further research, and Chapter 6 provides a conclusion to this thesis study.

CHAPTER 2. A SIMPLIFIED BANDGAP REFERENCE

2.1 Previous Work

2.1.1 Circuit Implementation

As mentioned in the previous chapter, several curvature correction approaches have been proposed, and each has its disadvantages. In Liu's [7] bandgap reference (Figure 2.1), five op-amps are used to achieve a sub-ppm/°C; however, based on op-amp usage, there is a greater power consumption, larger die area, and more offset propagating to the output. The proposed bandgap structure in this thesis study attempts to simplify the structure used in [7] by reducing the number of op-amps without scarifying too much precision.

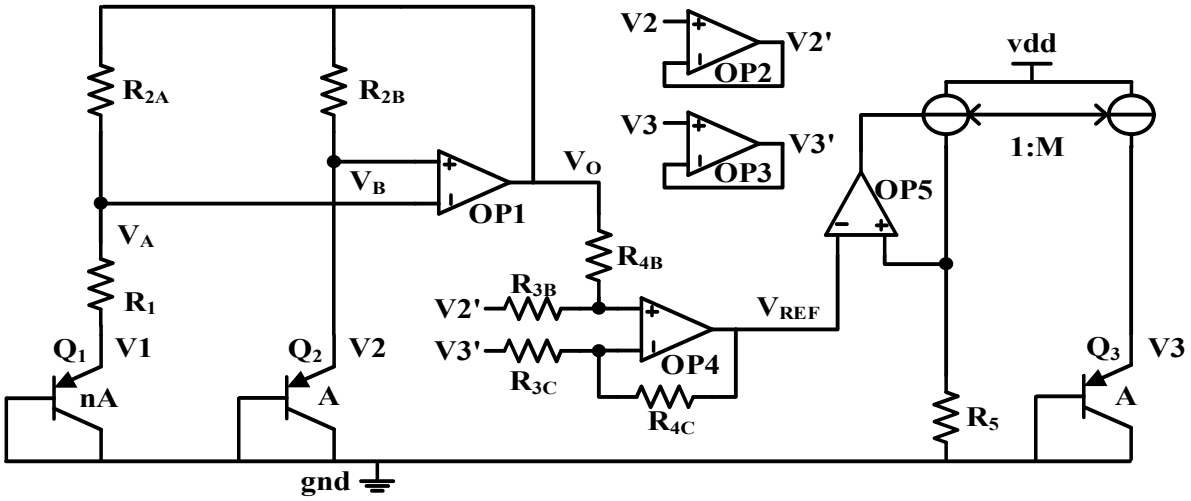

Figure 2.1. Liu's Bandgap Structure

In Liu's structure, a new output V_{REF} is used to generate a constant current I_3 which is sent to a third diode Q_3. The corresponding V_{BE3} is compared to V_{BE2} and their difference is added with Kuijk output to extract the V_{GO1}. By using the equations in the Bandgap Theory Review section, V_{BE2} in this structure can be simply written as

$$V_{BE}(T) = V_{GO1} + \varepsilon(T) + \left[V_{BE}(T_r) - V_{GO1} - \varepsilon(T_r)\right]\frac{T}{T_r} - [\eta - 1 - b\frac{q}{k}]\frac{kT}{q}\ln\left(\frac{T}{T_r}\right). \quad (10)$$

Compared to Eq.(9), δ is equal to 1 in this case because its collector current I_2, which is generated by the Kujik core, is a PTAT current. Since the collector current of third diode I_3 is temperature constant. Therefore, we can express the relationship between I_2 and I_3 as

$$I_2 / I_3 = a_1 * T^{\alpha}, \quad (11)$$

where a_1 is a temperature independent coefficient, and α is equal to 1 because of the properties of I_2 and I_3 in this case. Therefore, the V_{BE} difference of V_{BE2} and V_{BE3}, which could be trimmed to be equal at T_r and used to compensate for the TlnT term, can be derived as

$$\begin{aligned}\Delta V_{BE3,2} &= \left(V_{BE3}(T_r) - V_{BE2}(T_r)\right)\frac{T}{T_r} - \frac{kT}{q}\ln(\frac{T}{T_r}) \\ &= -\frac{kT}{q}\ln(\frac{T}{T_r})\end{aligned}. \quad (12)$$

By applying the V_{BE} equation in (2), the PTAT voltage difference of V_{BE1} and V_{BE2} in can be derived as

$$\Delta V_{BE2,1} = \frac{kT}{q}\ln(n). \quad (13)$$

To extract V_{GO1}, we would like

$$V_{REF} = A_1 V_{BE2} + A_2 \Delta V_{BE2,1} + A_3 V_{BE3,2} = V_{GO1} \quad (14)$$

where:

$$\begin{aligned}A_1 &= 1 \\ A_2 &= \frac{q}{kT_r \ln(n)}\left((\eta - 1 - b\frac{q}{k}) * [V_{BE3}(T_r) - V_{BE2}(T_r)] - [V_{BE2}(T_r) - V_{GO1}]\right). \\ A_3 &= -(\eta - 1 - b\frac{q}{k})\end{aligned} \quad (15)$$

In the circuit, V_{REF} can be represented as

$$V_{REF} = V_{BE2} + \frac{R_2}{R_1}(V_{BE2} - V_{BE1}) + \frac{R_4}{R_3}(V_{BE2} - V_{BE3}) . \quad (16)$$

R_5 can be selected so that $V_{BE3}(T_r)=V_{BE2}(T_r)$, which can make Eq. (15) to be further simplified. After simplification and applying values of A_2 and A_3 into Eq. (16), the resistor ratios can be calculated as below to make $V_{REF} \approx V_{GO1}$.

$$\begin{aligned} \frac{R_2}{R_1} &= -\frac{q}{kT_r \ln(n)}[V_{BE2}(T_r) - V_{GO1}] \\ \frac{R_4}{R_3} &= \left(\eta - 1 - b\frac{q}{k}\right) \end{aligned} . \quad (17)$$

2.1.2 Trimming Method

In Liu's work [7], a two-temperature trimming method is implemented. The method can be organized as follows:

1. At room temperature T_r, trim R_5 to make $V_{BE3}(T_r)=V_{BE2}(T_r)$, so that $\triangle V_{BE3,2}$ is 0V at T_r.
2. Still, at room temperature, sweep R_{2A} and R_{2B} until $V_{REF} = V_{GO1}$ with R_{4B} and R_{4C} unchanged.
3. After R_{2A} and R_{2B} are trimmed, change the environment temperature to a hot temperature, e.g., 100°C. R_{4B} and R_{4C} are swept until $V_{REF} = V_{GO1}$. V_{REF} at T_r is not changed here as $\triangle V_{BE3,2}$ is trimmed to be 0V and has no effect on V_{REF} at T_r.

By applying this method, appropriate calibrating the coefficient R_2/R_1, the PTAT term in V_{BE2} can be canceled out, and by adjusting the coefficient of R_4/R_3, the TlnT term in it can also be compensated. In this V_{GO1} extraction method, a sub-ppm temperature coefficient can be obtained, which is sufficiently precise. However, five amplifiers are used in this structure to achieve high precision, which consumes a large die area. Two buffer-connected amplifier OP2 and OP3 are required to prevent currents flowing from Vo back to Q_2 and Q_3. The OP4 is used to sum Vo and V_{REF}, and OP5 is for regulating two voltages.

To simplify the structure, we can see that, if V_{BE2} and V_{BE3} are directly connected to the CMOS gate, there will be no current flow and the buffer OP2 and OP3 can be removed. Further, if a source-follower based V-to-I converter is implemented without sacrificing the accuracy too much, voltage regulating amplifier OP5 can be replaced and the die area will be further reduced. The difference amplifier OP4 can also be replaced by a new Gm-cell based summer. With all of these changes, a new structure is then proposed in the next section.

2.2 Proposed V_{GO1} Extraction Method

2.2.1 Kujik Core

A modified Kujik core is shown in Figure 2.2. Compared to the previous Kujik core, the output voltage generated by the op-amp in the modified Kujik core is used to bias the top transistor M0. A temperature constant current from the V-to-I converter, which will be discussed below, is mirrored as the biasing current for the op-amp. Since there is negative feedback from the gate to the drain of M0, the positive and negative terminals of the op-amp need to be inverted to maintain the same polarity, and a capacitor is also needed to stabilize the system. The design and optimization details of the om-amp will be discussed in Section 3.4.

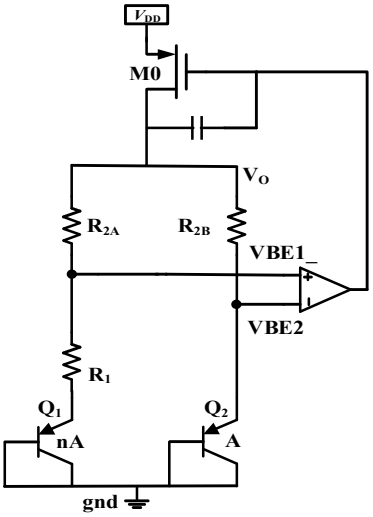

Figure 2.2. Kujik Core

2.2.2 Voltage-to-Current Converter

A simpler V-to-I converter is shown in Figure 2.3. In the proposed structure, a PMOS source follower is combined with an NMOS source follower to make V_C track V_{REF}. By carefully sizing and applying the same current to M1 and M2, the $V_{GS,p}$ rise on M1 and $V_{GS,n}$ drop on M2 can be canceled with each other. Resistor R_6 converts the voltage V_C to a temperature constant current which is further fed into the emitter of Q_3 to generate V_{BE3}. Although the threshold voltage Vth of PMOS and NMOS are different, and the Vth changing rate via temperature is also different, the V_{th} difference between PMOS and NMOS changes slightly via temperature in UMC65. In Figure 2.4 we can see that the Vth of each NMOS and PMOS changes about 120mV from -40°C to 125°C. However, the Vth difference between them changes only about 3mV via the whole temperature range, which verifies our previous statement.

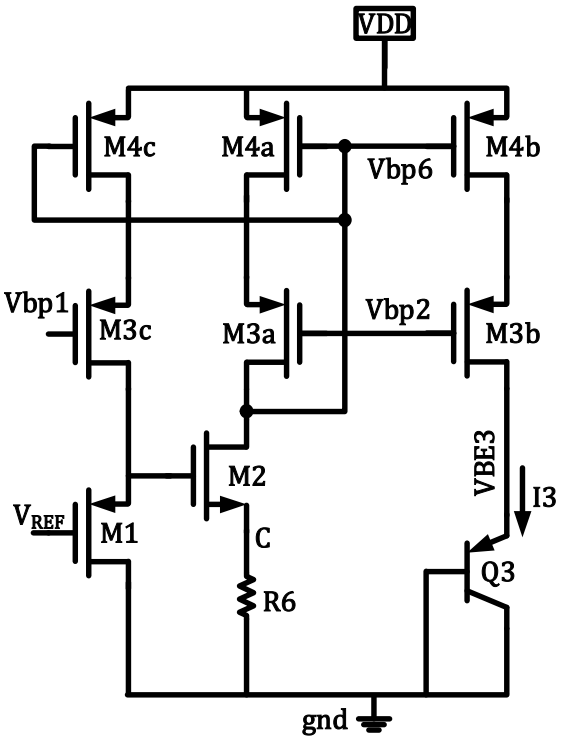

Figure 2.3. V-to-I Converter

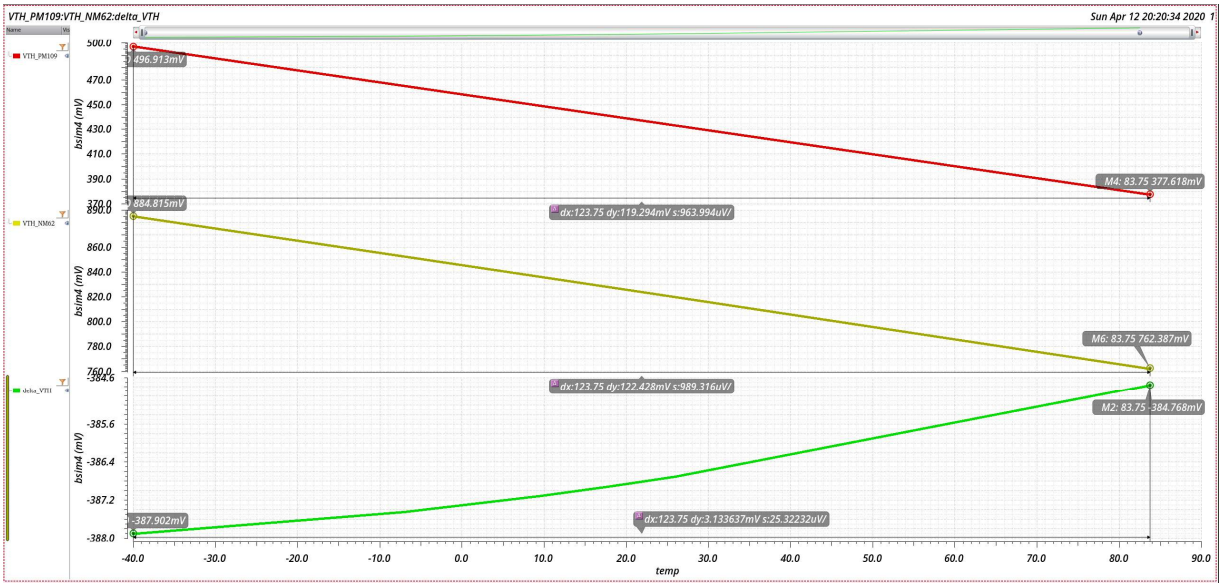

Figure 2.4. Vth Change with Temperature

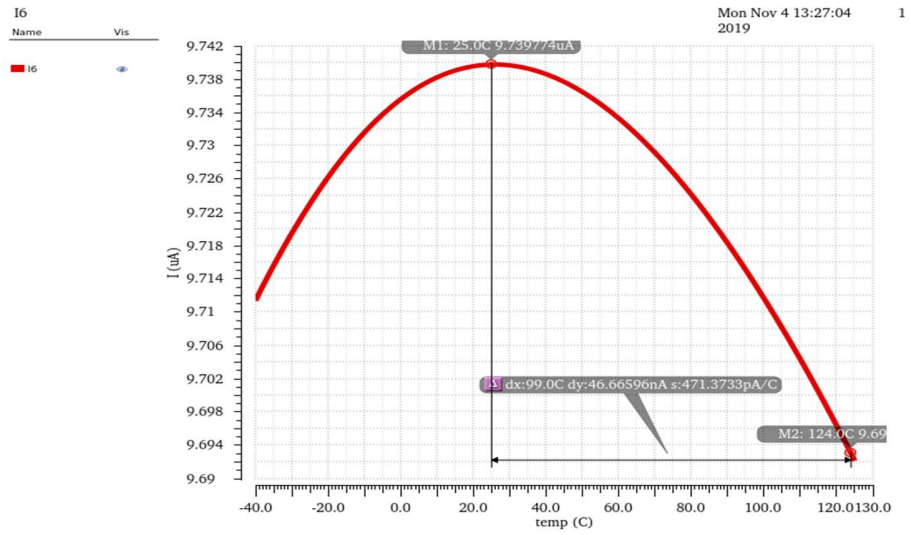

Figure 2.5. Temperature Constant Current Generated by V-to-I Converter

By sizing two source followers properly, we can achieve a relatively temperature-constant current I_3 which changes less than 0.5% over temperature change from -40°C to 125°C (Figure 2.5). The current I_3 can be calculated as

$$I_3 = \frac{V_{ref} + V_{SG,p} - V_{GS,n}}{R_6}. \tag{18}$$

2.2.3 Gm-Cell Based Voltage Summer

As mentioned in Liu's structure, a differential amplifier OP4 is used for summing the difference between V_{BE3} and V_{BE2} with the output voltage Vo from the Kujik core. Therefore, if a structure can accomplish the same goal with a simpler structure, it will be appreciated here.

The proposed Gm-cell based voltage summer prototype is a simpler replacement of difference amplifier OP4 plus R_3 and R_4 as previously shown in Figure 2.1. The circuit is provided in Figure 2.6. V_{BE2} and V_{BE3} are connected to the gates of input differential pairs in the first stage, and V_O is sent to the gate of the input pair in the second stage. Compared to Figure 2.1, this connection prevents currents flowing from V_O into Q_2 or Q_3. Therefore, two buffers OP2 and OP3 can be removed. R_S is a resistor connecting between source sides of M7a and M7b. At room temperature, V_{BE2} is set to be equal to V_{BE3} so that there's no current flowing through Rs, so the first stage is in balance, and thus no current flowing out of stage one to stage two. Stage two is also in balance, and V_{REF} tracks Vo. When the temperature rises, V_{BE2} becomes larger than V_{BE3} since diode Q_2 has a PTAT collector current and Q_3 has a temperature constant current. When there's a voltage difference between V_{BE2} and V_{BE3}, a small current is generated as:

$$i_S = \frac{V_{BE2} - V_{BE3}}{R_S}. \tag{19}$$

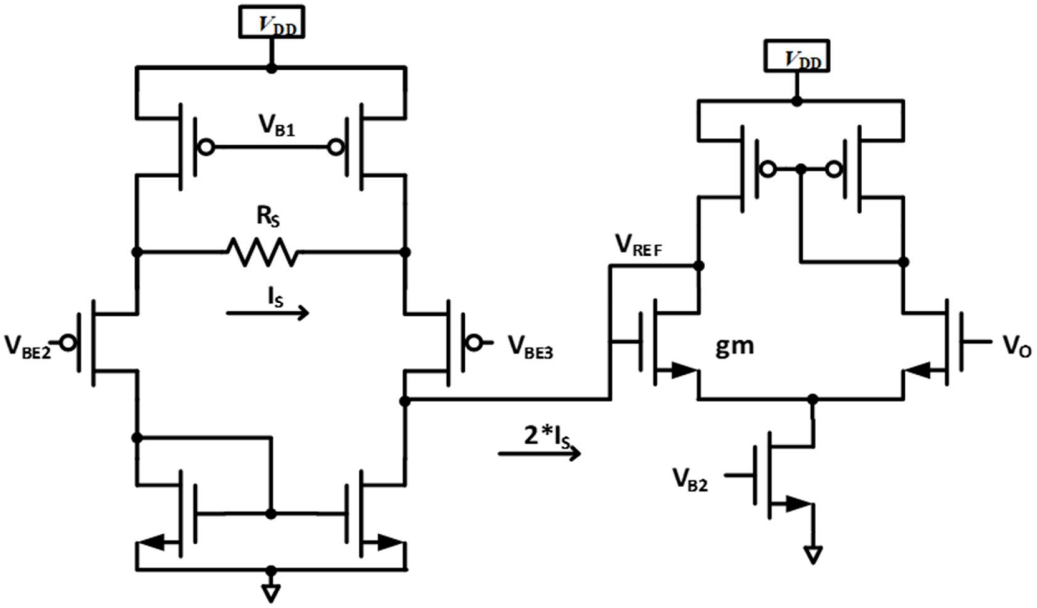

Figure 2.6. Gm-cell Based Voltage Summer Prototype

Since the small current is small enough to be analyzed by using small signal analysis, the reference voltage V_{REF} can be calculated as:

$$V_{REF} = V_O + \frac{2}{g_m R_S}(V_{BE2} - V_{BE3}). \tag{20}$$

A circuit designed like this has to have a good current matching, so cascode pairs need to be added to the current source in the first stage and current mirrors in both stages. The input pair in both stages may also need to be cascaded to improve the consistency of voltage to current converting, but limited by the voltage headroom.

Figure 2.7 shows an improved structure of the voltage summer prototype. Cascode pairs are added to the current sources and current mirrors to improve current matching. Input pairs M7a, M7b, and M13a, M13b are also cascoded to decrease channel length modulation effect. Input pair M13a and M13b are changed to PMOS to make bias easier and more consistent. Vo is

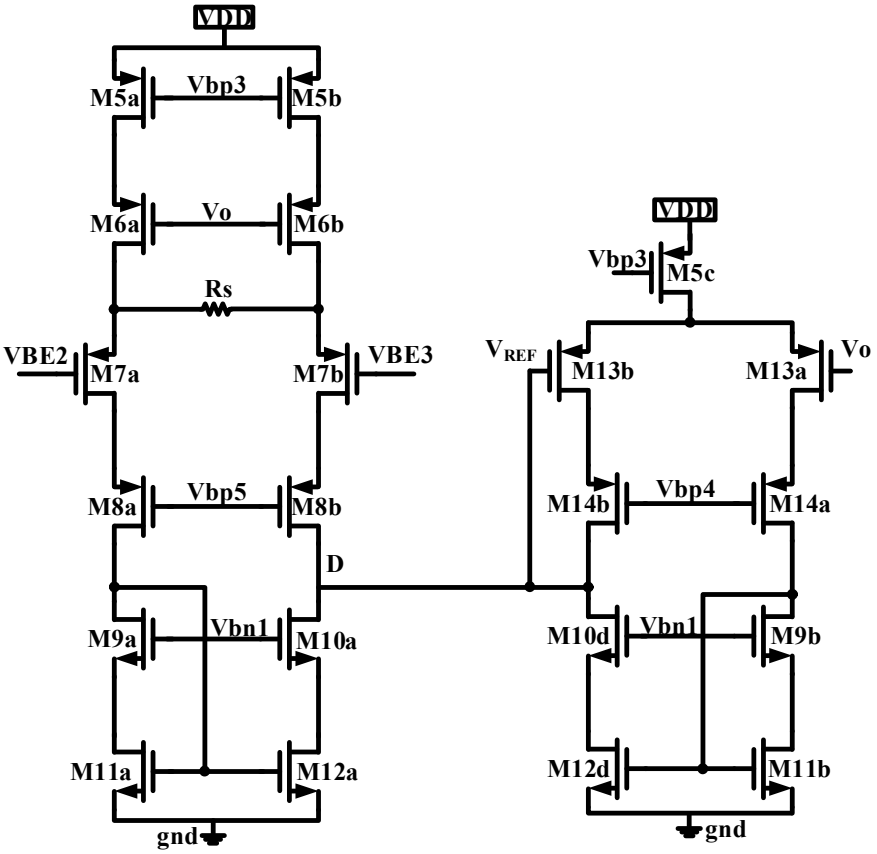

Figure 2.7. Improved Voltage Summer

used to bias M6a and M6b to increase current matching. However, directly connecting V_{REF} to node D can cause trouble. The voltages V_{REF} and V_{BE2} limit the V_{DS} headroom of transistor M7b so that M8b and input transistor M7b can go into the triode region at high temperature. Therefore, this structure needs to be further improved.

Figure 2.8 shows the final version of the voltage summer. A current subtractor is added in Figure 2.8 to "release" the voltage constraint at node D. To make calculation simple, the mirror ratio of M9 to M10 and M11 to M12 are chosen as 2:1. The principle of the voltage to current to the voltage converting remains the same as the prototype, but the input pair has been inversed. It is because we want the small current flowing into V_{REF} at high temperature, and the direction of

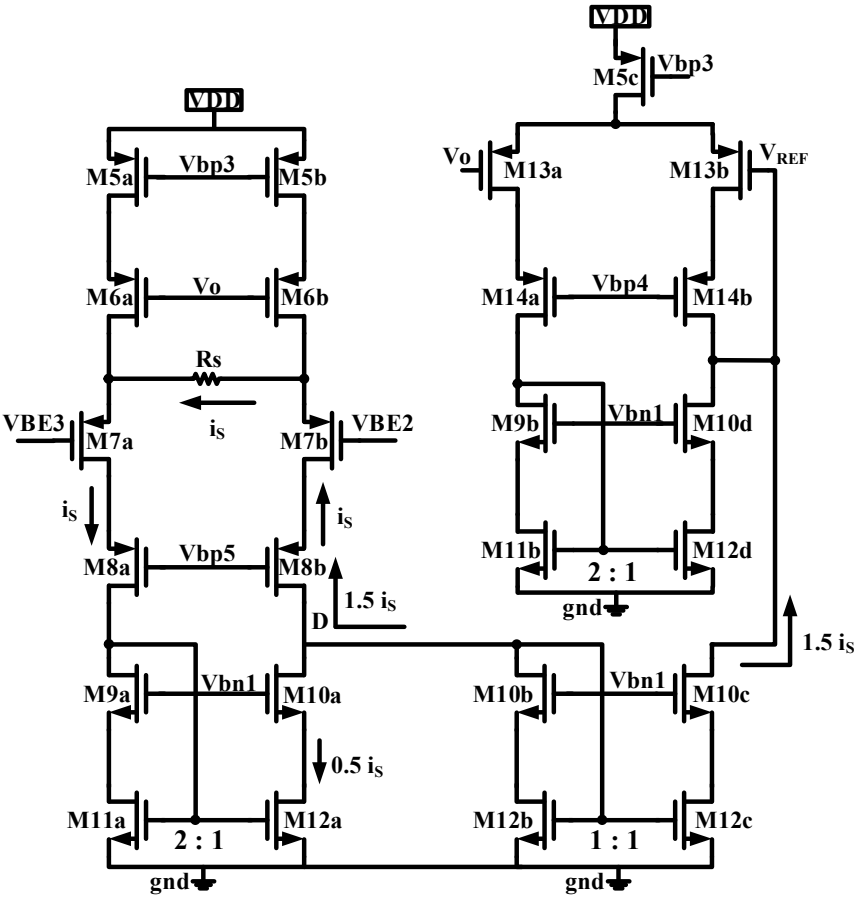

Figure 2.8. Final Version of Voltage Summer

the small current flowing at two sides of the current subtractor to be in symmetry. Therefore, there should be a small current flowing up at the left side of the current subtractor at high temperature, which means the small current flows from right to left through resistor R_S and, thus, V_{BE2} should be at the right side and V_{BE3} at left side.

For the quantitative analysis shown in Figure 2.8, since there is a small current flowing through R_S from the right side to the left side, M7b experiences a small current decreasing and M7a experiences a small current increase. The increased i_S from M7a is mirrored to M12a as a 2:1 ratio, so the overall small current flows into node D is $1.5i_S$. Symmetrically, the small current flows into M14b and M13b are $1.5i_S$ as well since the same ratio size of M12b and M12c. This

small current is regenerated as a small voltage added on V_O to achieve V_{REF}, which realizes the summing functionality here. The relationship between V_{REF} and V_O is derived below:

$$V_{REF} = V_O + \frac{1.5}{g_{m13b} R_S}(V_{BE2} - V_{BE3}) \tag{21}$$

As mentioned previously, the working performance of the voltage summer relies on good matching. Therefore, current source M5a, M5b, and M5c should precisely follow the relationship $I_{5a}=I_{5b}=1/2*I_{5c}$. Cascode transistors M6, M8, M9, M10, and M14 as shown in Figure 2.7 are also applied here to increase circuit matching. The same bias voltage V_O is applied to M6 and M14 to guarantee the V_{DS} matching of tail current sources on both stages.

Even though we came up with some techniques to reduce the systemic mismatches, there are still some mismatches caused by process variations that degrade the circuit performance. Before doing any circuit optimization to further reduce the mismatch errors, we first need to know where those mismatches are from. Therefore, a detailed mismatch analysis is presented in Section 3.1 and 3.2, and the circuit optimization will be introduced in Section 3.4.

CHAPTER 3. MISMATCH ANALYSIS AND CIRCUIT OPTIMIZAION

3.1 Mismatch Theory Review and Current Mismatch

Mismatch is a differential performance of two or more devices caused by improper circuit design or random process variation. In the design level, current mirror pairs with an incorrect ratio size or without a cascode pair to reduce channel length modulation effect will all cause a systematic error. Mismatches caused by a systematic error can be significantly reduced by using a better circuit design or applying additional mismatch-improved techniques. However, the mismatch normally appearing in our circuit is primarily caused by random process variation. In the modern process, unequal doping concentration between two transistors may cause a mobility difference and, thus, cause the current mismatch. Layouts without dummies or mismatch-reduced techniques, such as a common centroid, become easier to suffer from mismatches on transistor width and length due to process variation, and it will also lead to current mismatch eventually. However, for moderately-sized devices, the lithography errors are so small that width and length mismatches can be negligible. These kinds of mismatches caused by process variations can be reduced simply by circuit optimization but not erased. Some detailed mismatch analysis is shown as follows.

According to square-law model, the drain current in saturation region can be written as

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS}-V_{TH})^2 = \frac{1}{2}\beta(V_{GS}-V_{TH})^2 . \tag{22}$$

In Eq. (21), we can easily distinguish that current mismatches are mainly caused by two factors: the carrier mobility mismatch μ, which can also be represented as β since mobility mismatch is the dominant component; and the threshold voltage mismatch V_{TH}. Considering the mismatches of β and V_{TH} are regularly quite small when compared to themselves, we can apply the partial derivative of drain current to different mismatch sources to determine the extent the mismatches

are contributed by each source to the drain current. Then we can apply the superposition concept to add them together and get the total mismatches to the drain current. By following the steps, we first take the partial derivative of I_D to V_{TH}, which can be derived as

$$\left|\frac{\Delta I_D}{\Delta V_{TH}}\right| \approx \left|\frac{\partial I_D}{\partial V_{TH}}\right| = \left|-\beta(V_{GS}-V_{TH})\right| = g_m . \tag{23}$$

Then we take this absolute value because we care more about how much mismatch is caused, not whether the mismatch increased or decreased. Getting a positive number is easier for further calculation. By using the same method, we can also find the partial derivative of I_D to β, which is

$$\frac{\Delta I_D}{\Delta \beta} \approx \frac{\partial I_D}{\partial \beta} = \frac{1}{2}(V_{GS}-V_{TH}) = \frac{I_D}{\beta} . \tag{24}$$

Next, by applying the superposition, we can get the total current mismatch caused by both β and V_{TH} is

$$\frac{\Delta I_D}{I_D} = \frac{g_m}{I_D}\cdot \Delta V_{TH} + \frac{\Delta \beta}{\beta} . \tag{25}$$

From Eq. (25), we realize that if we want to decrease the current mismatch, which is normally the case in the current mirror, we should decrease the g_m/I_D ratio. Since g_m is the partial derivative of I_D to V_{GS}, the g_m/I_D ratio can also be expressed as

$$\frac{g_m}{I_D} = \frac{2}{V_{GS}-V_{TH}} = \frac{2}{V_{on}} . \tag{26}$$

Therefore, increasing the overdrive voltage of the current mirror pair or decreasing its g_m by applying source degenerated resistors are good choices to reduce drain current mismatch.

3.2 Input-Referred Offset Voltage

DC offset, also called input-referred offset voltage, is a DC voltage shift that appears at the input terminal when the output voltage is set to zero. Normally, the input-referred offset is caused by circuit mismatch and the weak negative feedback loop gain. The cause due to

insufficient loop gain will be discussed later and is not considered in this section, where the circuit mismatch is considered.

A circuit mismatch can happen anywhere in a circuit; for instance, in the current mirror pair. The drain current mismatch was discussed in the previous section. However, the effect caused by current mismatch can refer to a voltage mismatch that appears at the input terminal and, thus, becomes the input-referred offset voltage. Since the offset is small enough to be considered as a small signal, we can use small signal analysis to deal with the offset voltage as well. For small signals, the current to voltage conversion is divided by g_m. Thus, a new equation based on input-referred offset voltage can be derived from Eq. (26) as

$$V_{OS} = \Delta V_{GS} = \frac{\Delta I_D}{g_m} = \Delta V_{TH} + \frac{I_D}{g_m}\left(\frac{\Delta\beta}{\beta}\right). \tag{27}$$

When compared to Eq. (26), there is a contradictory result of the g_m and I_D relationship in Eq. (27). To reduce input-referred offset, we should decrease the I_D/g_m ration (i.e. increase the g_m/I_D ratio). It is known that, when the drain current of a transistor is insufficient, the gate-source voltage V_{GS} will decrease. When V_{GS} drops to a value around threshold voltage V_{TH}, or slightly smaller than V_{TH}, the inversion layer underneath the gate oxide will be very weak, and the transistor will enter the weak inversion region, also called the sub-threshold region. In this region, due to the very limited drain current, the g_m efficiency will be the greatest, or several times larger than in strong inversion. Thus, the g_m/I_D ratio will be relatively large if biased in the sub-threshold region. Therefore, we could bias the input pair in the sub-threshold region to reduce the input-referred offset by increasing the g_m/I_D ratio.

3.3 Influence of Offset Voltage in Bandgap Reference

3.3.1 Influence of Offset Voltage in Previous Work

As mentioned in previous work (see Section 2.1), because of the number of op amp use, the offset voltage of each op amp will contribute and propagate to the reference voltage V_{REF}. The detailed calculation for V_{REF} with offset voltages can be written as

$$\begin{aligned} V_O &= V_{BE2} + \frac{R_2}{R_1} \cdot \frac{kT}{q} \ln(N) - (1 + \frac{R2}{R1}) V_{OS1} \\ V_{REF} &= V_O + \frac{R_4}{R_3} \Delta V_{BE2,3} - (1 + \frac{R_4}{R_3}) \cdot V_{OS4} - \frac{R4}{R3} (V_{OS2} - V_{OS3}) \end{aligned} \tag{28}$$

where V_{OS5} is neglected because OP5 regulated V_{REF}; thus, it has little effect on offset propagation. In previous work, a high precision op ADA4528 spice model was applied to all op amps; therefore, the offset problem was not considered. However, the proposed bandgap reference is an SoC, which means everything covered in the circuit needs to be built; thus, the offset problem should be considered and optimized.

3.3.2 Influence of Offset Voltage in Proposed Bandgap Reference

Figure 3.1 shows the full schematic of the proposed bandgap reference. As illustrated in the structure, the offset voltages that will affect the output reference voltage are basically two offsets. One is the offset of the op amp in Kuijik core, which can be noted as V_{OS1}. The other is the voltage difference between V_{REF} and V_O at the second stage of voltage summer when the summer's input V_{BE2} and V_{BE3} are tied together, which can be written as V_{OS2}. The V_{REF} expression with offset contributing to it can be calculated as

$$V_{REF} = V_{BE2} + \frac{R_2}{R_1} \Delta V_{BE2,1} + \frac{1.5}{g_{m13b} R_S} \Delta V_{BE2,3} + (1 + \frac{R_2}{R_1}) V_{OS1} + V_{OS2} . \tag{29}$$

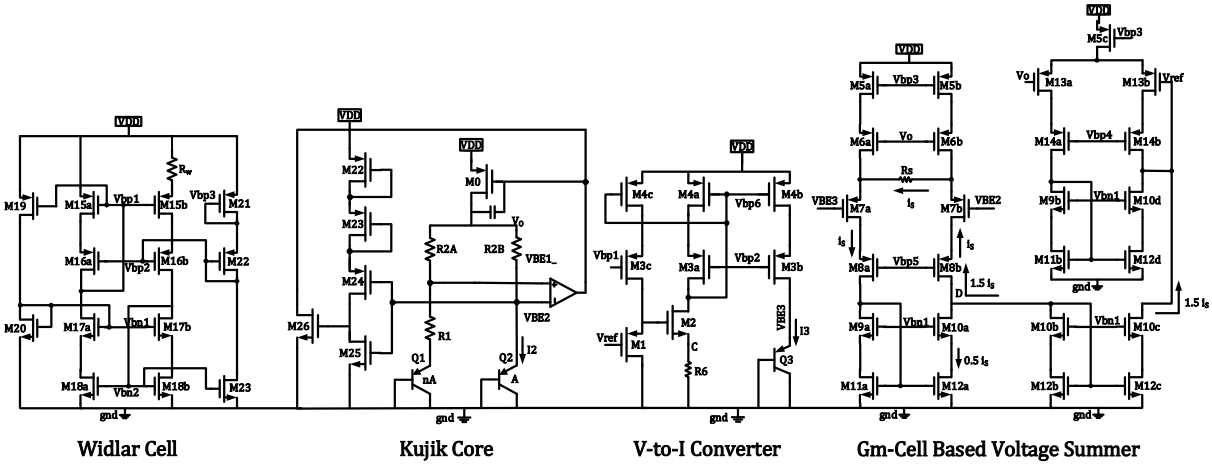

Figure 3.1. Schematic of Proposed Bandgap Reference

In Eq. (29), we can see V_{OS1} has been amplified by the resistor ratio of R_2 and R_1 and becomes around ten times larger when it propagates to V_{REF}, which is not acceptable and has to be trimmed out. V_{OS2} is small since it hasn't been amplified by a resistor ratio. However, trimming V_{OS2} out is hard because it has g_m and gain dependency. Therefore, V_{OS2} will not be trimmed in the proposed trimming method but will be optimized.

3.4 Offset Optimization

Figure 3.2 shows 100 Monte Claro runs for V_{OS1} in Kujik core. 3σ is chosen for process variation and temperature is swept from -40°C to 125°C. From the figure, we can realize the process variation is quite large in UMC65 so that the offset spread from -4mV to 4mV, which is too large to be trimmed out. Therefore, before trimming, the circuit needs to be further optimized to reduce V_{OS1}. As discussed in Section 3.2, the offset is mainly caused by limited loop gain and circuit mismatch. Figure 3.3 shows the loop gain of the op amp in Kujik core degrading over temperature. From the figure, it's obvious that the loop gain only decreases 5dB over 125 temperature, and still have sufficient value at 125°C. Therefore, the conclusion can be drawn that V_{OS1} does result from limited loop gain.

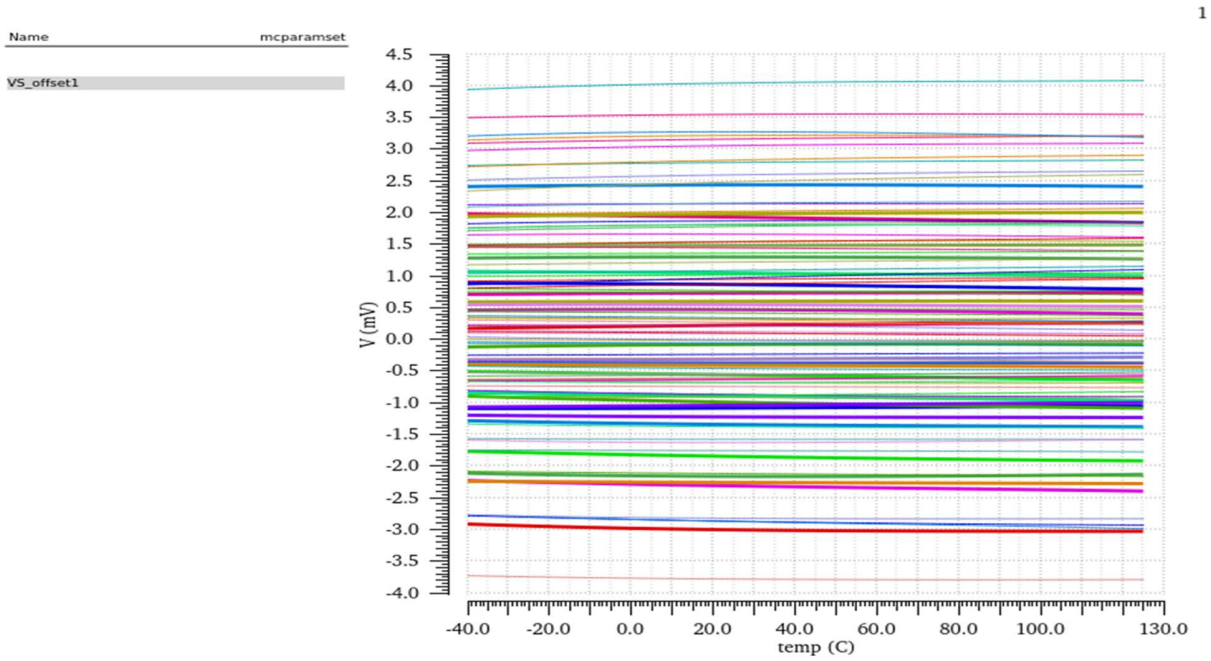

Figure 3.2. One Hundred Monte Carlo Runs of V_{OS1}

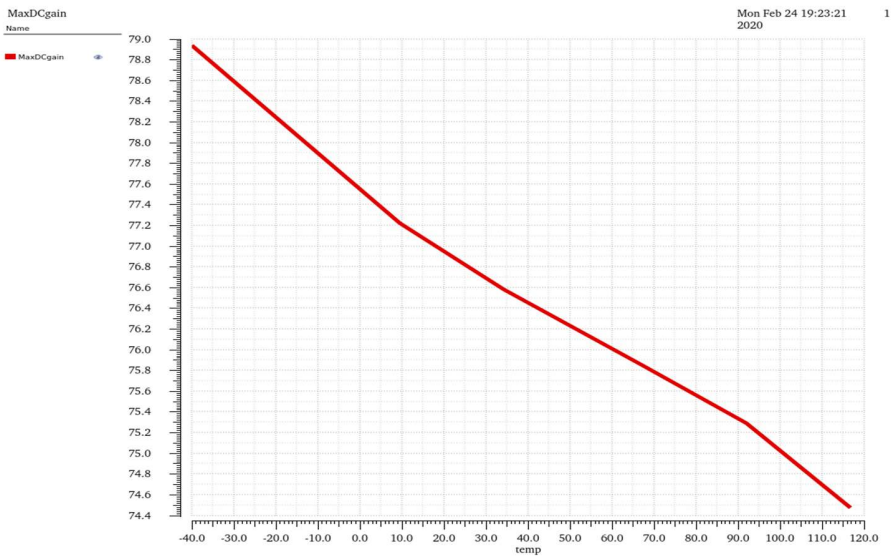

Figure 3.3. Loop Gain Changing over Temperature for Op Amp in Kujik Core

The offset is primarily caused by circuit mismatch. According to the mismatch theory review in Section 3.1, the current mismatch at the current mirror can be reduced by applying source degenerated resistor, and the input-referred offset can be reduced by biasing the input pair into the sub-threshold region. Details of the op amp are shown in Figure 3.4. The source degenerated resistor is not applied to current source pair M29a and M29b because they have a fixed bias and the current mismatch is relatively small compared to current mirror pair M32a and M32b. Adding source degenerated resistors will have very little improvement.

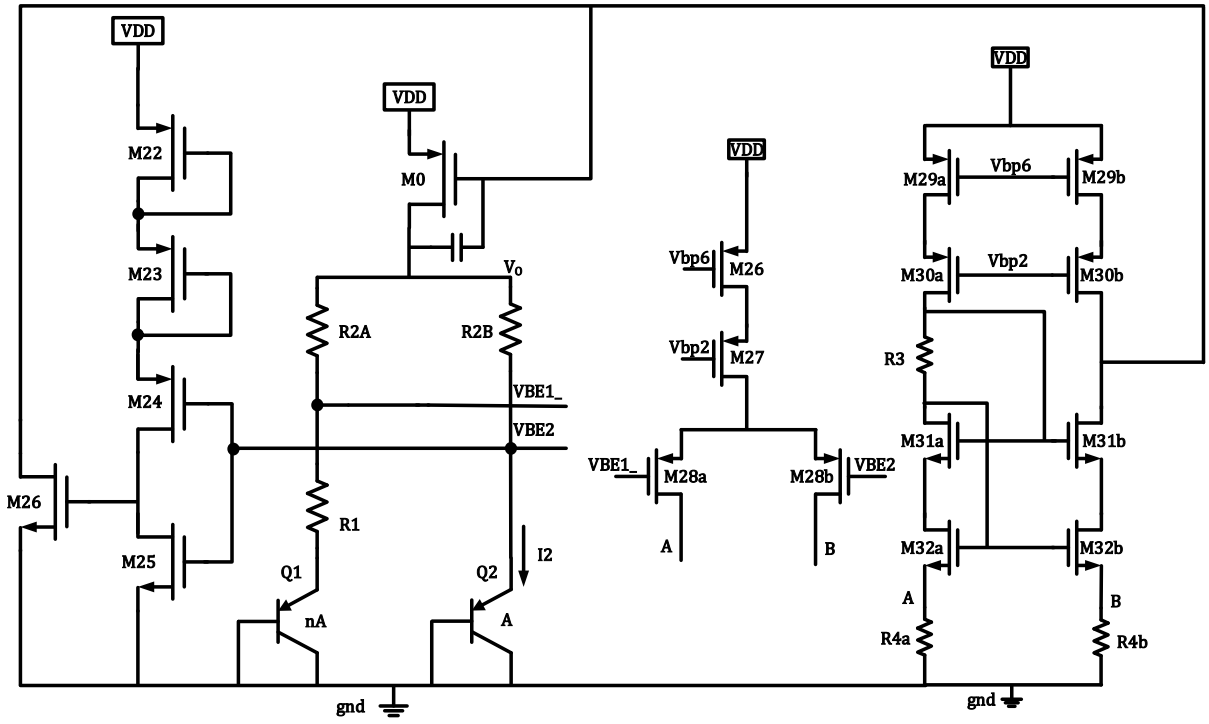

Figure 3.4. Optimized Op Amp in Kujik Core

After optimizing the op amp, the same 100 Monte Carlo runs are selected, and the result is shown in Figure 3.5. The offset of the op amp in the Kujik core has been significantly reduced. Offsets in three-sigma variation can be controlled in the range of -1.5mV to 2mV, except three failure runs. Offsets in one sigma variation can be controlled in around -0.5mV to 0.5mV, which is a lot better than before.

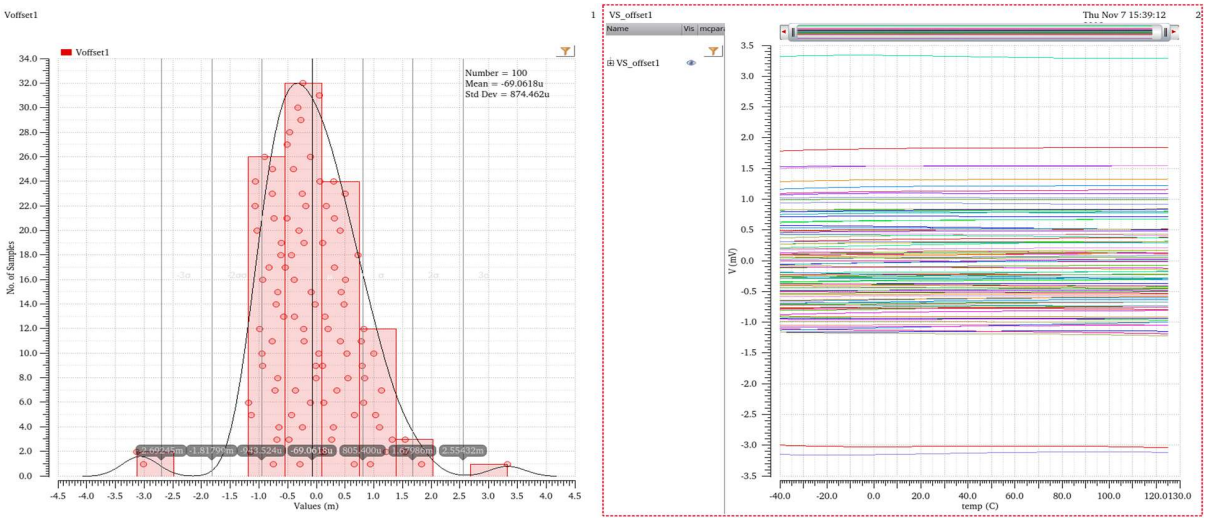

Figure 3.5. One Hundred Monte Carlo Runs of V_{OS1} After Optimization

CHAPTER 4. TRIMMING, SIMULATION AND LIMITATION

4.1 Single Temperature Trimming

A single temperature trimming was implemented in the proposed solution. Comparing to a two-temperature trimming, trimming only at room temperature has limited capability to trim against all error sources which include: BJT process variations, resistor mismatch, the offset of the op-amp in Kujik core (V_{OS1}), and the offset between V_{REF} and Vo (V_{OS2}). The effects of V_{OS1} and V_{OS2} on PTAT errors in V_{BE} were both trimmed in the proposed method. The propagation of V_{OS1} and V_{OS2} to V_{REF} is shown in Eq. (29), The V_{OS1} drift via temperature will still propagate to the reference output but it is optimized during design. The correlation between the voltage summer's gain and V_{OS2} makes the trimming of both parameters difficult. Therefore, only the summer's gain is trimmed. The trimming steps are organized as follows:

1. To trim out V_{OS1}, the difference between $V_{BE1\_}$ and V_{BE2} is measured, and a binary-weighted trimming on input pair's widths with 6-bit resolution, which is introduced in [11], is applied to trim V_{OS1} to nearly 0 V at room temperature.
2. Considering the existence of V_{OS2}, the trimming target for V_{REF} is set to be V_{GO1} + V_{OS2} instead of V_{GO1}. To measure V_{OS2}, the voltage summer input pair's gates are first shortened to V_{BE2}. Then we measure the difference between V_{REF} and Vo to get V_{OS2}.
3. To calibrate the gain, R_6 is doubled so that Q_3's current becomes half and two inputs of the summer have an observable difference. Then the difference V_{diff} between V_O and V_{REF} is measured and the gain can be calculated as (V_{diff} – V_{OS2})/ $\Delta V_{BE2,3}$. Its value is trimmed to $(\eta - 1 - b\frac{q}{k})$ by adjusting R_S at room temperature. After gain trimming, R_6 is tuned until $V_{BE3}(T_r) = V_{BE2}(T_r)$, so that $\Delta V_{BE2,3} = -\frac{kT}{q}\ln(\frac{T}{T_r})$ is 0 V at T_r and does not affect PTAT trimming.

4. The final step is to tune R_2 until $V_{REF} = V_{GO1} + V_{OS2}$.

In Liu's trimming method, resistor ratios are used to keep the coefficient accurate, as shown in Eq. (16). In the proposed structure, the coefficient for high order term is based on $1/g_mRs$, not a resistor ratio, which is shown in Eq. (21). To make it accurate and less affected by variations, a P-type Wilder cell is used to bias the voltage here so that the resistor in the Widlar cell and Rs can become a resistor ratio. More details are provided in Section 4.3.2, Eq. (31).

4.2 Simulation Result

4.2.1 Monte Carlo Runs for Reference Voltage

The proposed bandgap structure has been verified in the UMC65 process. A folded cascode op-amp with high gain and low offset was built for the Kujik core. One hundred Monte Carlo runs were simulated. As shown in Figure 4.1, the temperature coefficient of the reference can vary from several ppm/°C to tens of ppm/°C due to process variations and mismatch. Five runs are provided to verify the trimming method presented before. As provided in Figure 4.2, after single room temperature trimming, all 5 runs had a temperature coefficient of less than 10 ppm/°C in the range from -40 °C to 125 °C. The temperature coefficient of each run is marked in the figure. The proposed trimming method has limitations when dealing with op-amp offsets' temperature drift. To further reduce the temperature drift, a better technique needs to be applied to minimize the temperature drift of V_{OS1}.

4.2.2 Power Supply Rejection Ratio

Power Supply Rejection Ratio (PSRR) is a term used to describe the capability of the circuit to suppress any power supply variation to its output signal. In the proposed bandgap reference, a 10mV AC small signal was applied at voltage supply. The PSRR of the proposed bandgap reference is plotted in Figure 4.3. Considering bandgap references are commonly used in

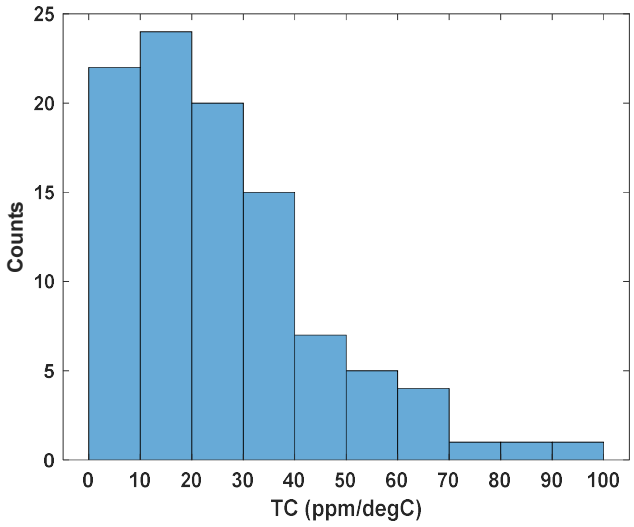

Figure 4.1. Distribution of One Hundred Monte Carlo Runs before Trimming

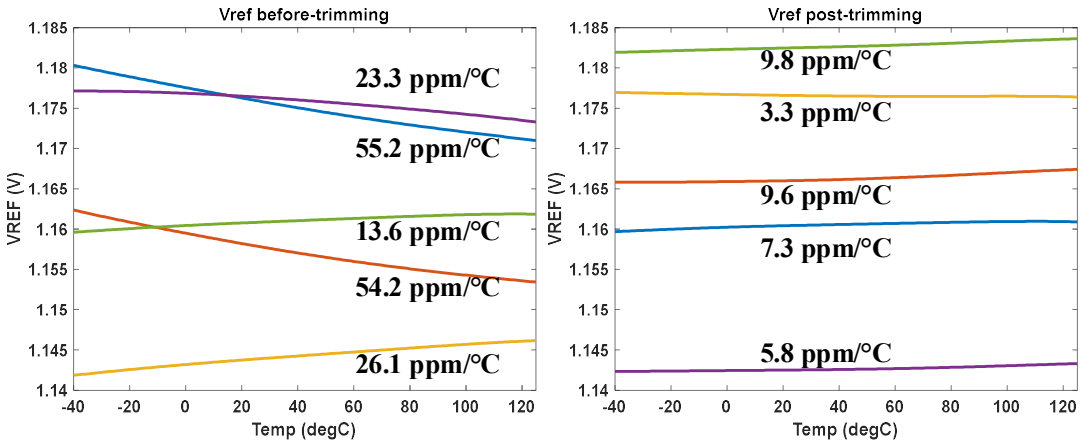

Figure 4.2. Five Picked Monte Carlo Runs (a) Before Trimming (b) After Trimming

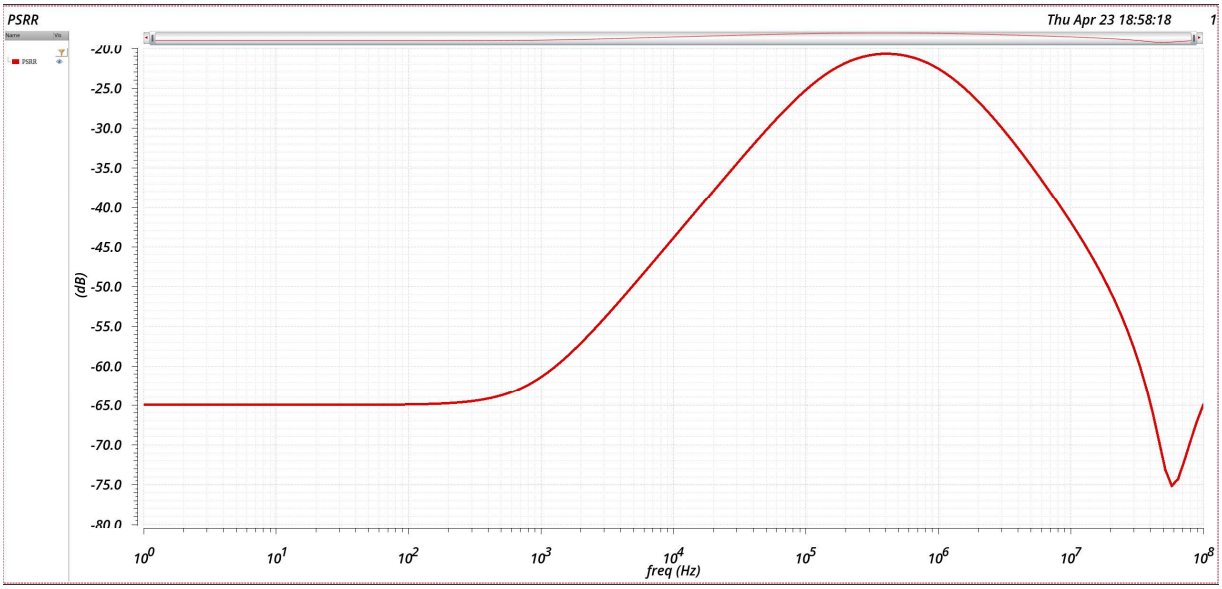

Figure 4.3. PSRR for Proposed Bandgap Reference

low-speed cases, the 65dB of PSRR are sufficient to suppress the power supply variation in low-speed applications

4.3 Limitations Caused by Temperature Drift

4.3.1 Temperature Drift of V_{OS1}

In Section 3.4, we optimized the offset voltage V_{OS1} in Kujik core and significantly reduced the offset at room temperature. However, as temperature changes, the offset voltage also changes as indicated in Figure 4.4. V_{OS1} is run in a typical corner, where it has an approximately 7uV change over 165°C temperature range. What makes the offset drift hard to be trimmed out is it has a Non-PTAT property. For a single temperature trimming, it's impossible to trim out both DC offset and its drift.

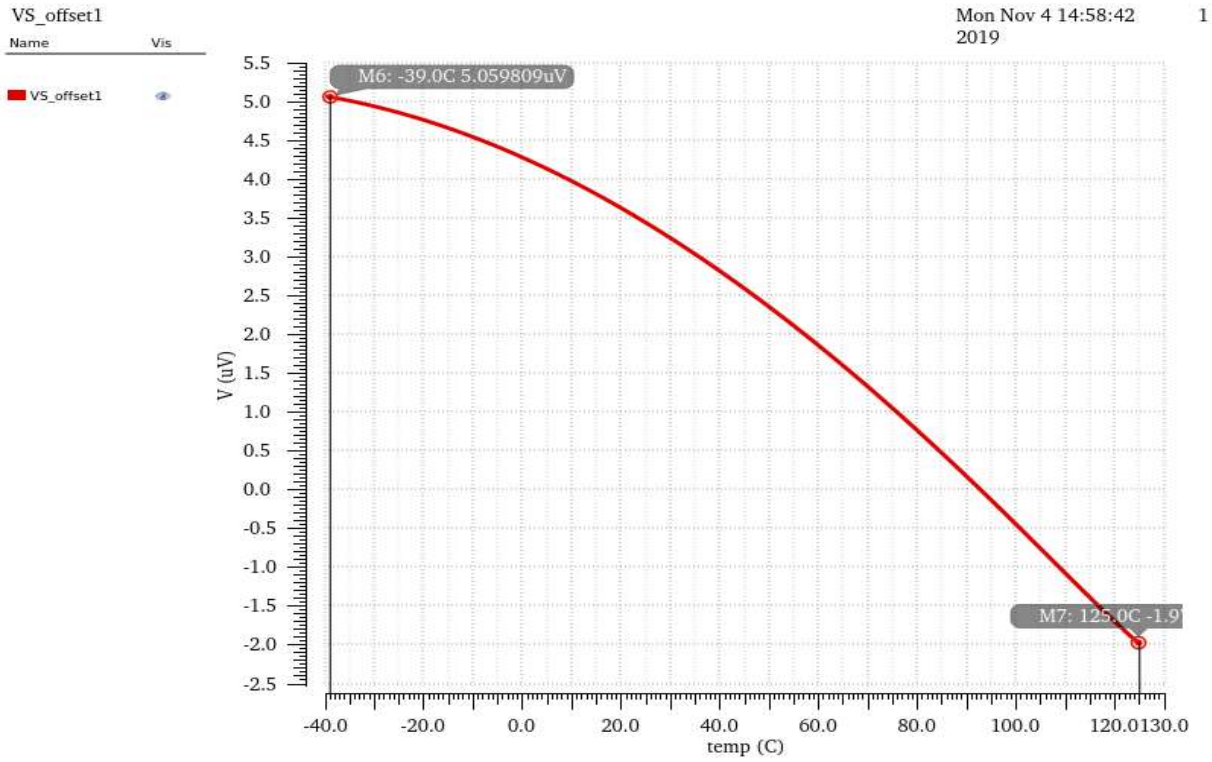

Figure 4.4. V_{OS1} Drift over Temperature

4.3.2 Temperature Drift of V_{OS2}

The temperature drift of the summer's gain can add a high order temperature dependent error to the reference output, but it has been to be small in design. In the proposed structure, the voltage summer was biased by a P-type Widlar current source. The bias current from the Widlar cell can be written as:

$$I_{OUT} = \frac{2}{\mu_p C_{ox} (W/L)_p} \cdot \frac{1}{R_W{}^2} (1 - \frac{1}{\sqrt{K}})^2 \tag{30}$$

where R_w is the resistor in the Widlar circuit and K is the size ratio, which is 4 in this design. The denominator of the gain can then be rewritten as:

$$g_{m13b} R_S = \frac{R_S}{R_W} \cdot \sqrt{\frac{\mu_{13b}}{\mu_p}} \cdot \sqrt{\frac{(W/L)_{13b}}{(W/L)_p} \cdot r} \tag{31}$$

where r is the current mirror ratio from Widlar current I_{OUT} to bias current I_{13b} of transistor M13b. In Eq. (31) the temperature dependency of parameters R_S and μ_{13b} in voltage summer have been canceled out by relevant parameters R_W and μ_p in the Widlar cell. The device variations may result in different temperature coefficients on these parameters, which can lead to a temperature drift on the gain. However, the drift is small since it's resulted from the mismatch between devices.

Figure 4.5 shows the V_{OS1} and V_{REF} of a picked Monte Carlo sample after trimming. The temperature drift of V_{OS1} propagates to the final output so that the drift of reference voltage looks the same as the offset drift. The difference between V_{REF} drift and V_{OS1} drift is the resistor ratio of R_2/R_1 in this case. This illustrates the offset drift is mostly from V_{OS1}, and the drift of V_{OS2} is small.

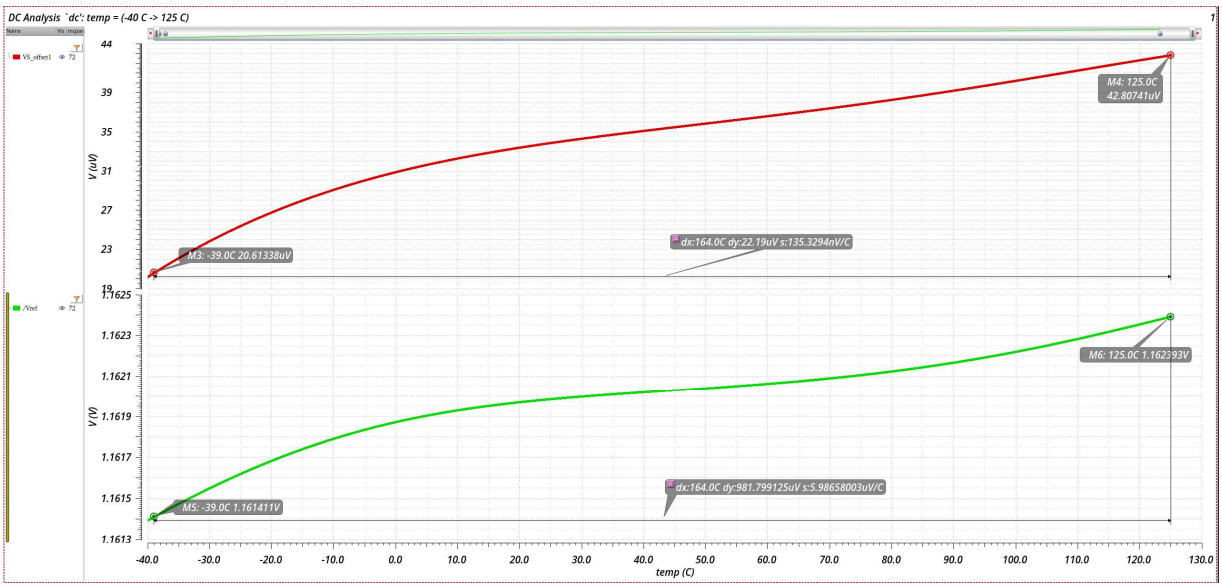

Figure 4.5. V_{OS1} Propagation

CHAPTER 5. DISCUSSION

As stated in Section 4.3, the proposed single-temperature trimming method cannot trim the DC offset of the reference voltage and the temperature drift of V_{OS1}. To remove the DC error of V_{OS2}, a user-side voltage buffer is needed to regulate the reference voltage to the wanted value. The research work that has been completed thus far was accepted for publication in May 2020 [15]. A goal for future study might be to consider how to remove the drift of V_{OS1}. Since achieving a simpler structure was the goal of the proposed structure, some offset removal techniques such as chopping and auto zeroing will significantly increase the complexity of the circuit; therefore, they were not considered in this research. Bolatkale et al. [16] supplied a good direction of drift cancellation. If the tendency of the drift can be predicted by measuring several parameters at room temperature, then trimming out both DC offset and offset drift may be achieved in a single-temperature trimming. Detailed noise analysis was not supplied in this thesis research, but was discussed briefly. Since the bandgap reference normally operates in low-speed applications, the flicker noise dominants. To decrease flicker noise in both the Kujik core and voltage summer, larger capacitors were added at the output nodes to filter out the noise. A good PSRR will also suppress the noise from the supply source at low frequencies.

CHAPTER 6. CONCLUSION

This thesis research proposed a simple bandgap reference which can extract V_{GO1}. Prior bandgap background knowledge was introduced in Chapter 1, and two specific bandgap references were introduced in Chapter 2. In the first half of Chapter 2, previous work was presented as well as motivation for improvement. The remaining half of Chapter 2 introduced the proposed bandgap reference and its essential block – a simple V-to-I converter – which can generate a constant current for the third diode whose V_{BE} is used for curvature correction is introduced. A G_m-cell based voltage summer was then proposed to save power and area compared to the previous structure. The offset issue was discussed in Chapter 3 as well as the proposed solution to it. In Chapter 4, a single temperature trimming method was proposed which can achieve less than 10ppm/°C temperature drift at the reference output. Table 6.1 provides a summary of transistor sizes, and Table 6.2 a reference comparison of different bandgaps.

Table 6.1. Transistor Size Summary

Number	Size(W/L) um	Number	Size(W/L) um
M_0	5/4	M_{14a}, M_{14b}	(5/1)*2
M_1	4/1	M_{15a}, M_{15b}	1.5/1
M_2	5/1.5	M_{16a}, M_{16b}	6/0.5
M_{3a}, M_{3b}, M_{3c}	(1.5/0.5)*4	M_{17a}, M_{17b}	2/0.5
M_{4a}, M_{4b}, M_{4c}	(2/4)*4	M_{18a}, M_{18b}	(4/8)*2
M_{5a}, M_{5b}, M_{5c}	5/1.5	M_{19}	1.5/1
M_{6a}, M_{6b}	2/2	M_{20}	1/4
M_{7a}, M_{7b}	(10/1)*2	M_{21}	(5/1.5)*2
M_{8a}, M_{8b}	10/1	M_{22}	(4/1.5)*2
M_{9a}, M_{9b}	(2/1)*2	M_{23}	(4/8)*2
M_{10a}, M_{10b}, M_{10c}, M_{10d}	2/1	M_{24}	6/0.24
M_{11a}, M_{11b}	(2/2)*2	M_{25}	3/0.24
M_{12a}, M_{12b}, M_{12c}, M_{12d}	2/1	M_{26}	0.45/0.3
M_{13a}, M_{13b}	0.5/2		

Table 6.2. Comparison Table of Different Bandgaps

Reference	Proposed Structure	[7]	[8]	[12]	[13]	[14]
Year	2020	2019	2011	2007	2005	2002
Publication	ISCAS	ISCAS	JSSC	JSSC	ISCAS	ISSCC
Bandgap Voltage (V)	1.21	1.21	1.0875	0.858	1.15	1.266
Supply (V)	2.5	2.5	1.8	1.4	1.8-5.5	1.8
Temp range (°C)	-40-125	-40-125	-40-125	-40-125	-20-120	0-100
Power (uW)	147.5	N/A[2]	99	162.4	180-550	5940
Area (mm^2)	**0.03**[1]	N/A[2]	0.12	1.2	1.2	0.007
Best TC (ppm/°C)	**3.3**	**<1**	5	12.4	3	10
Process (um)	0.065	0.13	0.16	0.35	0.6	0.18

*** Results that are only obtained by simulation are bolded.**

1. This value is an estimated value generated by automatic generate layout since the actual layout was not built.

2. Power consumption and die area are not applicable in this design since out-of-chip op amps are used.

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