

**Modified Kuijk Bandgap Reference with  $V_{GO}$  Extraction**

by

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The student author, whose presentation of the scholarship herein was approved by the program of study committee, is solely responsible for the content of this thesis. The Graduate College will ensure this thesis is globally accessible and will not permit alterations after a degree is conferred.

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**NOMENCLATURE**

BJT	Bipolar Junction Transistor
BGR	Bandgap Reference
TC	Temperature Coefficient
PTAT	Proportional to absolute temperature
CTAT	Complementary to absolute temperature
CMOS	Complementary metal oxide semiconductor
PPM	Parts per million
Opamp	Operational amplifier

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**ABSTRACT**

This creative component presents an innovative CMOS Bandgap Reference Generator topology targeting sub-ppm temperature coefficient over a wide temperature range. The proposed circuit consists of extracting  $V_{GO}$  from the temperature characteristics of  $V_{BE}$ .  $V_{GO}$  is the bandgap voltage of the silicon that is extrapolated at 0K and is temperature independent over a wide range of temperature (-40°C to 125°C). Analytical constraints are carefully investigated which lead to the output voltage that is proportional to  $V_{GO}$  when certain mismatches and opamp offsets are accurately trimmed using two temperatures trimming. The modified circuit, less number of operational amplifiers and resistors which make the circuit less complex, reduces area and power requirements. Transistor level simulations are implemented in GlobalFoundries 130nm process and achieve temperature coefficient about 3.5ppm/°C across the industrial temperature range (-40 °C to 80 °C).

## CHAPTER 1. INTRODUCTION

### 1.1 Bandgap References

A **bandgap voltage reference** is a temperature independent voltage reference circuit which is widely used in integrated circuits. It produces a constant voltage regardless of power supply variations, temperature changes and circuit loading.

Voltage references are required in most analog and mixed-signal circuits as part of internal biases or the target of operations. The increasing demand for modern high-performance circuits, such as voltage regulators and high-resolution data converters, poses a need for high precision, low temperature coefficient (TC) voltage references.

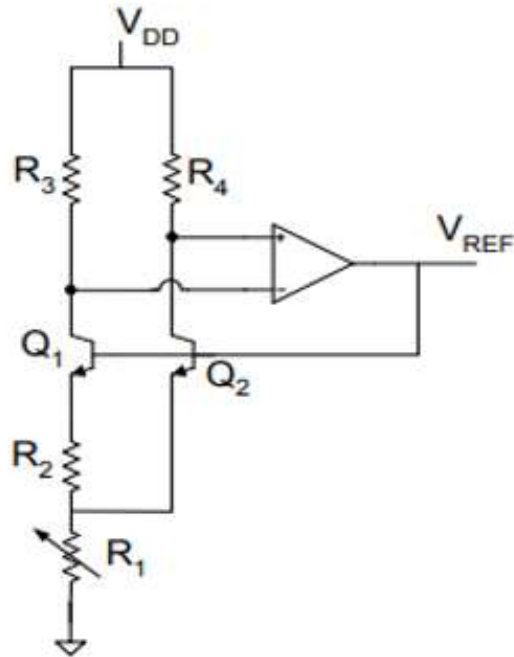
The bandgap reference,  $V_{GO}$  as the dominant component at the outputs, extrapolated at zero Kelvin is found to have a temperature independent behavior over a wide range of temperatures [1]. The standard solution has been to design circuits which can perform a linear combination of the base-emitter voltage  $V_{BE}$  which has a negative temperature coefficient and a proportional-to-absolute-temperature (PTAT) voltage. Unfortunately, the  $V_{BE}$  has a  $T \cdot \ln(T)$  dependence and this results in an around 10 ppm/°C temperature drift at the output voltage over a 150 °C range [2]. However, often trimming at two or more temperatures is required and most measured results are still in the single-digit ppm/°C range.

### 1.2 Architectures of bandgap reference circuits

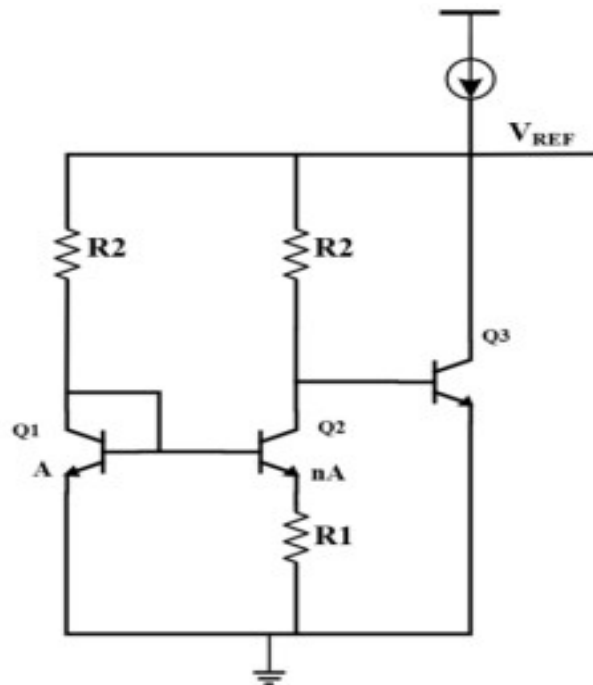
Since the mid-1970s, bandgap references circuits have been widely used in analog design. Start-up circuits are required for these references but do not affect the basic voltage-temperature characteristics under normal operation. A variety of circuits are designed, the implementation varies from one circuit to others, but the underlying concept remains the same. Figure 1 shows four different basic architectures of bandgap reference circuits which are the



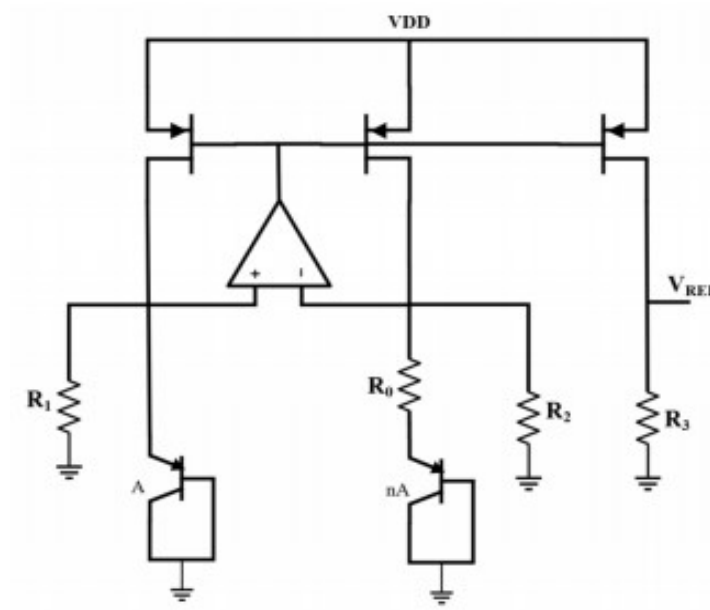
Brokaw bandgap reference circuit, Widlar bandgap circuit, Kuijk bandgap reference circuit and Banba bandgap circuit.



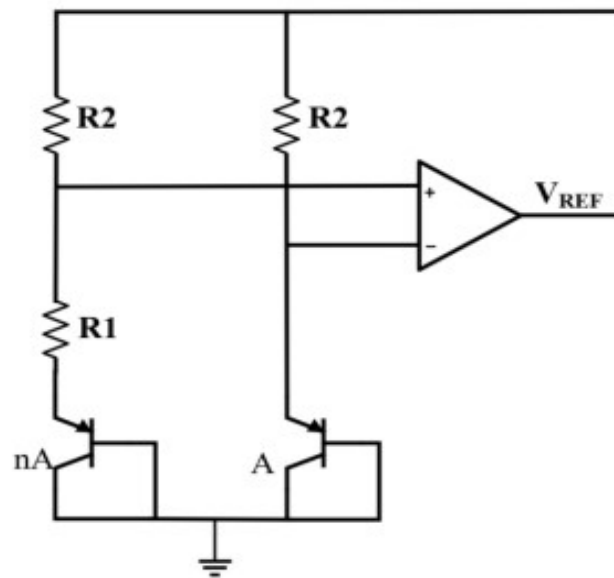
(1.1)



(1.2)



(1.3)



(1.4)

Figure 1. Architectures of bandgap reference circuits (1.1) Brokaw [3] (1.2) Widlar [4]

(1.3) Banba [5] (1.4) Kuijk [6]

## CHAPTER 2. $V_{GO}$ Extraction and $V_{BE}$ Temperature Characteristics

### 2.1 Analytical Expression of $V_{BE}$

The collector current of an NPN transistor in the forward active region or I-V relationship for a diode-connected BJT [8] can be expressed as

$$I_C = I_S \exp\left(\frac{qV_{BE}}{kT}\right) \Rightarrow V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S} \quad (1)$$

$$\text{when } I_S(T) = bT^\eta \exp\left(-\frac{qV_G(T)}{kT}\right)$$

where T is the absolute temperature,  $I_C$  the collector current,  $I_S$  the saturation current,  $V_{BE}$  the base-emitter voltage, q the electron charge, k the Boltzmann constant,  $V_G(T)$  is the bandgap voltage at temperature T, where b is a temperature-independent constant that includes emitter area  $A_e$ ,  $\eta$  is a process-dependent constant.

$$\text{At } T \quad V_{BE}(T) = \frac{kT}{q} \ln \frac{I_C(T)}{I_S(T)}$$

$$\text{At } T_r \quad V_{BE}(T_r) = \frac{kT_r}{q} \ln \frac{I_C(T_r)}{I_S(T_r)}$$

$$V_{BE}(T) - \frac{T}{T_r} V_{BE}(T_r) = \frac{kT}{q} \left( \ln \frac{I_C(T)}{I_S(T)} - \ln \frac{I_C(T_r)}{I_S(T_r)} \right)$$

$$V_{BE}(T) = \frac{T}{T_r} V_{BE}(T_r) + \frac{kT}{q} \left( \ln \frac{I_C(T)}{I_S(T)} \frac{I_S(T_r)}{I_C(T_r)} \right)$$

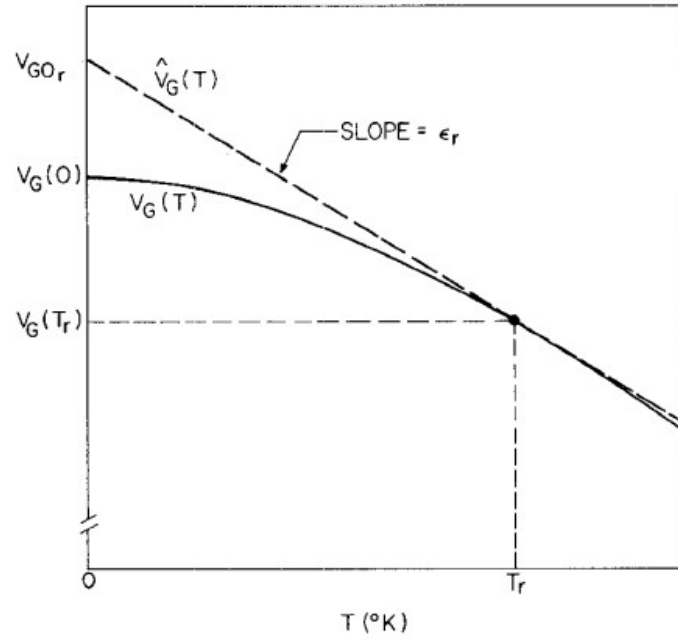


Figure 2: Bandgap voltage versus absolute temperature and its first-degree approximation [8]

Bandgap voltage,  $V_G(T)$  is assumed to have a linear temperature dependence,

$$V_G(T) = V_{GOr} + \epsilon_r (T)$$

$$V_G(T_r) = V_{GOr} + \epsilon_r (T_r)$$

$$I_c(T) = I_s(T) e^{q(V_{BE}(T) - V_G(T))/kT}$$

$$I_c(T_r) = I_s(T_r) e^{q(V_{BE}(T_r) - V_G(T_r))/kT_r}$$

$$\frac{I_c(T)}{I_c(T_r)} = \left(\frac{T}{T_r}\right)^\eta e^{\frac{q}{k} \left( \frac{V_{BE}(T)}{T} - \frac{V_{BE}(T_r)}{T_r} - \left( \frac{V_G(T)}{T} - \frac{V_G(T_r)}{T_r} \right) \right)}$$

$$\ln \left( \frac{I_c(T)}{I_c(T_r)} \right) = \eta \ln \left( \frac{T}{T_r} \right) + \frac{q}{kT} (V_{BE}(T) - V_{GOr}) - \frac{q}{kT_r} (V_{BE}(T_r) - V_{GOr})$$

If the collector current is proportional to some power ( $\delta$ ) of temperature, the above expression can be modified and rearranged as shown below. In [8] [10] proposed an analytical

expression to predict the temperature characteristics of a BJT. Derived from the collector current equation, the  $V_{BE}$  can be expressed as:

$$V_{BE}(T) = V_{GOr} + [V_{BE}(T_r) - V_{GOr}] \frac{T}{T_r} - \eta \frac{kT}{q} \ln\left(\frac{T}{T_r}\right) + \frac{kT}{q} \ln\left[\frac{I_C(T)}{I_C(T_r)}\right]. \quad (2)$$

where  $\eta$  is a process related constant and if the collector current is proportional to  $T^\delta$ ,

$$I_c(T) \propto T^\delta$$

$$I_c(T_r) \propto T_r^\delta$$

(2) can be simplified as

$$V_{BE}(T) = V_{GOr} + [V_{BE}(T_r) - V_{GOr}] \frac{T}{T_r} - (\eta - \delta) \frac{kT}{q} \ln\left(\frac{T}{T_r}\right). \quad (3)$$

## 2.2 $V_{GO}$ Extraction

The PNP substrate BJT is available in most modern CMOS processes and will be used in the following analysis with the assumption that collector current is equal to emitter current. This assumption will not affect the correctness of the following analysis as long as current gain  $\beta$  is constant versus temperature [7] and part of the theory of this method has been introduced in [9].

The  $V_{GO}$  extraction method requires three diode-connected BJTs Q1, Q2 and Q3 with area ratio equal to  $n:1:1$  as shown in Figure 3. Q1 and Q2 should have the same or ratio current. Assuming that  $I_1=I_2$  and an opamp holds the voltages V1 and V2 equal, the  $V_{BE}$  difference between Q1 and Q2 can be calculated based on (2), which is a PTAT voltage named  $V_{PTAT}$ .

$$V_{PTAT} = \Delta V_{BE2,1} = V_T \ln(n) = \frac{kT}{q} \ln(n) \quad (4)$$

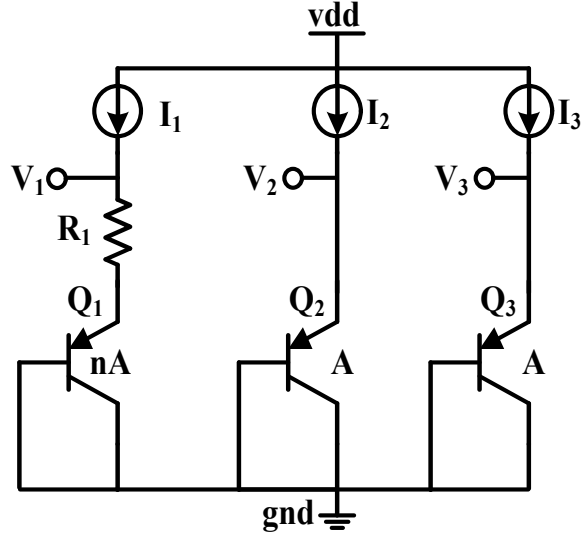


Figure 3. Illustration of using three BJT connected as diodes to extract the VGO.

where  $V_T$  is the thermal voltage and  $n$  is the emitter area ratio. Then  $V_{BE}$  of Q2 equals:

$$V_{BE2}(T) = V_{GOr} + [V_{BE}(T_r) - V_{GOr}] \frac{T}{T_r} - (\eta - 1) \frac{kT}{q} \ln\left(\frac{T}{T_r}\right) \quad (5)$$

The PTAT term in  $V_{BE2}$  can be cancelled using the PTAT current across another resistor with low TC. To compensate the  $T \cdot \ln(T)$  term, Q3's current should have the following property:

$$I_2 / I_3 = a * T^\alpha \quad (6)$$

where  $a$  is a temperature independent parameter and  $\alpha \neq 0$ .  $V_{BE}$  difference between Q2 and Q3 is a superposition of a PTAT term and a  $T \ln(T)$  term is named  $V_{NL}$ :

$$V_{NL} = \Delta V_{BE3,2} = (V_{BE3}(T_r) - V_{BE2}(T_r)) \frac{T}{T_r} - \alpha \frac{kT}{q} \ln\left(\frac{T}{T_r}\right) \quad (7)$$

$V_{PTAT}$  and  $V_{NL}$  can be combined linearly with  $V_{BE}$  in either voltage domain or current domain to extract the  $V_{GO}$  as shown in Fig. 2. To extract  $V_{GO}$ , we will have

$$V_{GO} = A_1 V_{BE2} + A_2 V_{PTAT} + A_3 V_{NL} \quad (8)$$

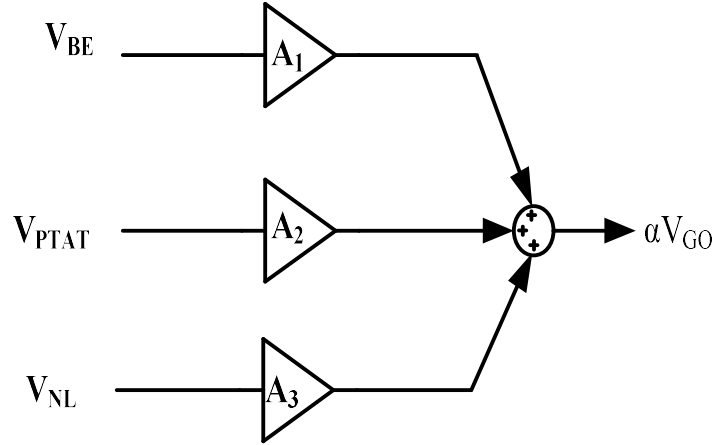


Figure 4. Weighted summation to extract the  $V_{GO}$

Solving (8), the weighted gains can be calculated as follows:

$$A_1 = 1, A_2 = \frac{q}{kT_r \ln(n)} \left( \frac{(\eta-1)}{\alpha} * [V_{BE3}(T_r) - V_{BE2}(T_r)] - [V_{BE2}(T_r) - V_{GO_r}] \right), A_3 = -\frac{(\eta-1)}{\alpha}. \quad (9)$$

In this approach, the voltage reference's performance is determined (6) by  $I_3$  accuracy. Some architectures [12] utilized a first-order temperature independent current ( $V_{BG}/R$ ) or a CTAT current ( $V_{BE}/R$ ) as  $I_3$ , which are not accurate enough to achieve sub-ppm TC. Bootstrapping concept is introduced here to generate a temperature independent current.

## CHAPTER 3. Bandgap Structure

### 3.1 Kuijk circuit

The Kuijk bandgap reference circuit is repeated in Figure 5. The circuit was first discussed in 1973 [2]. Kuijk used diode-connected transistors to sense the variation of the temperature. One method based on Kuijk structure [6] is given here to illustrate how  $V_{GO}$  can be extracted.

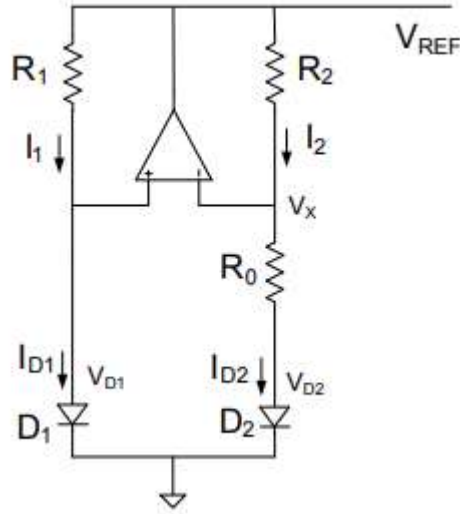


Figure 5. Kuijk bandgap reference circuit

Its analysis is very similar to that of the other two as well. For convenience, it will be assumed that  $R_1=R_2$  [12]. It follows from a basic circuit analysis that the following five equations are independent with the five unknowns  $\{I_{D1}, I_{D2}, V_{D1}, V_{D2}, V_{REF}\}$ .

$$I_{D2} = \frac{V_{D1} - V_{D2}}{R_0}$$

$$I_{D1} = I_{D2}$$

$$I_{D1} = J_{S0} A_1 T^m e^{\frac{V_{D1} - V_{G0}}{n \frac{kT}{q}}}$$

$$I_{D2} = J_{S0} A_2 T^m e^{\frac{V_{D2} - V_{G0}}{n \frac{kT}{q}}}$$

$$V_{REF} = V_{D1} + I_{D2} R_2$$



After simplifying the above equations,

$$V_{ref} = V_{G0} + n \frac{k}{q} \left( \ln \left( n \ln \left( \frac{A_2}{A_1} \right) \frac{k}{q R_0 J_{S0}} \right) - \ln \left( \frac{A_2}{A_1} \right) \frac{1}{R_0} \right) T - (m - 1) n \frac{k}{q} T \ln T$$

### 3.2 One implementation of Kuijk circuit

An implementation of Kuijk structure is shown in Figure 6 [7], a differential opamp OP4 is used to subtract  $V_{BE2}$ ,  $V_{BE3}$  and add the  $V_{NL}$  to the original Kuijk's output  $V_O$  to generate reference voltage  $V_{REF}$ .  $V_{REF}$  is then regulated over a 0 TC resistor  $R_5$  to generate the temperature independent current which is mirrored to  $Q_3$ . Buffers are inserted between  $V_2'$  and  $V_2$ ,  $V_3'$  and  $V_3$  to guarantee  $Q_3$ 's current,  $I_3$  equals to  $M \cdot V_{REF} / R_5$ , which is necessary to make (6) valid.

In this structure, the new output  $V_{REF}$  is used to generate the constant current  $I_3$  and produce  $V_{BE3}$ ,  $V_{NL}$  which is further feedback into  $V_{REF}$ . The bootstrapping concept here makes this  $V_{GO}$  extraction method qualitatively superior to the existing voltage reference generators because they only attempt to cancel the first-order or high-order temperature dependence of  $V_{BE}$ .

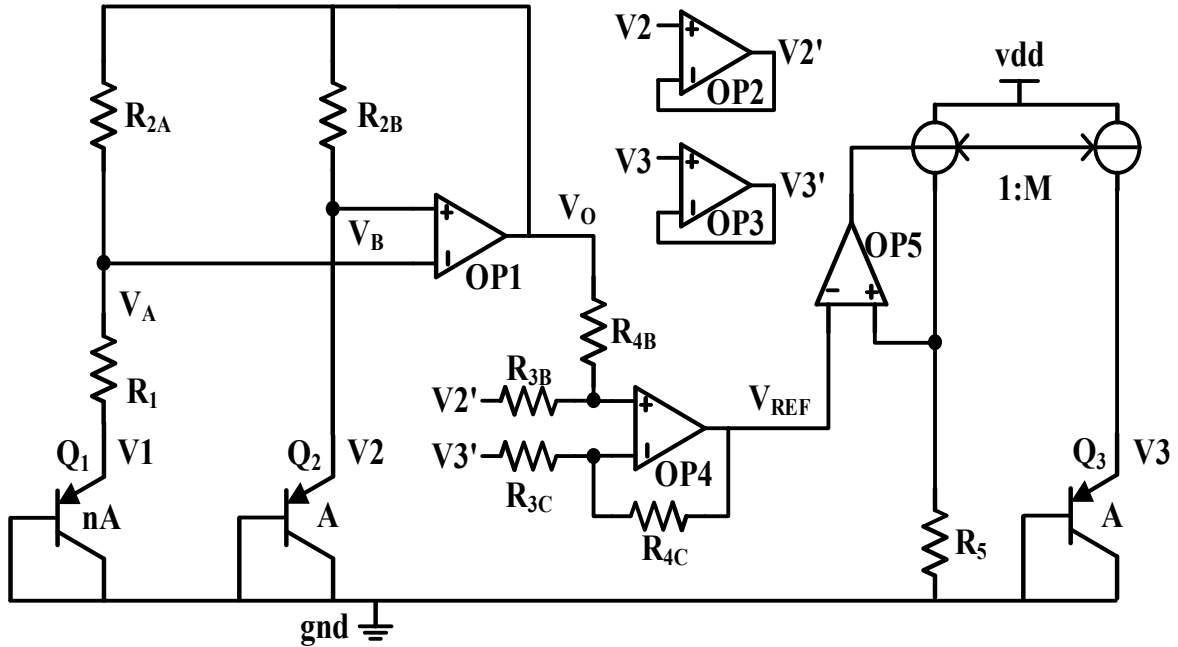


Figure 6. VGO extraction based on Kuijk structure [7].

Careful sizing and layout techniques, i.e., common centroid, should be used for the resistors. Assuming resistors R3B, R3C and R4B, R4C is equal. The voltage reference's output equals to,

$$V_{REF} = V_{BE2} + \frac{R_2}{R_1}(V_{BE2} - V_{BE1}) + \frac{R_4}{R_3}(V_{BE2} - V_{BE3}) \quad (10)$$

Can be compared to (9) with  $\alpha=1$ , the resistor ratios can be calculated to make  $V_{REF}=V_{GO}$ :

$$\frac{R_2}{R_1} = \frac{q}{kT_r \ln(n)} * \{(\eta - 1) * [V_{BE3}(T_r) - V_{BE2}(T_r)] - [V_{BE2}(T_r) - V_{GO}]\}, \quad \frac{R_4}{R_3} = (\eta - 1) \quad (11)$$

R5 and M can be selected so that  $V_{BE3}(Tr)=V_{BE2}(Tr)$  which can further simplify the equations and make the trimming solution simple.

### 3.3 Error reduction techniques

Error sources that can degrade the performance of voltage references which include process variations of  $V_{BE}$ , the mismatch between diodes, opamp offsets, temperature dependence. Which can be seen in (3), process variations of  $V_{BE}$  or mismatch between diodes result in PTAT errors. The spread of  $V_{BE}$  can be corrected by a single room temperature trim, which simultaneously corrects PTAT error due to resistor mismatch. The curvature of  $V_{BE}$  can be corrected by utilizing the difference of  $V_{BE2}$  and  $V_{BE3}$  between two BJTs [2].

Other error sources, temperature dependent on base resistance  $r_b$ ,  $\beta$ , and offsets are typically not just PTAT errors. Substrate PNP has very limited  $\beta$  ( $<10$ ) compared to NPN and its base resistance can be large if the layout is not optimized. Considering these effects, (4) becomes

$$\Delta V_{BE2,1} = V_T \ln(n) + \frac{I_1 r_{b1}}{\beta_1} - \frac{I_2 r_{b2}}{\beta_2} \quad (12)$$

which is not a pure PTAT voltage anymore. All these small error sources will appear at voltage reference output following a transfer function. The total small error  $e(T)$  at  $V_{REF}$  can be expanded into constant,  $T$  and  $T \ln(T)$  bases where  $\varepsilon$  is the residue [7].

$$e(T) = e(T_r) + b_1(T - T_r) + b_2(T - T_r) \ln\left(\frac{T}{T_r}\right) + \varepsilon(T - T_r) \quad (13)$$

Two temperature trimming is implemented here [11]. First, at room temperature ( $T_r$ ),  $R_5$  is tuned to make  $V_{BE3}(T_r) = V_{BE2}(T_r)$  that  $V_{NL} = -\alpha \frac{kT}{q} \ln\left(\frac{T}{T_r}\right)$  and is 0 V at  $T_r$ . Still at room temperature,  $R_{2B}$ ,  $R_{2C}$  is swept across until  $V_{REF} = V_{GO}$ . After  $R_{2B}$  and  $R_{2C}$  are trimmed, the thermal environment is changed to a hot temperature, i.e., 80 °C. Remaining resistors are swept and corresponding  $V_{REF}$  values are measured at this hot temperature. Similarly, the right trimming codes are chosen when  $V_{REF}$  voltage equal to  $V_{GO}$ . In this trimming method, only room temperature and one hot temperature are needed which saves the costs of maintaining thermally regulated testing environments compared to methods requiring cold temperature. Measurement and trimming time may still be long, but that is the price for pursuing sub-ppm performance.

## CHAPTER 4. Modified Kuijk Structure

### 4.1 Objective

The purpose of the modified kuijk circuit is to make a simple circuit while decreasing number of operational amplifiers and resistors in the given circuit. The modified circuit reduces the complexity, decrease area. In this process, new circuit replaces 2 buffers opamps (OP2, OP3), summing opamp (OP4) and decrease number of resistors. The new circuit consists of two single stage amplifiers which work as buffers and summing circuit. Widlar circuit is designed for voltage biasing.

### 4.2 Design

The circuit is designed to add the nonlinear voltage  $V_{NL}$  to Kuijk output  $V_O$  to get a constant voltage  $V_{REF}$ .  $V_{NL}$  is to calculate the difference between  $V_{BE2}$  and  $V_{BE3}$ . The circuit is designed in a way so that it follows the below equations in the industrial temperature range of -40°C to 80°C.

$$I_2 = \frac{I_{tail}}{2} + I_s$$

$$I_3 = \frac{I_{tail}}{2} - I_s$$

$$\Delta V_{ref} = \Delta I_{ref} * R_{ref}$$

$$V_{ref} = V_o + \Delta V_{ref}$$

$$V_{ref} = V_o + V_{NL} \left( \frac{1}{R_S * g_m} \right)$$

$$V_{ref} = V_o + V_{NL} \left( \frac{\beta R_w}{R_S} \right)$$

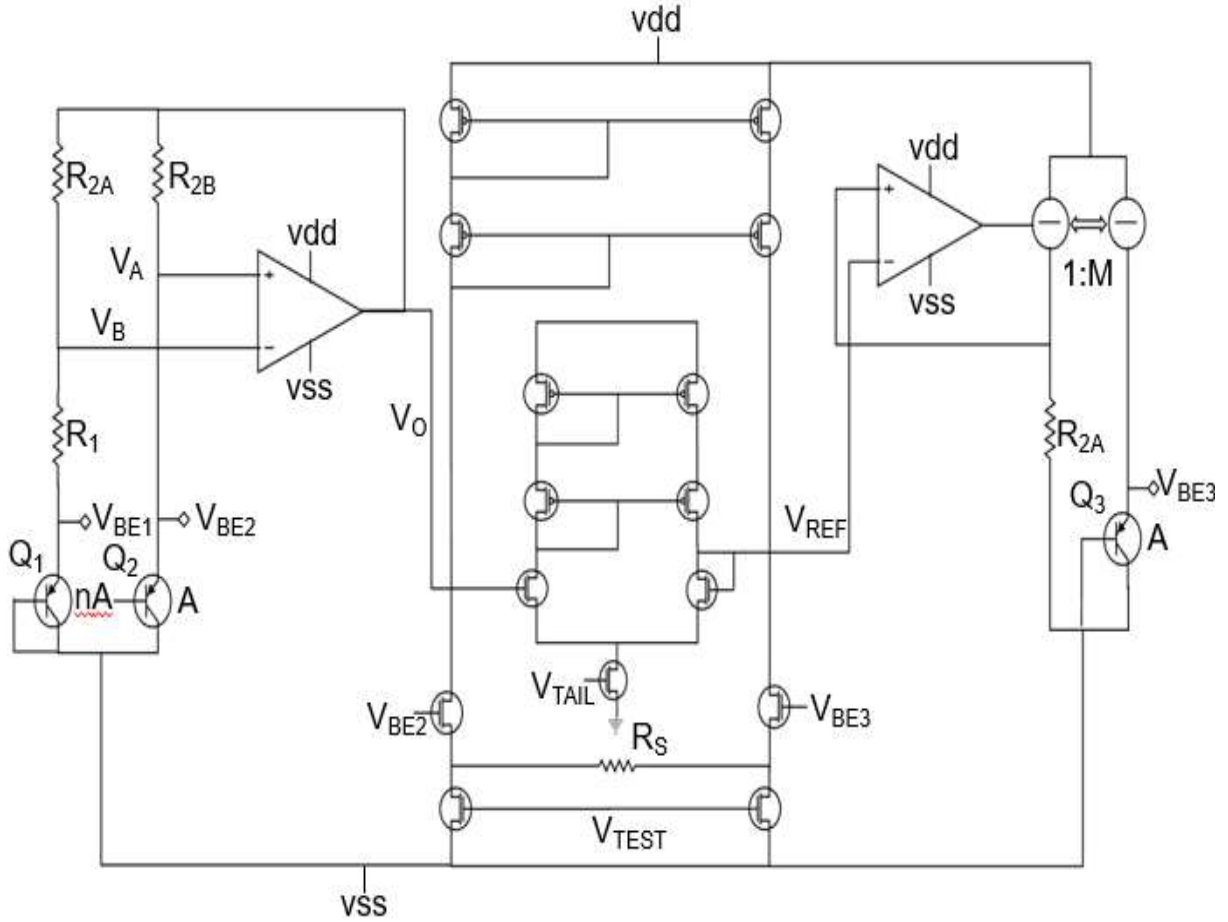
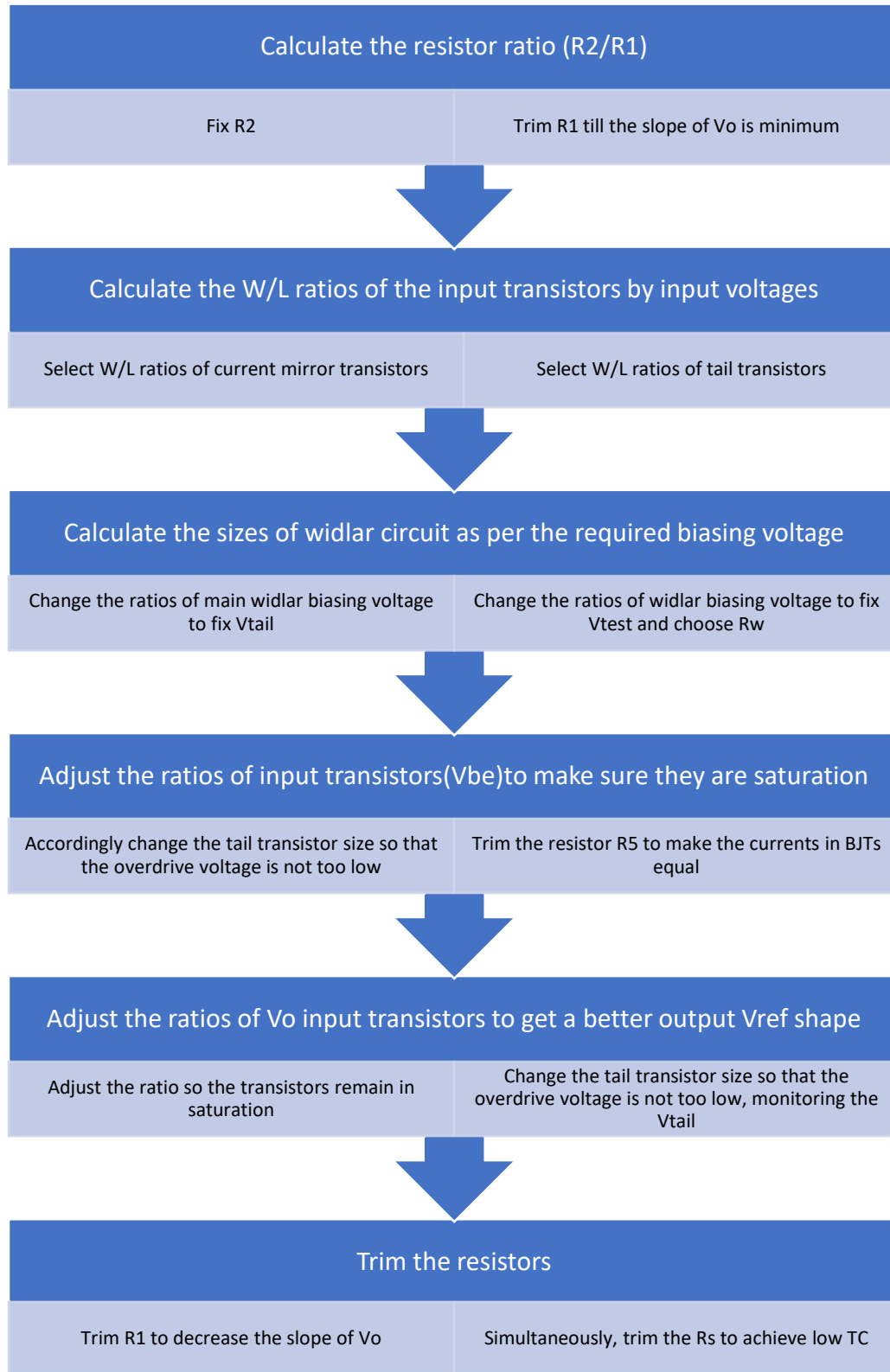


Figure 7. Modified VGO extraction based on Kuijk structure

The modified circuit is built with nfet33 as inputs and the current mirror is formed by pfet33 transistors. In this design total, 15 transistors are used and sized according to stay in saturation and act as a buffer and summing circuit. And the voltage biasing for the circuit is done by the Widlar circuit. Where the current mirror transistors have a good range of selection for the W/L ratio. While the W/L ratio range is limited for the nfet33 transistors because of its low gate voltages.

Flow chart describes the steps followed while designing the circuit



## CHAPTER 5. Results

### 5.1 Simulation of Kuijk circuit

The proposed  $V_{GO}$  extraction method is verified in a 130nm CMOS process.  $V_G(T)$  in this process can be decomposed to a constant term  $V_{GO}$ , a PTAT term, a  $T\ln(T)$  term and residue errors. The residue errors ( $\sim 100$  uV) will limit the temperature drift to about  $0.5$  ppm/ $^{\circ}\text{C}$ . The W/L ratio of the unit resistor is taken so that their positive body TC and negative body TC can be cancelled. The final TC of a unit resistor is  $0.5$  ppm/ $^{\circ}\text{C}$ . To save the efforts of implementing chopping or auto-zeroing in opamps, spice models of ADA4528 is used in the simulation of Kuijk circuit [7].

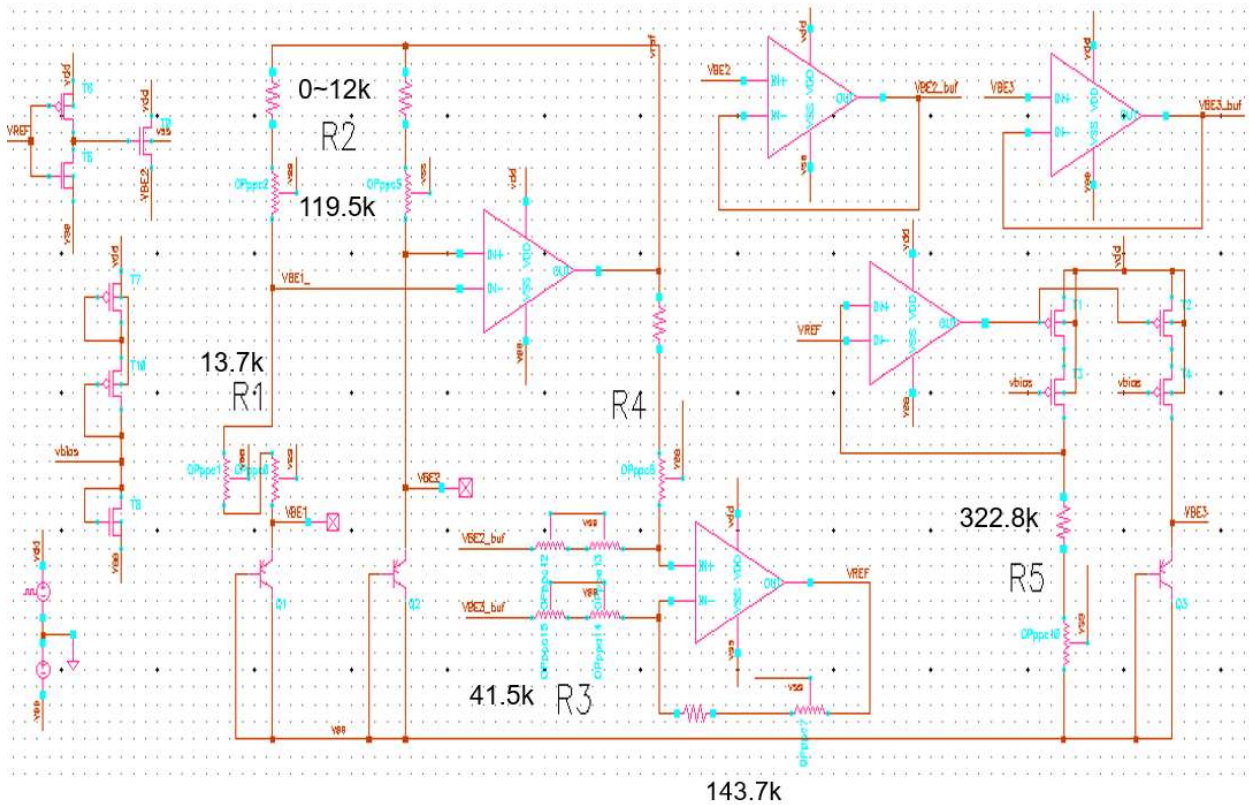


Figure 8. Schematic of the Kuijk circuit

The output of Kuijk circuit  $V_o$  and the constant voltage  $V_{ref}$  were plotted in the below graph,  $V_{ref}$  is nearly constant at 1.119V. The temperature coefficient is calculated as 0.3 ppm/°C, the difference between the base emitter voltages as  $-37\mu V$ .

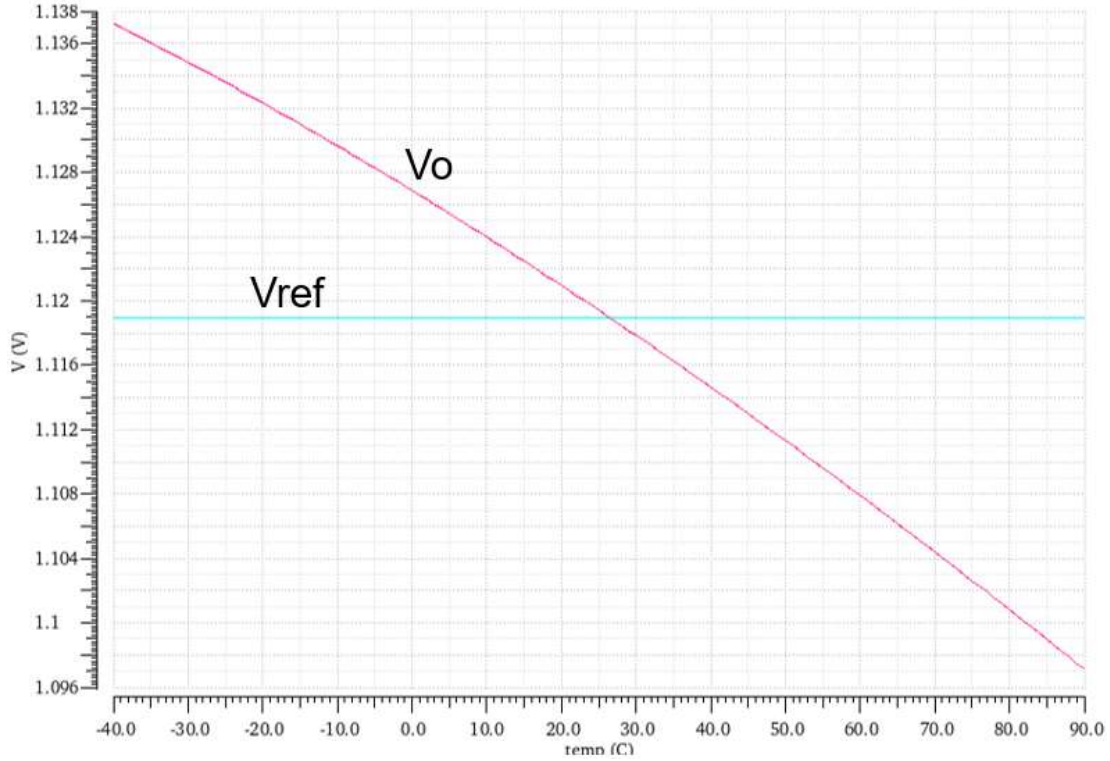


Figure 9. Output of Kuijk circuit

## 5.2 Simulation of modified Kuijk circuit

As mentioned earlier, the new Kuijk circuit replaces the OP2, OP3, OP4 and the resistors R3B, R3C, R4B and R4C. The resistor ratios are taken in such a way that it follows (14). The spice models of ADA4528 is used in the simulation of Kuijk circuit.

$$V_{ref} = V_o + V_{NL} \left( \frac{\beta R_w}{R_s} \right). \quad (14)$$

Where  $R_w$  and  $R_s$  values are 45K and 14.29K.



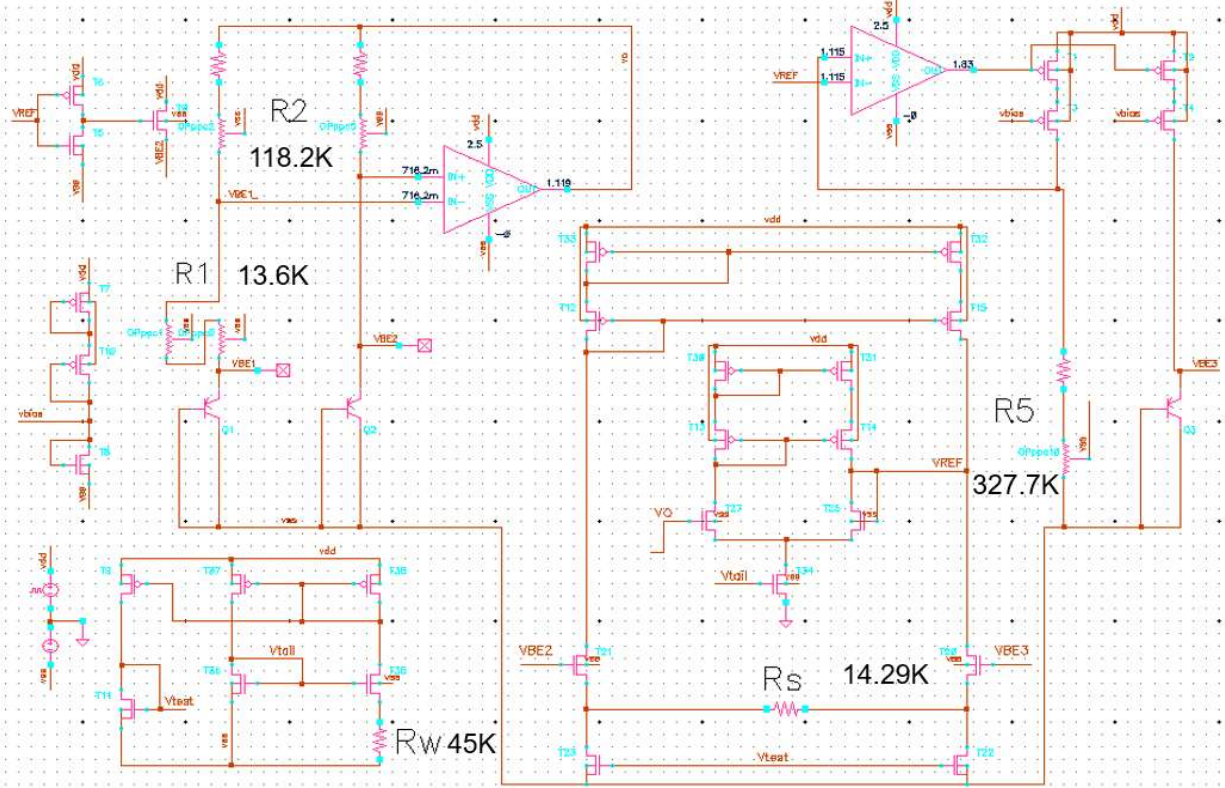


Figure 10. Modified Kujik circuit

The modified circuit is built with nfet33 as inputs and the current mirror is formed by pfet33 transistors. In this design total, 15 transistors are used and sized according to stay in saturation and act as a buffer and summing circuit. And the voltage biasing for the circuit is done by the widlar circuit. Where the current mirror transistors have a good range of selection for the W/L ratio. While the W/L ratio range is limited for the nfet33 transistors because of its low gate voltages.

For the VBE input circuit, current mirror transistors, the W/L range can start from 16 till 0.33 where the transistors could stay in saturation but for the input transistors the W/L ratio range is 2 to 0.25. There is a tradeoff between overdrive voltages of input transistors and the drain voltage of tail transistors. Sizing is done by balancing both and keeping all the transistors in saturation.

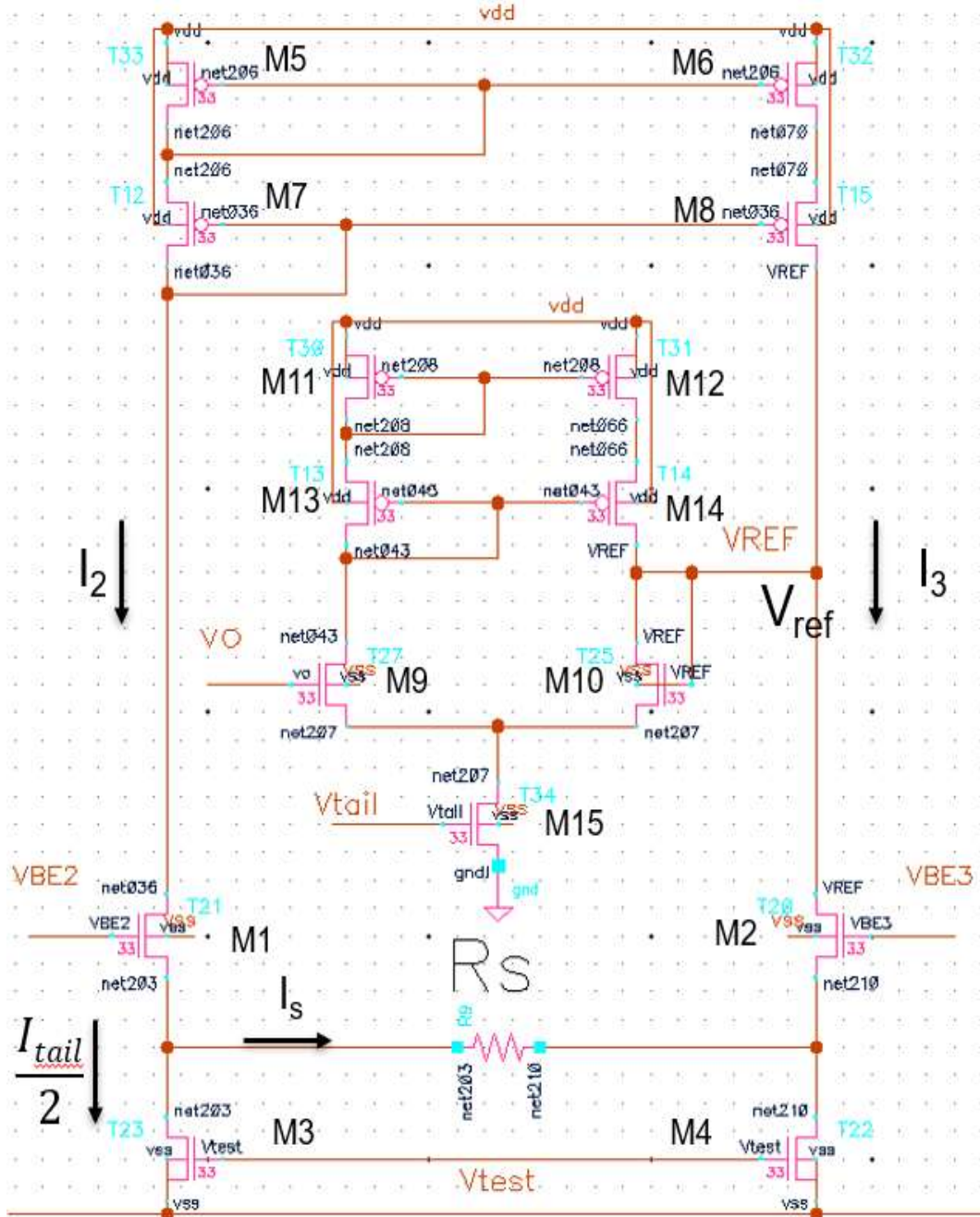


Figure 11. New circuit

In the above circuit, the  $V_{tail}$  and  $V_{test}$  are generated by the widlar circuit which is swept across the temperature.  $V_o$  and  $V_{ref}$  are plotted on the below graph,  $V_{ref}$  is nearly constant at 1.115V. The temperature coefficient is around 3.5 ppm/°C, the difference between the base emitter voltages as 194.4nV.

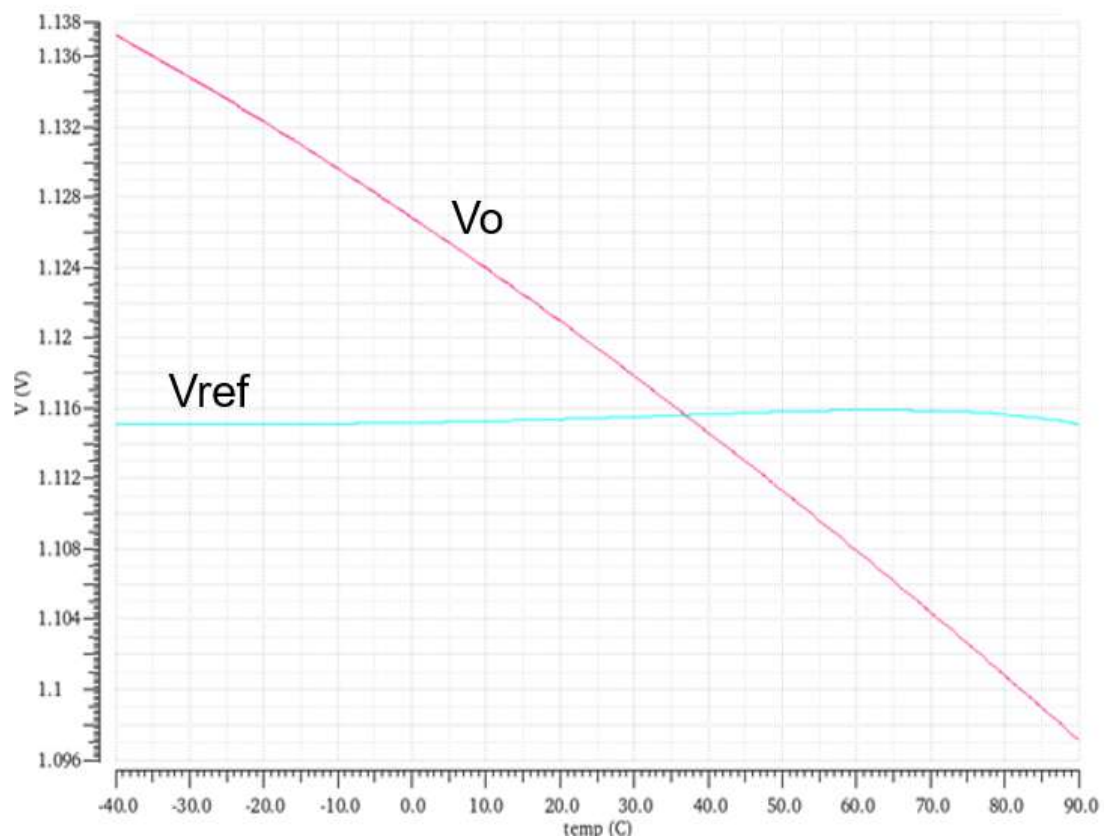
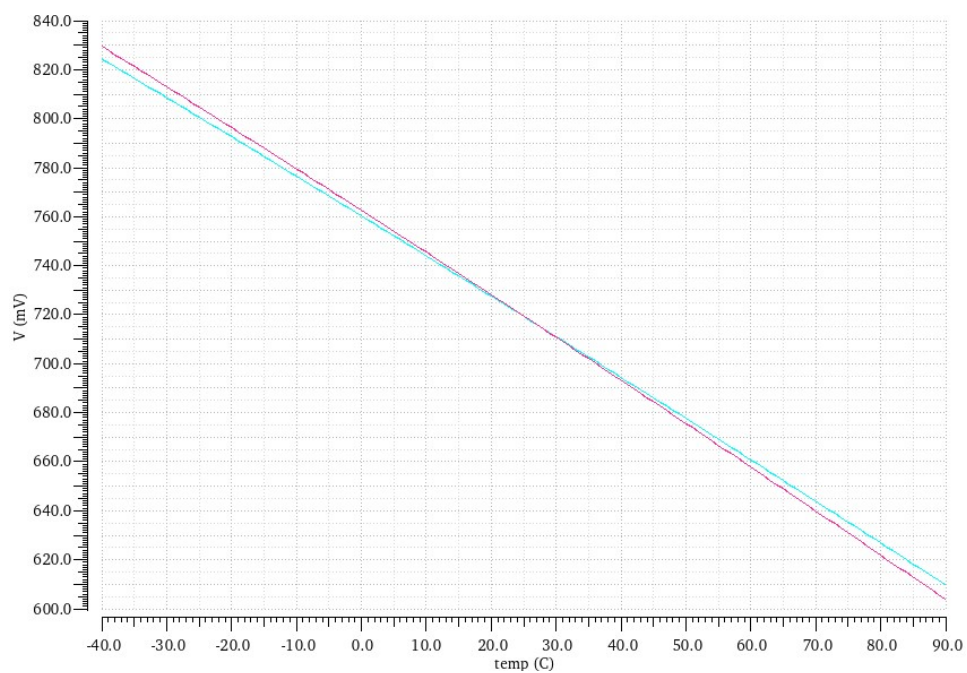
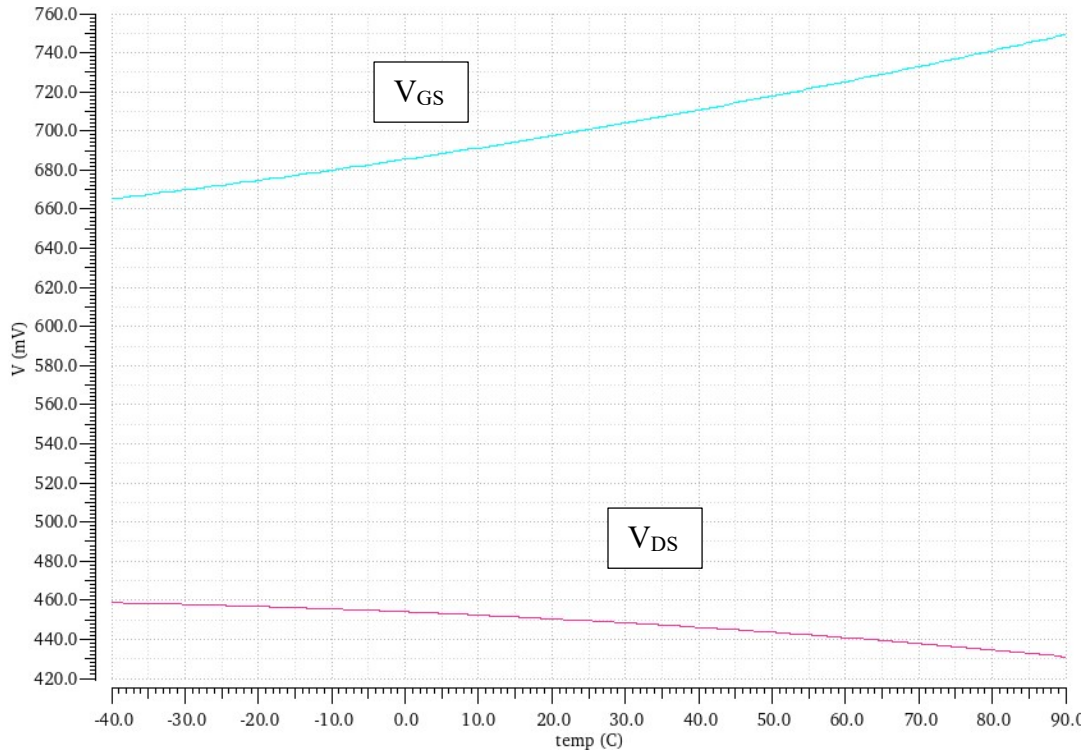


Figure 12. Output of modified Kuijk circuit

Figure 13.  $V_{BE2}$  and  $V_{BE3}$

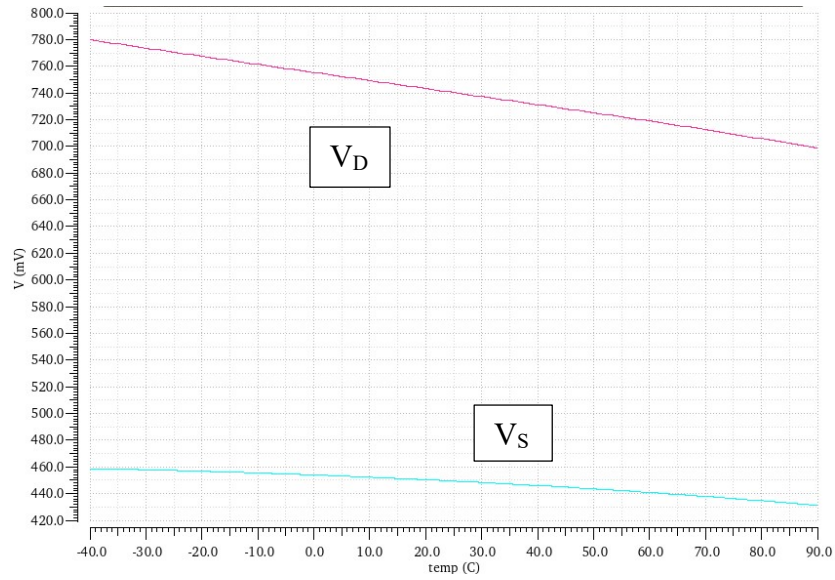
Few graphs of the voltages of transistors are plotted against temperature which is used to confirm the transistors are in saturation. And using the graphs observation was made that above the industrial temperature range of  $-40^{\circ}\text{C}$  to  $80^{\circ}\text{C}$ , few transistors are no longer in saturation. The table shows the values of the voltages of the transistors that are changed over the range of temperature from  $-40^{\circ}\text{C}$  to  $80^{\circ}\text{C}$ .



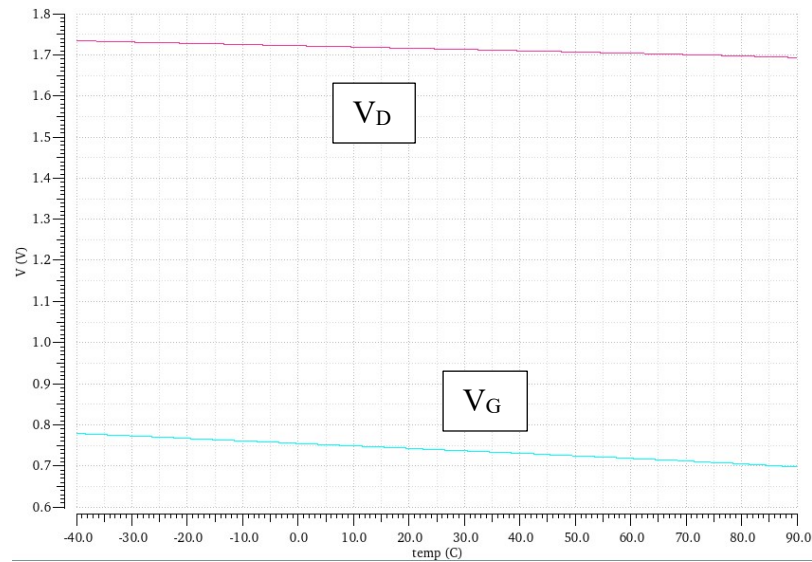
(14.1)  $V_{th}$  is 456.3

For the  $V_{BE}$  input circuit, the change in W/L ratio of the M5 to M8 will alter the threshold voltage and overdrive voltage of the transistors (M5 - M8). The W/L ratio of the M1, M2 transistors changes its overdrive voltage and source voltage. The W/L ratio of M3, M4 can alter the overdrive voltages of M1 to M8. Considering all the parameters the sizes are calculated.





(14.2)



(14.3)

Figure 14. Voltage variations

The modified circuit, uses a simple single stage amplifiers to replace three operational amplifiers and decrease two resistors which occupies lot of area. This circuit consumes 50% less power.

This circuit can be used in low accuracy, low power and integrated applications.

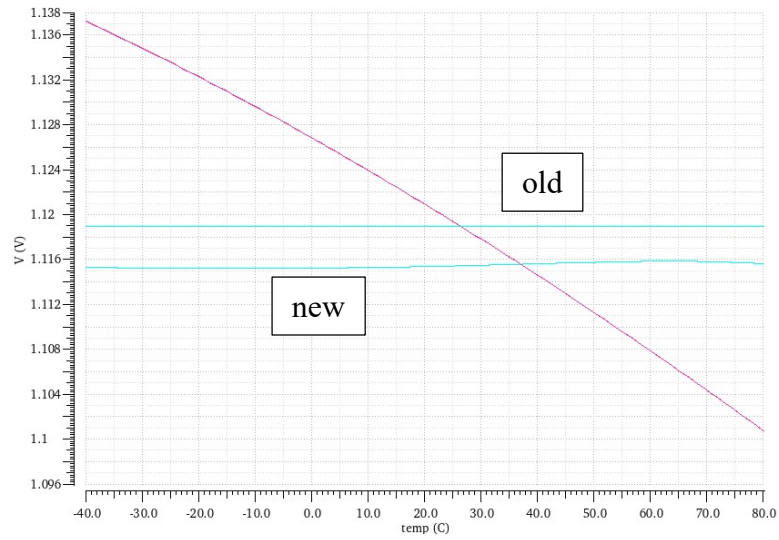


Figure 15. Output Results

Table 1. Voltage values over the temperature range

	$V_d$	$V_s$	$V_g$	$V_{ds}$	$V_{gs}$	$V_{th}$	$V_{od}$
<b>M1</b>	1.32–1.42	205–85m	825-670m	1.11-1.34	620-585m	492.5m	127.5-92.5m
<b>M3</b>	225-105m	0	550-543m	225-105m	550-543m	456.1m	193.9-86.9m
<b>M5</b>	1.96-1.99	2.5	1.96-1.99	540-510m	540-510m	424.6m	115.4-85.4m
<b>M7</b>	1.32-1.42	1.98-2.02	1.32-1.42	660-396m	660-396m	559.7m	101-164m
<b>M9</b>	1.73-1.69	2.5	770-810m	1.73-1.69	770-810m	442.9m	327.1-367.1m
<b>M11</b>	780-700m	1.73-1.69	778-990m	780-700m	778-990m	634.9m	143.1-355.1m
<b>M13</b>	780-700m	459-431m	321-269m	1.13-1.09	678-667m	539.2m	138.9-128m
<b>M15</b>	459-431m	0	459-431m	665-755m	665-755m	456.7m	208-289m

### 5.3 Widlar circuit

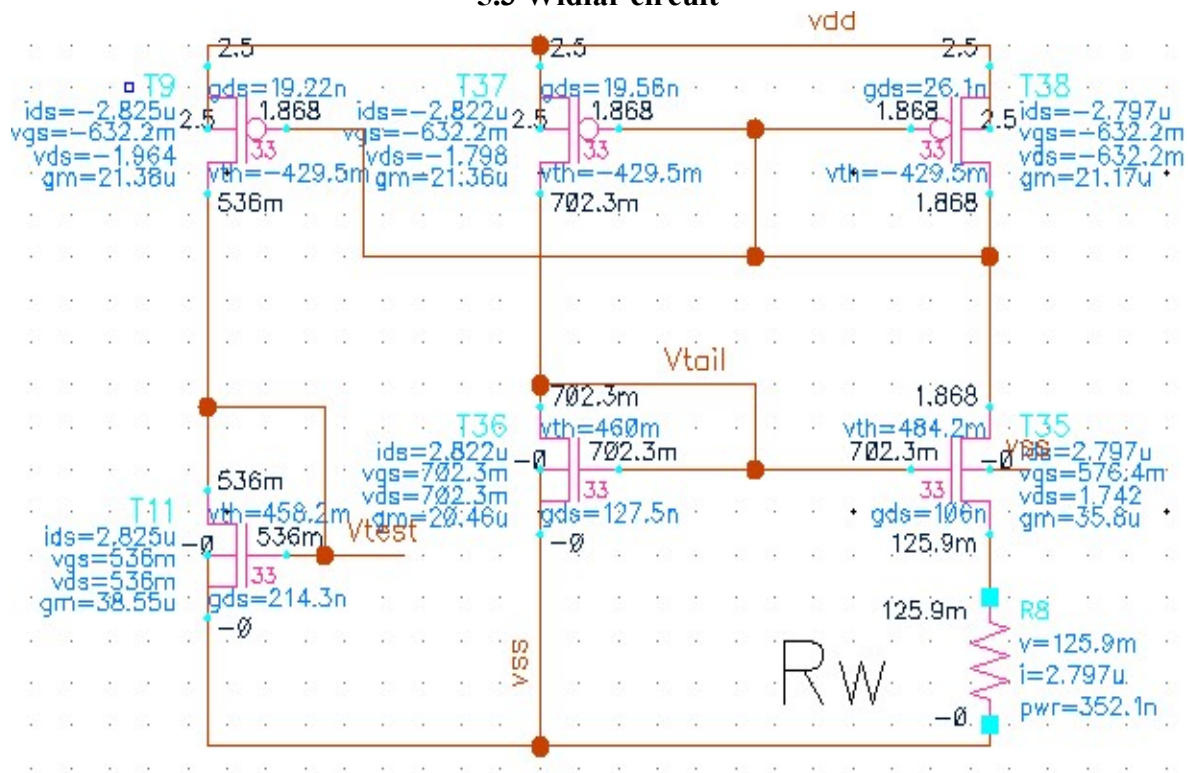


Figure 16. Widlar circuit

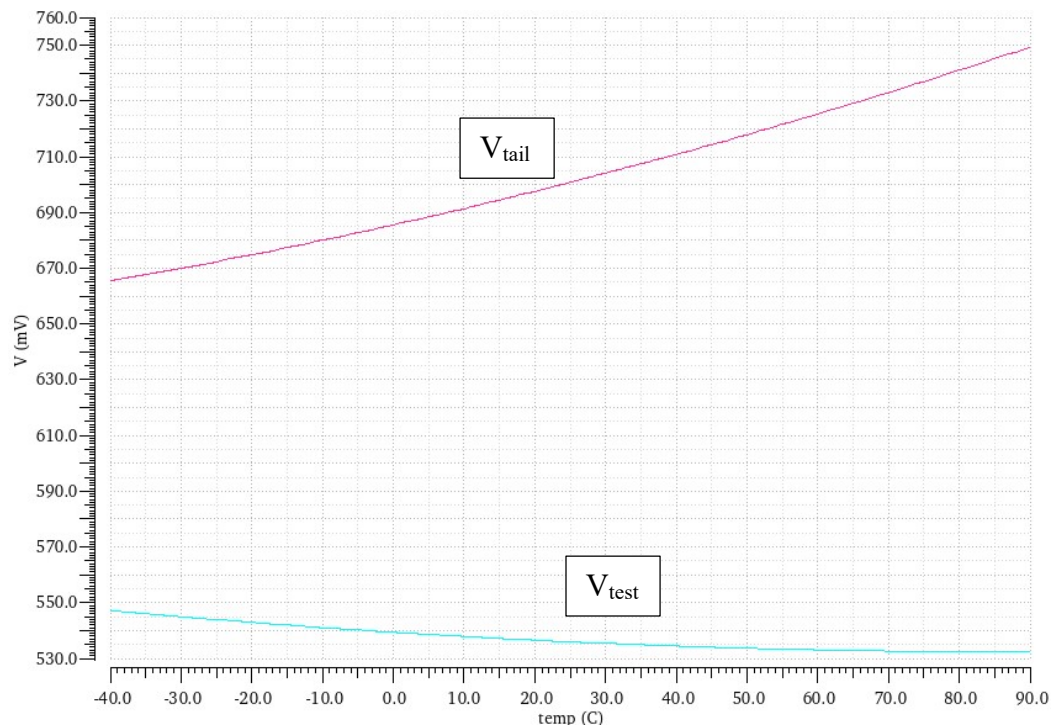


Figure 17. Biasing voltages

## CHAPTER 6. Conclusion

This creative component proposed a method to extract  $V_{GO}$  from the temperature characteristic of base-emitter voltage ( $V_{BE}$ ) in a bipolar transistor. Small error sources which can affect the voltage reference performance are analyzed and their effects on the temperature coefficient can be minimized after trimming. This analysis and modified method used to decrease the number of operational amplifiers and resistors which makes the circuit less complex, reduces area and power requirements. The performance of the circuit was verified experimentally. The presented method is implemented in the Global Foundries 130nm process. Simulation results show that the design can achieve sub-ppm level temperature coefficient over an industrial temperature range from  $-40\text{ }^{\circ}\text{C}$  to  $80\text{ }^{\circ}\text{C}$ .



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