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Switched capacitor, self-referencing sensing scheme for high-density magnetoresistive memories

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Switched capacitor, self referencing sensing scheme for high density magneto-resistive memories

by

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CHAPTER 1. INTRODUCTION

1.1 Review of Storage Technologies

Computer memories play a key role in computer technology since they have a major impact on the cost and performance of any computer. For many years, considerable effort has been put in to developing these memories and great advances have been made in speed improvement and cost reduction.

There are many types of storage technologies in use today. They vary considerably in performance and cost. The most dominant technologies are described below.

1.1.1 Static random access memories (RAM)

These memories are the fastest memories available commercially. The memory stores data in a cell which acts as a bi-stable latch. Figure 1.1 shows a six transistor storage cell. Complimentary metal oxide semiconductor (CMOS) versions offer access times of 20 - 50ns and the emitter coupled logic (ECL) versions offer access times of 5 - 10 ns. Due to the very high cost of these memories they are mainly used as high speed caches and registers. The data need no refreshing (ie rewrite of data periodically) and is volatile (i.e., data does destroy when power down).

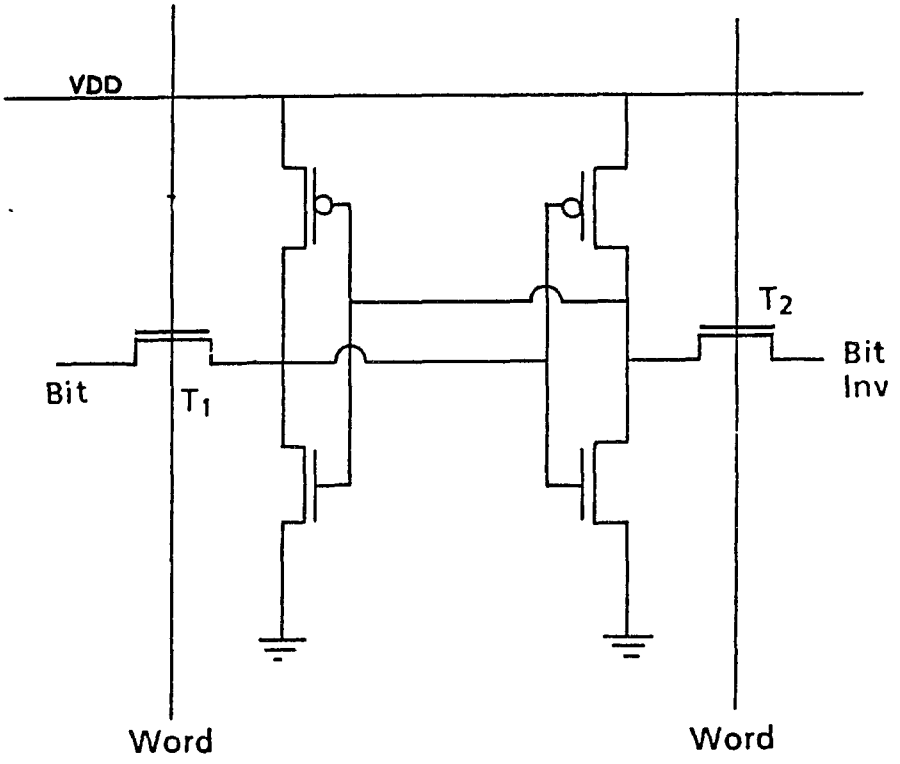


Figure 1.1 Six transistor Static RAM cell

1.1.2 Dynamic RAM's

These memories are very dense and the data is stored as a charge in a capacitor. A typical cell consists of a capacitor to store data and a transistor to switch the capacitor in to the access rails. This cell shown in Figure 1.2. The capacitor is generally made to be an oxide capacitor. Several techniques used to construct this capacitor are shown in Figure 1.3. Recently high density 16Mbit memories have been produced. Dynamic RAM memories have destructive read out and need periodic refreshing to recharge the capacitor to its bit value. The refreshing must be done approximately every 2ms. A typical cell size is 4.5 μm^2. The memory is also volatile and has a typical access time of 100 - 200ns. This technology is mainly used for primary storage in computers and is the main type of semiconductor memory in use. The Dynamic RAM has grown rapidly in the past few years and Table 1.1 [1] shows the growth and the future projections for this memory.

1.1.3 Hard Disks

Unlike the dynamic RAM's hard disk memory is not a solid state storage device. It contains rotating magnetic disks where data is stored, and a magnetic head to read or write data. The storage density on these disks is very high . One such 5.25 inch diameter disk can store up to 1.2 Gbytes of data [1]. The disadvantage of this device is that it does not provide random access. Thus the access time is very high compared to the Dynamic RAMs. A typical disk access time would be 20ms [1]. The data is usually stored in blocks and is read serially within a block. Once started reading data in a block, the data transfer rate can be as high as 25Mbits/s.

This storage is non volatile and the cost/byte of these devices are very much less than Dynamic RAMs. Thus these devices are mainly used for on line secondary storage, where

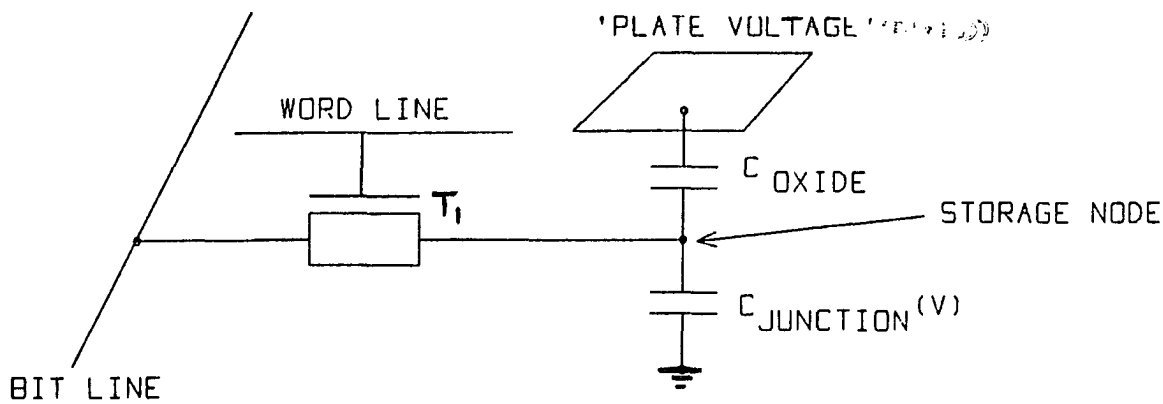


Figure 1.2 One transistor Dynamic RAM cell

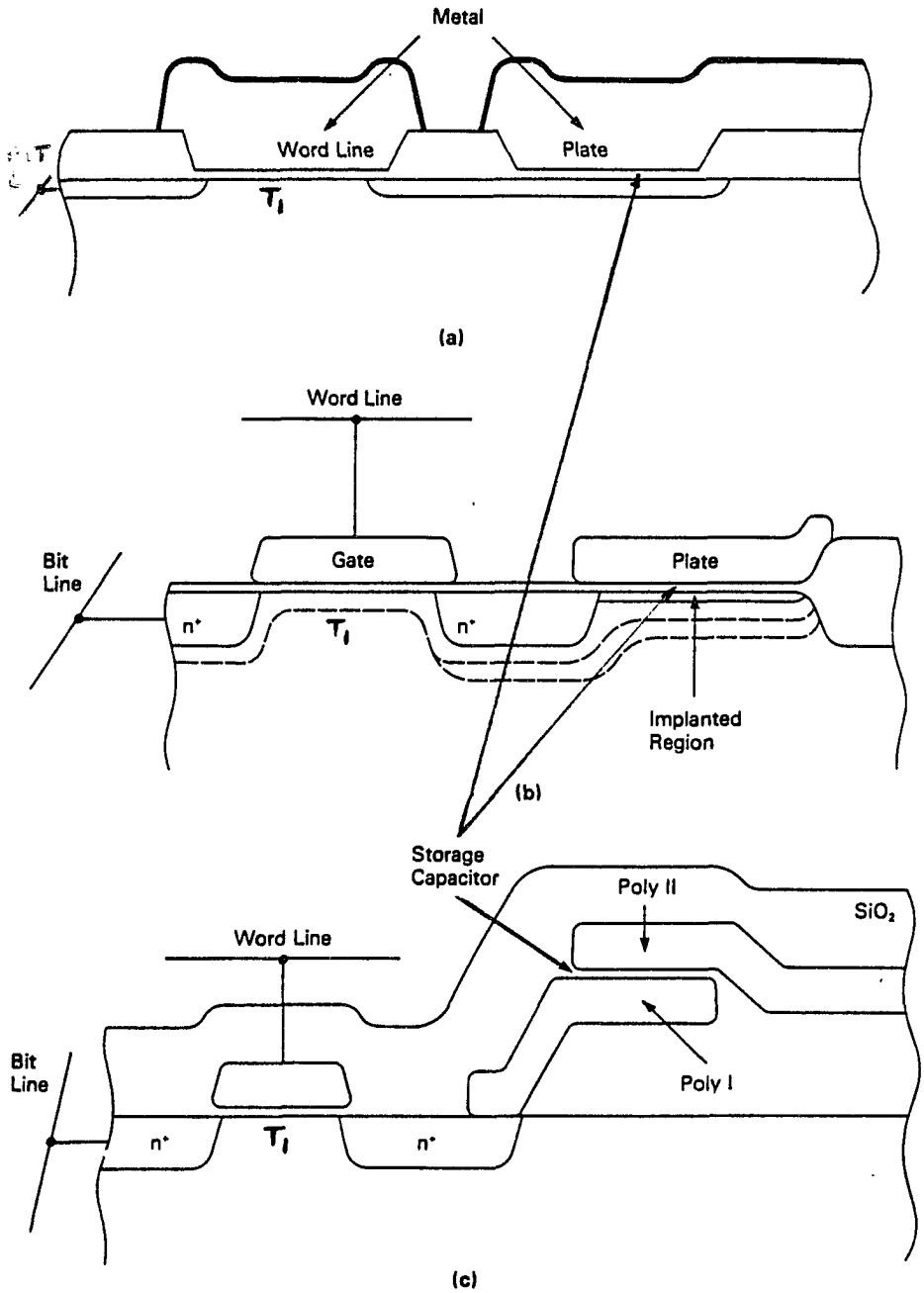


Figure 1.3 Three possible implementations of a DRAM cell capacitor,

(a) metal plate (b) polysilicon plate (c) two ploysilicon plates

Table 1.1 Current DRAM technology and projections

YEAR INTRODUCED: (Qualifaction - 1M/yr)	1983	1985	1988	1991	1994	1997	2001
DRAM Size	256K	1M	4M	16M	64M	256M	1024M
Vdd (volts)	5	5	5	5/3.3	3.3	3.3	3.3
Min. Feature (μ)	1.5	1.0	0.8	0.5	0.3	0.25	0.15
Metal Pitch (μ)	5.0	3.5	2.5	1.5	1.0	0.8	0.78
Overlay Requirement (μ)	0.5	0.35	0.25	0.15	0.12	0.075	0.05
Killing Defect (μ)	0.3	0.25	0.15	0.1	0.06	0.05	0.02
Cell Size (sq. mic)	38	20	9	4.5	2	0.9	0.4
Gate Oxide Thickness (A)	250	200	200	150	100	85	75
Die Size (sq. mm)	41	59	78	98	190	400	415
Wafer Dia (mm)	150	150	150	250	250	250	250/300
Die/Wafer	360	263	191	271	162	103	100
Mask Levels (average)	10	16	18	22	25	28	32
Defects/cm^2	0.8	0.7	0.5	0.4	0.3	0.08	0.05
Defects/cm^2/mask	0.08	0.045	0.03	0.015	0.008	0.003	0.0015

data is read, one block at a time, into the primary storage. Currently research is being done to use magneto-resistive memory read heads which would permit higher storage densities in hard disks.

1.1.4 Flash memories

These memories were developed recently and they use floating gate technology to store data. The presence or absence of trapped charges in a floating CMOS gate determines whether the gate is on or off. This in turn gives the state of the bit stored. This memory is random accessible and has a density approaching 1Mbit for a single chip [2]. The read access time is 100 - 200ns and the storage is non volatile. The two main disadvantages of these memories are the high write time of 10ms/byte and the limited writes that can be done. The maximum number of writes possible is 10,000 [2]. This prevents it being used as a primary or secondary storage device which generally experiences a large number of writes. However this technology is a very attractive alternative to electrically erasable programmable memories (EEPROMs) which is mainly used for firmware and any type of configuration storage such as in programmable logic devices (PLDs).

1.1.5 Bubble memories

This memory has only serial access. The data is stored as a moving magnetic bubble and the storage is non volatile. Since the memory is serially accessed the average access time for a given bit is very high. Thus it cannot be used as a primary memory. The cost of these memories compare to DRAMs which prevents them from being used for secondary storage. Further improvements are needed for this memory to be used for any major application.

1.1.6 Ferroelectric memories

This memory has random access storage. The data is stored in the ferroelectric dielectric material, and uses hysterisis in the polarization of this dielectric for storage of data. This memory needs refreshing and the storage is non-volatile. The main problem of this device is the wear out of the dielectric. Due to this the memory cannot be written or read a large number of times and this prevents it being used as a primary or secondary storage. However it could be used for firmwear or any other application where the number of accesses are limited (eg. storage of the configuration of a system).

1.1.7 Tape Systems

In tape systems the data is stored serially on a removable magnetic tape. The average access time is approximately 15 seconds and each tape stores about 2Mbytes of data [1]. This costs very much less than hard disks and is mainly used for archivel storage of data.

1.2 Evaluation of Different Storage Technologies

When evaluating a storage technology three parameters are of main interest.

They are: (1) Density

(2) Access time

(3) Cost/bit

Very often a cost/bit vs access time graph is used to compare the performance of storage technologies. Such a graph is shown in Figure 1.4[1] in which points corresponding to the current storage technologies are plotted. It can be seen clearly that the successful popular technologies such as static RAMs, Dynamic RAMs, Hard disks and Tape systems do tend

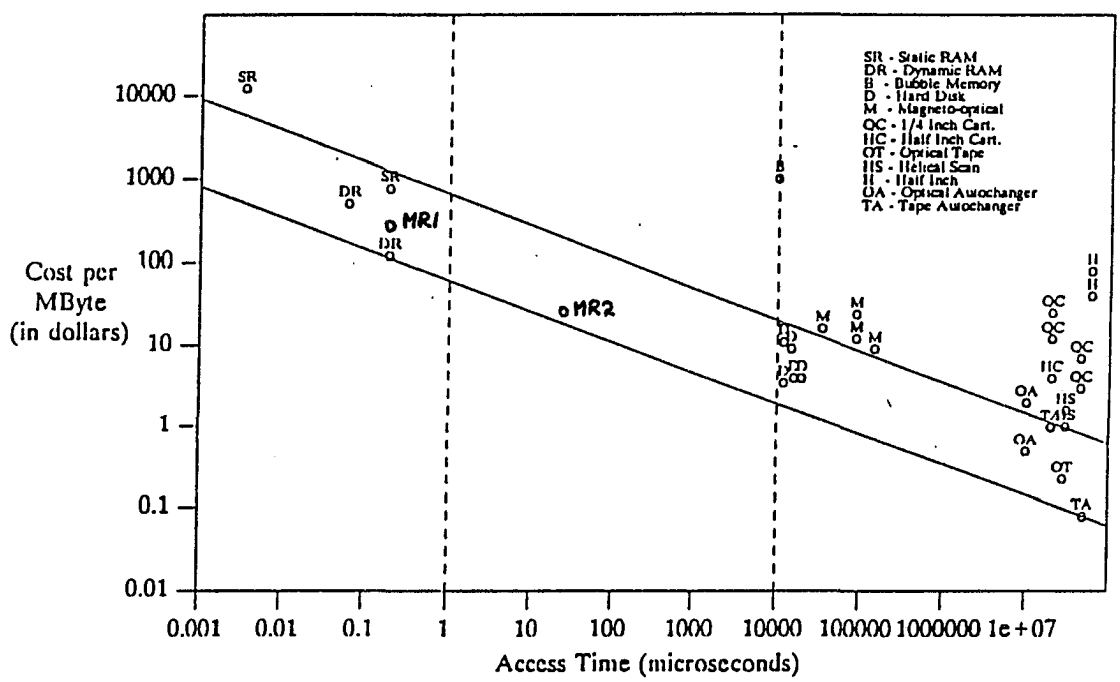


Figure 1.4 Cost/Mbyte vs Access time plot for current storage technologies

to fall into a straight band like region as indicated in the graph. The negative gradient of this band indicates the fact that the industry would like to spend more money for low access time storage. It could be predicted that in order for a new technology to succeed, its access time and cost parameters must fit in to this band or must fall below this band.

It also could be noticed that there is a large gap in the graph between dynamic RAMs and Hard disks. Any new technology that falls into this gap could easily be used as a disk cache which is not practical using today's technology.

Recently a new type of memory technology has been discovered. This memory is called Magneto-resistive memory and it stores data magnetically in a ferromagnetic film. There are many attractive properties of this memory.

They are:
(1) Random accessibility
(2) Very short write times
(3) Density close to Dynamic RAMs
(4) Size is scalable with lithography
(5) Very low cost
(6) Radiation hardness
(7) Non - Volatility

In this memory the read access time is inversely proportional to the bit size. Since the cost/Mbyte decreases with the bit size the memory access time is inversely proportional to the cost/Mbyte. It has been shown that access times of as low as 50ns are achievable. A 16K version has been successfully fabricated and a 1M bit version is currently being laid out. These two versions have been plotted in the graph in Figure 1.4 as "MR1". It clearly indicates that these memories do fall into the suggested band and have the potential of being successful. As magneto-resistive memory technology improves, the cost/Mbit and access time is expected to shrink rapidly. In fact a recent discovery of a new variation of this

memory, called Giant magneto-resistive memory, indicates that ten times lower access times and $4\mu m^2$ cell size (current 16Mbit Dynamic RAM density) is possible [3]. Thus these magneto-resistive memories are expected to challenge the Dynamic RAM market in the near future.

In addition the magneto-resistive memory could be used as disk caches by increasing the density and lowering the cost at the expense of access time. This is mainly possible using wafer scale technology. The performance projection for this type is indicated in Figure 1.4 as "MR2".

In addition to these applications (as disk caches, and as an alternative to Dynamic RAMs) many other niche applications do exist. Due to the radiation hardness and the non volatile property this memory could be used to replace plated wire memories in military and space environments. Currently plated wire memories are used in these environments since radiation does destroy the storage in Dynamic RAMs, Static RAMs and floating gate type memories (EEPROM, EPROM, Flash). The disadvantages of these plated wire memories are that they require very large currents, have very large cell sizes and cost very much. Thus the magneto-resistive memories provides an excellent alternative. These memories also could be used for remote data recorders and as firmware (alternative to floating gate technology [4]) and as configuration storage devices.

Currently a research effort is underway to develop a 1Mbit magneto-resistive memory. In the development of such a device the magneto-resistive element technology and the sensing scheme (which generates logic data form the storage element signal) are the most important factors in determining its performance. This dissertation presents the work done in developing the sensing scheme.

CHAPTER 2. THE MAGNETO-RESISTIVE ELEMENT

2.1 Magneto-Resistance

Magneto-resistance is an effect such that when a magnetic material is subjected to a magnetic field its electrical resistance would change. The magneto-resistive effect could be explained in detail using the electron model of atoms. In a magnetic material, the magnetization is formed by the magnetic field generated by the electrons of each atom which spin around each nucleus. When an external magnetic field is applied the magnetization rotates thus deforming the spinning electron cloud. This deformation changes the amount of scattering experienced by the conduction electrons as they travel through the material. The change of scattering reflects as a change in resistance.

2.2 Magneto-Resistive Material used

The magneto-resistive element uses a thin magnetic film to store data. This film exhibits the magneto-resistive effect. It is sandwich structured and contains two 150 A thick magnetic layers separated by a 50 A thick non magnetic layer. The two magnetic layers are used to reduce the demagnetization effect. A ternary alloy of 65% Ni, 15% Fe and 20% Co is used as the magnetic material. The change in resistance due to magneto-resistive effect is approximately 2.4% [5]. The 50 A separation layer is made of high resistive tantalum. Thus when current is passed through the element (parallel to the layers) most of the current tends to flow through the double magnetic layers.

2.3 Structure and Fabrication of the Magneto-Resistive Element

The basic structure of the magneto-resistive cell is shown in Figure 2.1. The active magneto-resistive element area is darkened. These magneto-resistive elements are rectangular (looking from top) with an aspect ratio of 5-10: 1 (length: width). Currently elements with lower aspect ratios are being tested [3]. There are two main axes associated with the magneto-resistive element. They are called the easy axis and the hard axis as seen in Figure 2.1. The magnetization at the middle of the film would be most stable along the easy axis, and the hard axis is perpendicular to the easy axis. There are two possible memory cell geometric configurations. The configuration where the length of the element is along the easy axis is called a longitudinal element and the case where the length is along the hard axis is called a transverse element (Figure 2.1). In memory applications only the transverse element is used.

In the magneto-resistive elements the magnetic film forms a conductor (along the hard axis) and this conductor is called the sense line as indicated in Figure 2.1. This conductor carries a sense current which flows through the magnetic material. When a magnetic field is present, this current will experience a change in resistance, due to the magneto-resistive effect.

Above the sense line is the word line which is electrically isolated from and orthogonal to the sense line as shown in Figure 2.1. This is a low resistance conductor which also carries a current, called word current. The combination of these two lines form a magneto-resistive storage cell. The top view and the cross section of a magneto-resistive cell (when laid out) is shown in Figure 2.2.

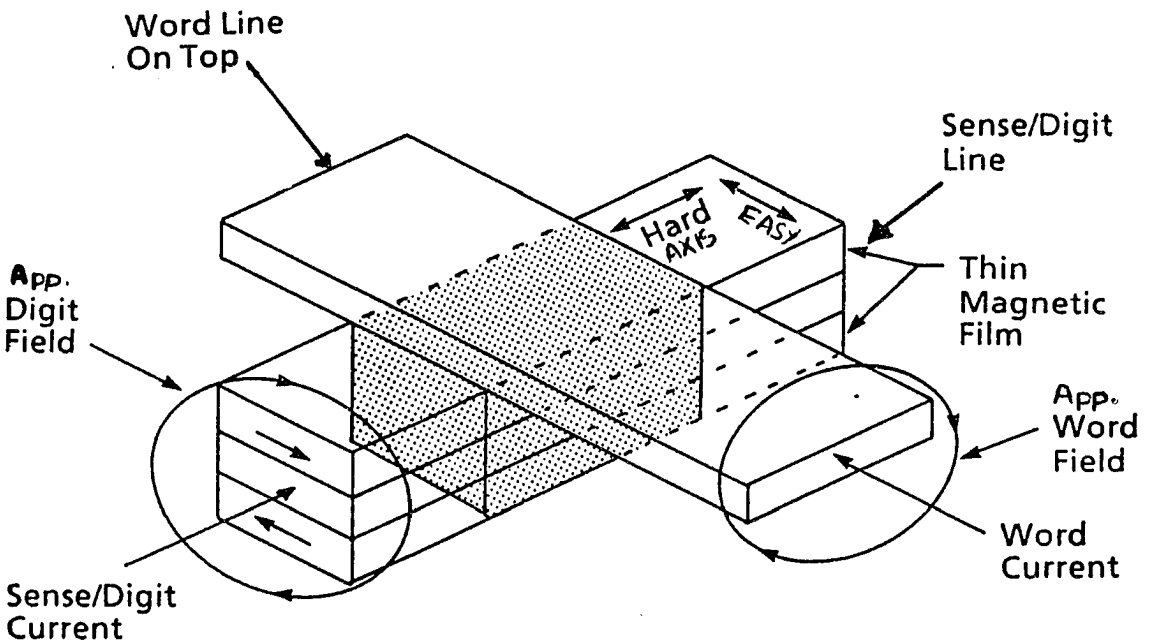


Figure 2.1 Magneto-resistive memory cell structure

When fabricating this cell on a silicon wafer, the semiconductor processing is done up to (not including) metal 1. Then the 150 A thick Ni, Fe, Co double layer and metal 1 is deposited, one after the other (Figure 2.2). Both these layers are then patterned, and the double layer and metal 1 are etched away, leaving the areas where the magneto-resistive elements and the shorting bars (which connects the elements) are going to be present. Now metal 1 over the active areas of the magneto-resistive elements is etched away. Shorting stubs of metal 1 are left between active areas to electrically connect the double layers of elements (fig 2.2). SiO_2 is next deposited. Then metal 2 is deposited, and etched, to form the orthogonal word lines as seen in Figure 2.2. This completes the magneto-resistive cell construction. The masks are made such that a two dimensional array of magneto-resistive cells are formed. This fabrication process requires only one mask beyond a typical CMOS process which is used to selectively etch the double layer. Since the fabrication cost mainly depends on the number of masks these magneto-resistive cells tend to be very low cost compared to a Dynamic RAM process which requires 7-8 masks beyond a typical CMOS process.

2.4 The Magnetic Fields in the Element

In the thin Ni, Fe, Co double layer the magnetization M lies along the easy axis in the absence of an external field as shown in Figure 2.2. The magnetization M has two stable positions along this axis which are the two opposing directions. These two positions correspond to the two states of the digital storage element "1" and "0". Thus each magneto-resistive element stores one bit of information.

When the sense current is applied, a magnetic field called the sense field is produced (Figure 2.2). This field is parallel to the easy axis. When the word current is applied another

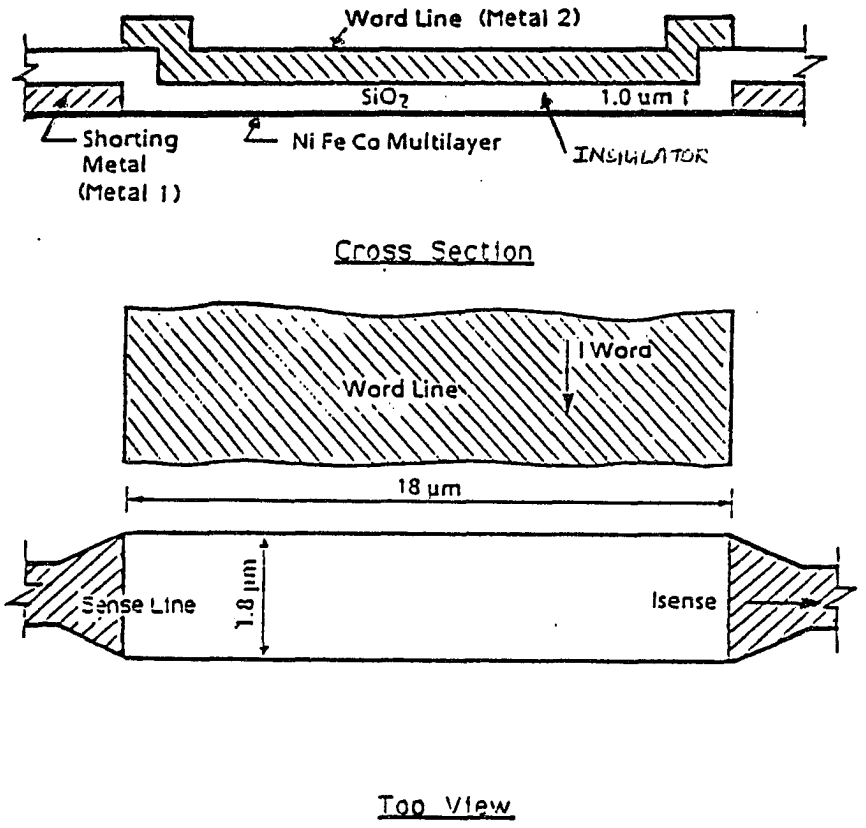


Figure 2.2 Magneto-resistive memory cell cross section and top view

magnetic field is produced. This field is called the word field which is parallel to the hard axis. This word field (Hw) is perpendicular to the magnetization in both layers and causes these magnetizations to rotate in the direction of this field (see Figure 2.3). If a sense current is applied so the resultant sense field is parallel to the original direction of the magnetization, the rotation (caused by Hw) is opposed. If the sense field is antiparallel to the original direction of the magnetization, the rotation is enhanced, favouring switching of the element.

2.5 Read and Write in the Magneto-Resistive Element

The direction of magnetization determines the state of the stored bit. The resistance of the magnetic double layer is a function of the angle (θ) between the magnetization, M, and the sense current . The magneto-resistive coefficient, α, is given below.

$$R = R_0 + \alpha R_0 \text{Cos}^2\theta \quad [6]$$

The magneto-resistive coefficient α is approximately 2% for the current materials used. R_0 is the resistance of the ferromagnetic double layer when no field is applied. This resistance is typically called the anisotropic magneto-resistance. When using these elements, a constant sense current is sent along the hard axis through the double layer. Thus when a word current is present, the magnetization rotates as shown in Figure 2.3, and the value if θ decreases from 90^o. This causes the resistance to increase according to the above formula. Since a constant sense current is flowing through the double layer element, the voltage across the ends of the element (along the sense line shown in Figure 2.1) increases. As mentioned earlier the amount of rotation θ of the magnetization M depends on the direction of the magnetization and the amount of word field applied. Thus the voltage increase depends on the state of the bit ("1" or "0") and the amount of the word current applied. This increase in voltage vs the word current applied is plotted in Figure 2.4 [7].

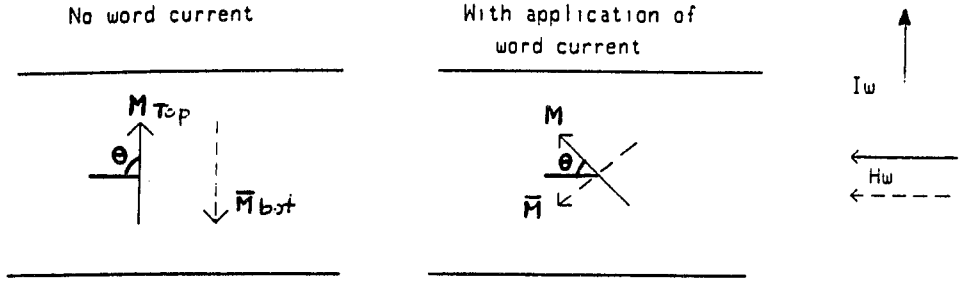


Figure 2.3 Rotation of magnetization in magnetic double layer

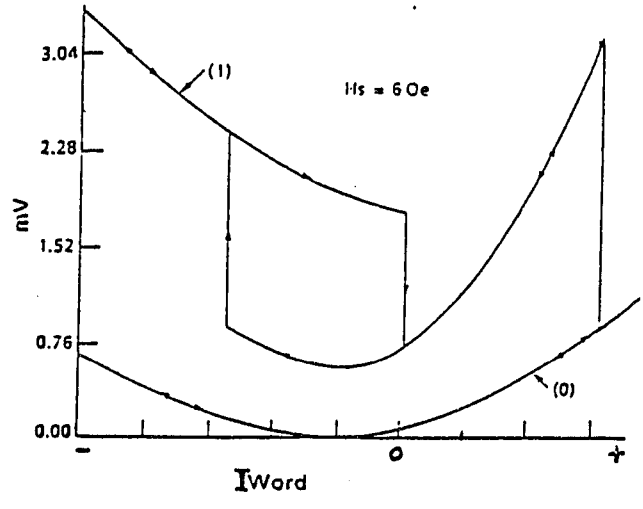


Figure 2.4 Voltage change across the double layer vs word current

2.5.1 Read

When reading a bit, a negative word current is always applied (the positive direction of currents is shown in Figure 2.1). The direction of the applied sense current would determine whether the larger voltage change would correspond to a stored "1" or a Stored "0". The direction usually chosen is the positive direction which gives a larger voltage change for a stored "1". The left part of Figure 2.4 indicates the change in voltage for a negative word current and a positive sense current during a read. The difference in the amount of change in voltage for a stored "0" and "1" can be used to identify the state of the stored bit. This difference voltage for the elements used in the 1Mbit design is 0.8mV. This difference can be detected by comparing the change in voltage from a storage element with the change in voltage from a dummy element which always contain a "0'. It also can be seen from Figure 2.4 that the read process is nondestructive.

2.5.2 Write

To implement a write process, a positive word current is used. The characteristics for a positive word current is shown in the right side of Figure 2.4. Assume the memory cell is in logic state "1" (Figure 2.5a). Then a positive word field (caused by a positive word current) is applied. Assume the sense current is positive which means the sense field is in a direction antiparallel to the magnetization M. The resultant orientation of the rotated magnetization is shown in Figure 2.5a. As the word field is increased the magnetization rotates further and the downwards (for top film) sense field helps this rotation. When the magnetization rotation approaches a switching threshold it suddenly switches to the other stable state shown in Figure 2.5b [8]. Now when the fields are removed the (top layer) magnetization will be downwards corresponding to the sate "0". This switching is shown in

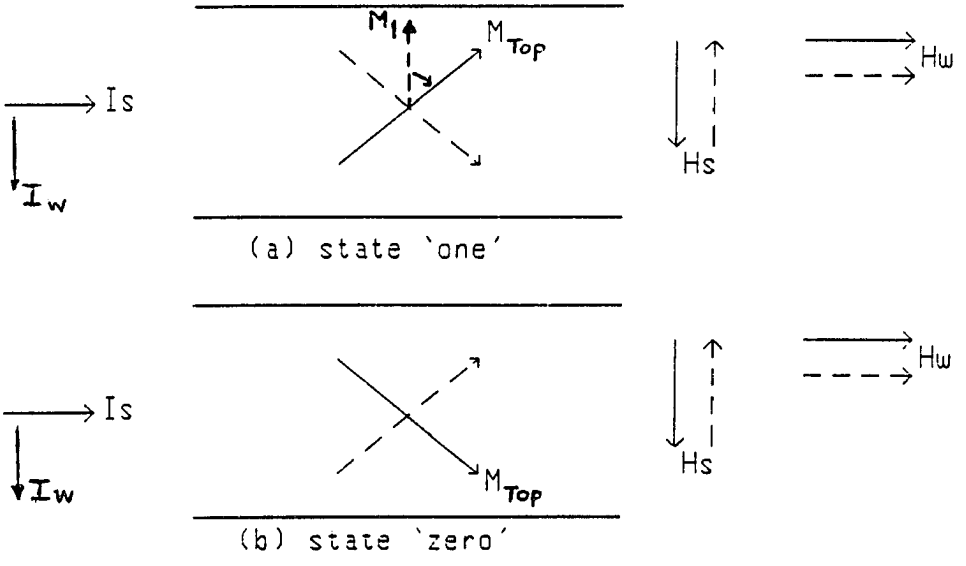


Figure 2.5 Switching from a one to a zero in an element.

Figure 2.4 as a sudden drop in signal level from a "1" to a "0". The bit stays in the "0" state until written back to the "1" state.

To write a "1" the same positive word current is applied and a negative sense current is applied. The same scenario explained above occurs in the reverse direction. Thus to write a bit it is necessary to apply only a positive word current and a sense current in the appropriate direction. A summary of the currents for different modes are given in Table 2.1.

Table 2.1 Current through a element for read and write

Mode	Sense Current	Word Current
Read	positive	negative
Write "zero"	positive	positive
Write "one"	negative	positive

CHAPTER 3. THE MAGNETO-RESISTIVE MEMORY

3.1 The Block Diagram

The magneto-resistive memory contains a magneto-resistive element storage array, column decoder, row decoder, and a sense amplifier. The block diagram is similar to any other semiconductor memory and is shown in Figure 3.1. The memory is organized in eight bit words.The address is 17 bits wide and the data bus is eight bits. As seen in Figure 3.1 part of the address is sent to the column decoder and the rest is sent to the row decoder. A redundancy scheme substitutes spare columns of elements for failed element columns. The column decoder and the row decoder activates the proper column and row thus activating only one element. During a read the signal of the activated element is amplified to logic levels using the sense amplifier. In case of a write the appropriate currents are sent through the accessed element.

3.2 The Magneto-Resistive Element Array

The magneto-resistive elements are organized in a two dimension array as shown in Figure 3.2. Resistors indicate the Ni, Fe, Co double layer in an element. The double layers are connected together in series using Metal 1 shorting bars to form columns, which are the sense lines. The Metal 2 word lines on top of the double layer are connected in series to form rows. There is one sense line per group of 128 sense lines which always store zeros.

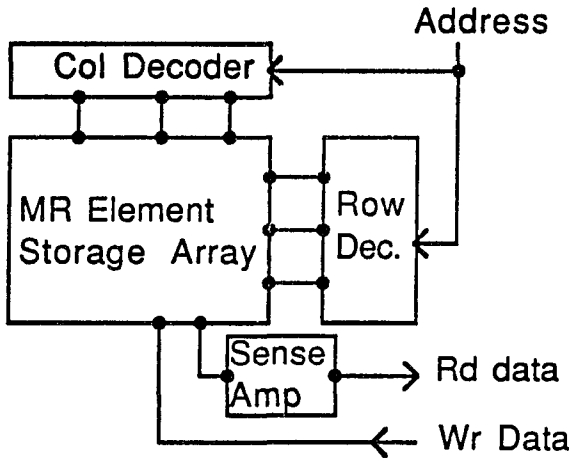


Figure 3.1 Magneto-resistive memory block diagram

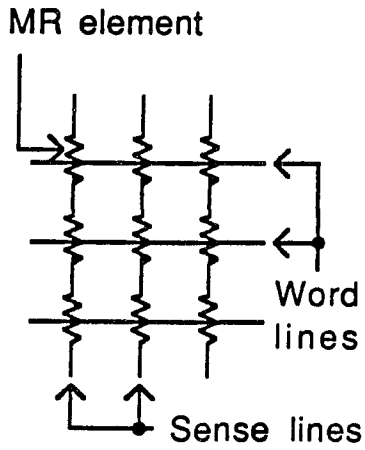


Figure 3.2 Magneto-Resistive memory cell array

This line is called a dummy sense line. A detailed circuit diagram of these sense lines is shown in Figure 3.3. (A modified circuit which uses the same principles, called the balanced sensing scheme is used in the current design and is described in chapter 6. In the circuit shown in Figure 3.3 circuit the currents are supplied by the sense current supply transistors. The direction of the sense current is determined by turning on the proper transistor pair. The current is always sent through the dummy sense line whenever an actual sense line is turned on. Unlike in the actual sense line, the direction of the current in the dummy line is never reversed. In Figure 3.3 the proper sense line (actual) is selected by turning on the central gating transistor T1. The signals of all sense lines are multiplexed to a common line X using the mux transistor T2. Thus whenever a sense line is selected the gating transistor and the mux transistor attached to this line is turned on by the column decoder. Thus during a read the appropriate signal will go on to the common line X.

As explained in chapter 2, during a read process, a voltage change will exist across the the magneto-resistive element. There are two methods to sense this voltage change .

(1) The constant current source method

(2) The voltage mode method.

The constant current source method uses a constant current source to provide the sense current. Here the signal is sensed at one end of the sense line and the entire element voltage change could be obtained for sensing. The voltage source method is shown in Figure 3.3 and this uses a constant voltage source as the power supply to the sense circuit. Here only half of the voltage change appears at the line X (signal cannot be sensed from the end of the sense line). The voltage mode method is used in the 1Mbit design due to lower thermal noise [9]. The voltage change appearing at line X varies depending on whether the accessed element has a stored zero or a stored one. One obvious method to detect the difference in voltage change is to compare the voltage of line X against a constant voltage reference.

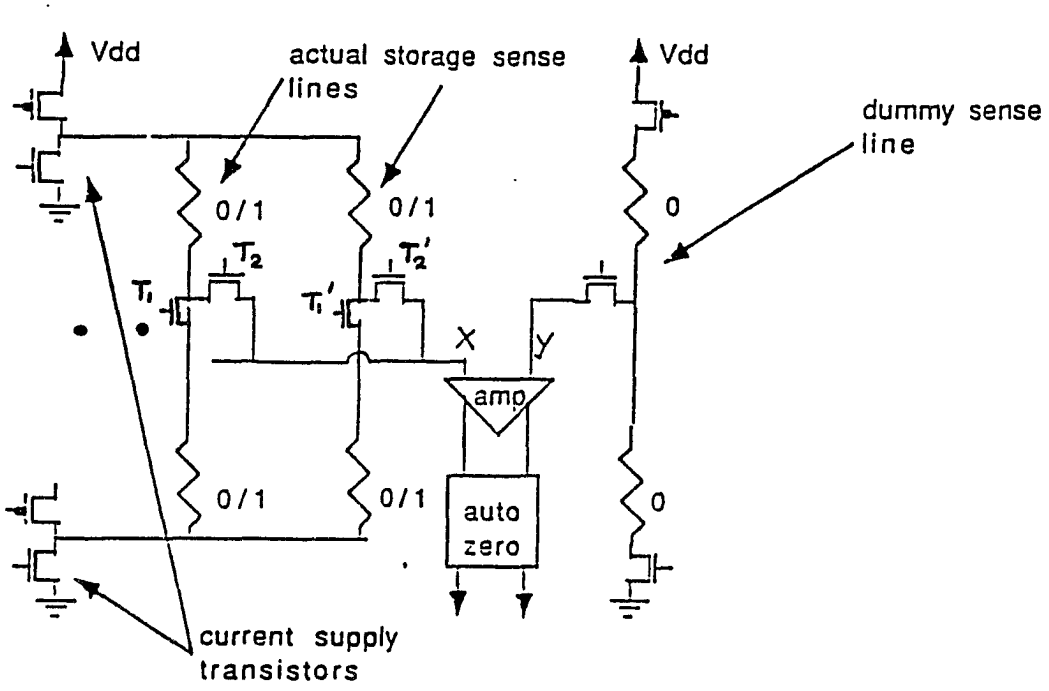


Figure 3.3 Sense lines and dummy line in the element array

However, during the read process the magneto-resistive element heats up considerably. Thus the resistance of the elements changes rapidly making the voltage on line X change. Thus using a constant voltage reference is not possible. To avoid this problem a dummy line is used [9] which would experience approximately the same thermal characteristics. The center point Y of this dummy line is compared against the line X to detect the difference voltage. This difference voltage is the actual signal used to generate logic levels and is shown in Figure 3.4. (The stored zero voltage is moved up due to auto-zeroing which is explained in chapter 7.) The magnitude of this signal is 0.4 mv and is detected using a differential preamplifier. The preamplifier amplifies only the difference signal and rejects the common mode signals.

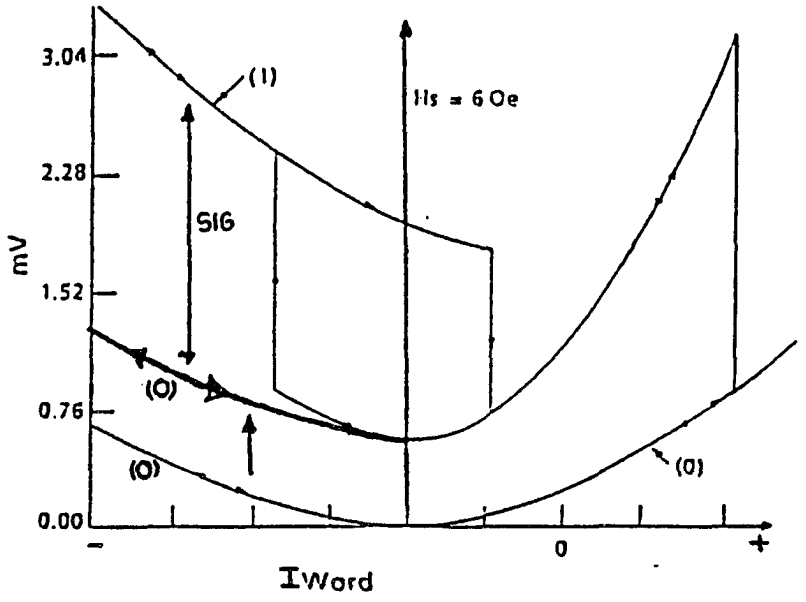


Figure 3.4 Voltage change across element vs word current.
Useful signal is denoted by "SIG".

CHAPTER 4. PROBLEMS IN SENSING

There are many problems to be solved when sensing the signal from a magneto-resistive element. The main reason for these problems is the very low signal produced by the magneto-resistive elements. These elements have a size of 10μm x 2.8 μm and produce a difference signal (when used with dummy elements) of 0.4 mV. Although an increase in element size would produce a larger signal, in order to achieve high density the size is kept small. The subtopics below describe the problems encountered in detail.

4.1 Change in Element Resistance due to Heating

This is the problem caused by the heating of the sense lines when a current flows through them. This heating causes the resistance of the element to change thus causing the voltage at the center of the sense line to change. A dummy sense line is used to solve this problem. This problem was described in detail in chapter 3.

4.2 Mismatch Between the Sense Lines and the Dummy Line due to Process Variations

The sense lines are laid out in columns which span across the chip. In any fabrication process the process parameters change across the wafer. Due to this change the resistance of the double layer will change across the chip, causing a mismatch in the resistance of the

sense lines and the dummy line. Since there is only one dummy line for a group of 128 sense lines, when accessing a sense line further away from the dummy line this mismatch in resistance could be very high. This mismatch in resistance could cause the voltage at the center points of the dummy line and an accessed sense line to differ even when there is no element signal present. The resulting voltage difference could be as high as 50mV. The difference signal from the accessed magneto-resistive element and the dummy element also appears across the same two points as a voltage difference of 0.4 mV. Thus the 50mV voltage difference could easily mask the signal. An auto-zero scheme is used to solve this problem and is described in chapter 7.

4.3 Noise

The sense lines which contain the elements have an ohmic resistance which could cause noise problems. The sheet resistance of the Ni, Fe, Co double layer in an element is 10 Ω/sq. Thus for a 7μm x 1.4μm double layer the resistance should be 50Ω. When the resistance of the shorting bar and the other contacts are added the resistance of a complete element along the sense line is 55Ω. Sixteen of such elements are put in series to form a sense line. The equivalent noise resistance of such a sense line together with a dummy line, including mux, switching, and current supply transistors is 1100Ω [9]. The noise generated by this equivalent resistance is calculated using the following equation.

$Vn^2 = 4KTR\Delta f$

Vn = RMS noise voltage generated

K = Boltzman constant

T = Temperature of the sense array

R = Equivalent noise resistance

Δf = The equivalent noise bandwidth of the sensing system

From this equation it could be easily observed that the amount of noise is proportional to the bandwidth of the sensing scheme. Thus to keep the amount of noise generated far below the signal generated a bandwidth limiter is used. This is described in detail in chapter 8.

4.4 Differences in Heating Time Constants of Elements

When using a dummy line (as explained in chapter 3) for differential sensing, there exists a problem due to the difference between the heating time constants of the dummy line elements and actual sense line elements. In the sensing scheme the offset, due to a resistance mismatch (from process parameter variations across the chip) between the dummy line and the sense line, appears as difference signal between the center of the dummy line and the sense line. In the sensing scheme this offset is removed first by the auto-zero process. Then the signal from the elements is generated and it appears across the same center points. However due to the different thermal time constants of the dummy line and sense line the heating rates of these two lines vary. Thus during the time between the removal of the offset and detection of the signal, the temperature between the two lines can vary causing further resistance mismatch, which is not removed by the auto-zero process. This mismatch generates another offset voltage which could completely mask the element signal.

This problem is further aggravated by the fact that the dummy is always activated and a given sense line is rarely activated. Random nature of the memory addresses causes different sense lines to be activated at different times, which results in a given sense line being activated very infrequently. This pattern causes the dummy line to be at a higher temperature than the sense lines. This temperature difference gives rise to a significant difference in the heating rates for the two lines. To solve this problem a given element is

sampled twice, first as a zero and then as a one. The second sample value is subtracted from the first sample value eliminating the common error due to above problem. This method is explained in detail in chapter 9.

CHAPTER 5. OVERVIEW OF THE SENSING SCHEME

Once the problems in sensing the element signal are identified, a sensing scheme can be developed to eliminate these problems and generate a logic output. The sensing scheme developed for this 1Mbit memory has a number of stages, with each stage taking care of one type of problem.This chapter gives a brief overview of the entire sensing scheme and the following chapters describes each stage in detail.

Figure 5.1 gives a block diagram of the sensing scheme showing the different stages. The magneto-resistive element array, with a dummy line, generates the required difference signal. A balanced magneto-resistive element array is used for better performance. This difference signal is amplified using a low noise differential preamplifier called "Diffamp1". This amplifier has a gain of 10. Then the signal from the preamplifier is fed into a two stage auto-zero circuit to remove the offset due to the mismatch between the sense line and dummy line resistance caused by parameter variations across the chip. The preamplification is done before auto-zero, to reduce the clock feed-through effects of the auto-zero, and to reduce the effect of the thermal noise produced by the switching transistors in the auto-zero.

In the two stage auto-zero, the two stages are isolated from each other using a differential amplifier named "Diffamp2". This amplifier has a gain of 10. After the second auto-zero stage the differential signal is converted to a single ended signal using a differential amplifier named "Diffamp3" (see Figure 5.1). This amplifier has a gain of 5. At this point the 0.4 mV signal is amplified to 200mV. The bandwidth of the stages through

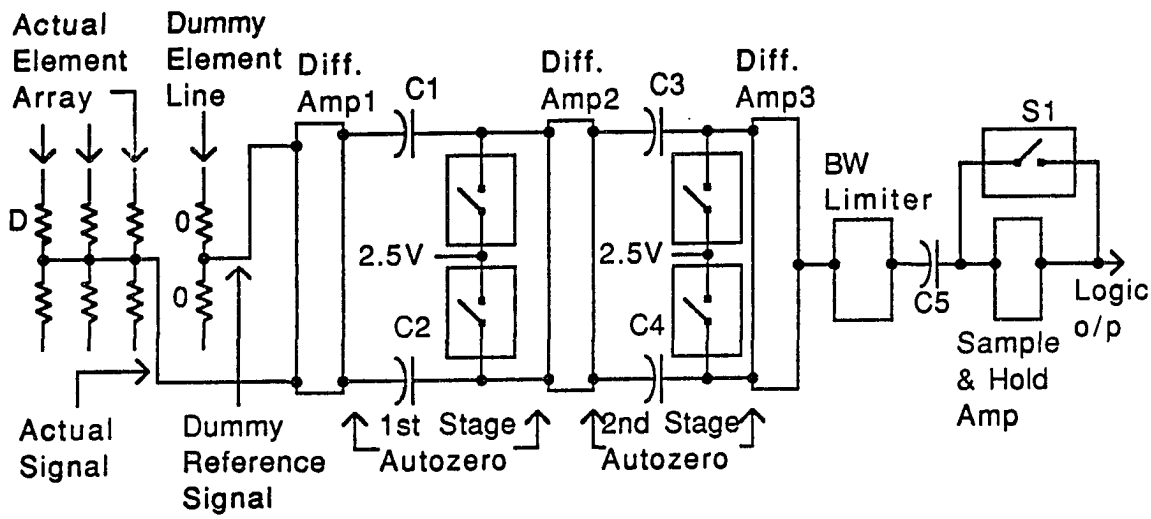


Figure 5.1 Block diagram of sensing scheme

"Diffamp3" is high, during the amplification of the signal. To limit the bandwidth, in order to reduce the noise generated by the magneto-resistive element array,a bandwidth limiter is used.

After limiting the bandwidth the signal is fed into a sample and hold stage to remove the offset due to the differences in the heating rates of elements. To remove this offset the accessed bit is read twice (first as a zero and next as a one). This stage then compares the two values to remove the offset. This stage also amplifies the signal up to logic levels.

When designing each stage, in additional to its functionality, many other factors need to considered. These factors are the noise generated, delay, area consumed, complexity and sensitivity to the following: temperature, induced glitches, process variations in gate threshold voltage and geometric tolerances in fabrication. The importance of each factor varies depending on the purpose each stage is used for.

CHAPTER 6. BALANCED SENSING

In earlier chapters the magneto-resistive element array shown in Figure 6.1 was used to explain problems in sensing. This was the old scheme and it had some serious drawbacks due to glitches and the large voltage offset at the preamplifier ("Diffamp1") inputs. The large voltage offset was caused by the mismatch of resistance between the sense lines the dummy line.

6.1 Problems of the Old Scheme

6.1.1 Glitch problem

Glitches occur at the center of the sense lines due to power supply voltage glitches, and due to glitches in other voltage varying lines, which are capacitively and inductively coupled to the sense lines. Since a large number of actual storage sense lines are multiplexed to one line, due to drain capacitance of mux transistors, the input line to the amp has a large charging time constant associated with it. The RC model for the scheme given in Figure 6.1 is shown in Figure 6.2. However the input to the amp from the dummy line has a very small time constant since only one drain capacitance exists. The above glitches at the center of the actual sense lines and at the dummy sense lines are approximately same in magnitude.However due to the different time constants, the amplitude of glitches at each amplifier input can vary considerably at a given moment even if the signal is band limited.

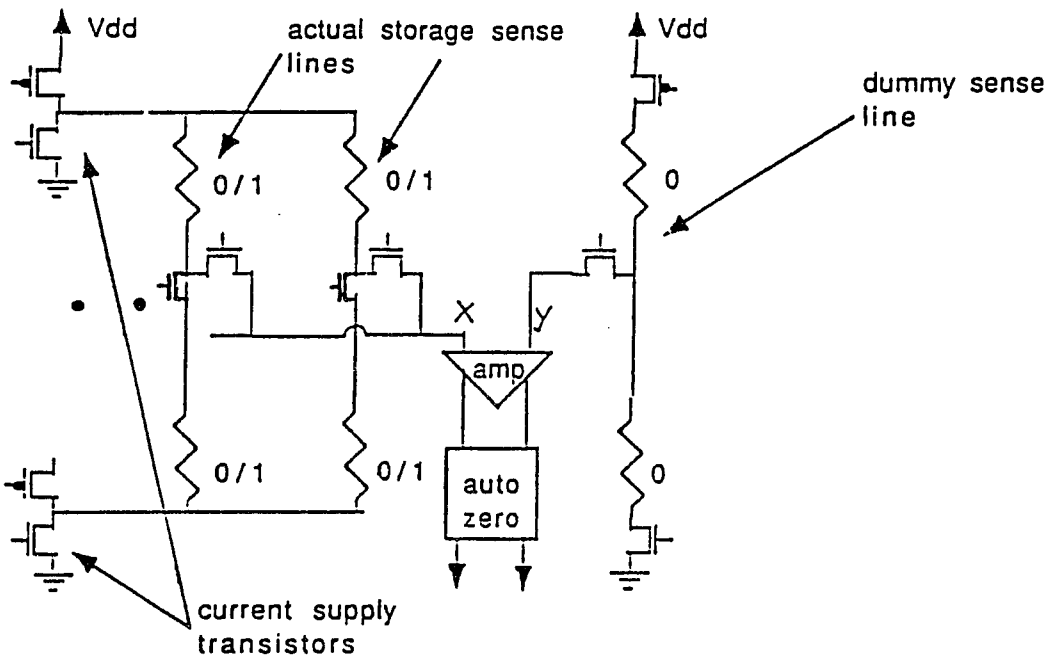


Figure 6.1 Sense lines and dummy lines in the element array (not implemented)

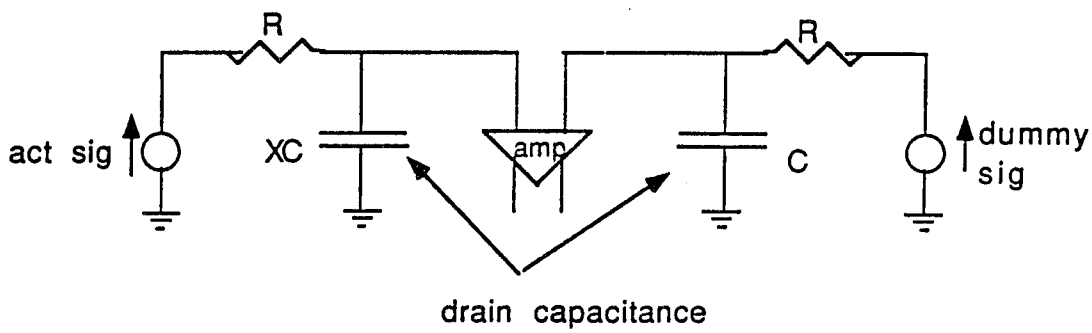


Figure 6.2 RC model of figure 6.1

Thus the glitches can cause a difference signal across the inputs, which is comparable to the signal required (0.4mV). Therefore extensive precautions have to be taken to reduce the sources of glitches and to provide a very high roll-off bandwidth limiter. This would cause an increase in area and complexity of the circuit.

6.1.2 Charging Problem

When the current is switched through the elements, due to different RC time constants the charging curves at the inputs of amplifier can vary considerably. Thus to get the same voltage at the input of the amplifier the system has to wait for a very long time before generating the required signal of 0.4mV.

6.1.3 Offset Problem

The resistances of the current supply transistors can vary due to process variations even if they are placed at close proximity. This variation would cause an offset voltage at the input of the amplifier, which adds to the offset voltage caused by the difference in the storage element and dummy element resistances. Since the required signal is superimposed on this offset the linear region of the amplifier must be increased and the auto-zero must work over a wider voltage range.

6.2 New Scheme

The new scheme eliminates the above three problems, by dividing the number of storage sense lines (array) into two groups and having the current supply transistors common to dummy and storage sense lines. The signals from the sense lines of each half are

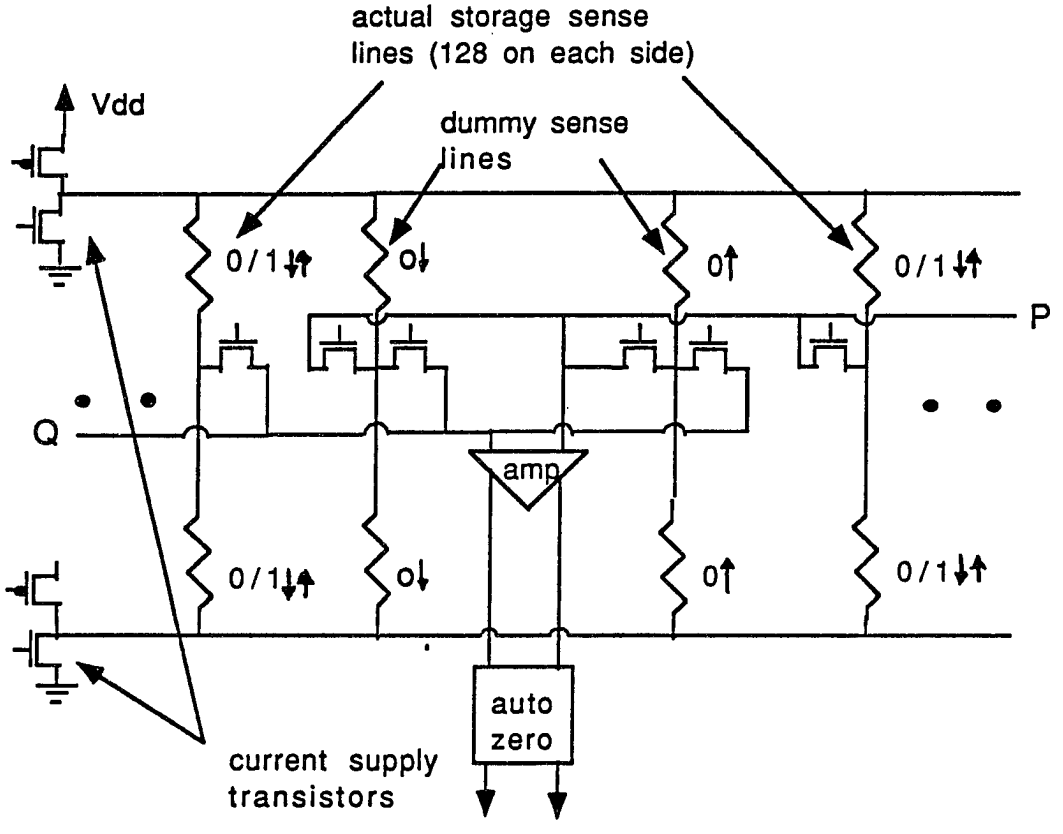


Figure 6.3 New Scheme for sense lines and dummy lines in element array

multiplexed separately to two separate lines as shown in Figure 6.3. These two separate lines are fed to a differential amplifier. In this scheme when sensing, the dummy sense line signal is connected to the left common line Q (Figure 3.3) if the sensing bit is on the right half of the array, and vice versa. This makes the stray capacitance on input to the amplifier, due to the mux transistor drains equal. Thus the RC time constant, of each input of the amplifier, is equal and it makes the amplitude of the glitches, at each input, also the same. Since glitches are common mode to the amplifier they will be rejected. Also the charging problem will be solved due to identical time constants providing identical charging curves.

In this scheme there are two dummy lines, and the left dummy line always carries current in the downward direction and the right dummy line carries current in the upward direction. The current-supply transistors of the dummy and storage sense lines, in an earlier scheme can be merged. Thus the offset due to variations in supply transistors will not exist. In addition, unlike the earlier scheme, the noise generated by these transistors becomes common mode at the amplifier input, thus increasing the signal to noise ratio.

This new scheme would increase the area of the sense array by 1% due to the extra dummy line. However, alleviation of the above discussed problems would result in a much simpler sense amplifier design, a scheme which would be tolerant to glitches and parasitics and result in lesser overall area.

CHAPTER 7. AUTO-ZERO

7.1 Principle of Operation

Due to process parameter variation across the chip a mismatch between the sense lines and the dummy line occurs (as described in section 4.2). This mismatch produces an unwanted differential offset voltage across the midpoints of the two lines. The useful signal generated from these two lines also appears across the same two midpoints. Since the useful signal (0.4mV) is much smaller then the unwanted offset voltage (50mV), the useful signal can easily be masked by the offset voltage. To solve this problem auto-zeroing is done. In auto-zeroing the offset is removed before the signal is generated.

7.2 Signal to Noise Ratio Calculation for Auto-Zero

The thermal noise generated in the magneto resistive array and the sensing scheme is random. Thus this noise causes soft errors if the magnitude of a random noise pulse is comparable to the useful signal. To minimize these soft errors the probability of this occurrence must be minimized. This is done by reducing the RMS (root mean square) value of the thermal noise voltage with respect to the useful signal voltage (i.e. the signal to noise ratio is increased). It is estimated that to have an acceptable soft error rate a signal to noise ratio of 20/1 is required.

The logic output is generated from the useful signal in the following sequence.

1. Perform the auto-zero process to remove the offset due to process variations.
2. Generate the useful signal and sample it.
3. Reverse the sense current and perform auto-zero again to remove the offset due to process variations.
4. Generate the useful signal and compare it with the previous sample to get logic output.

Each of the above steps generate an almost equal amount of thermal noise.

If the noise generated by each step is = N mV

The total noise generated by all four steps = $(N^2+N^2+N^2+N^2)^{0.5}$

= 2N

(Since the noise is random a RMS addition must be done.)

Thus the signal to noise ratio of each step = 2 x Signal to noise ratio of the entire system

= 2 x 20/1 = 40/1

Therefore the signal to noise ratio of the auto-zero process = 40/1

7.3 Single Stage Auto-Zero Scheme

In previously used auto-zero schemes [4] only a single stage was used.This is shown in Figure 7.1.

7.3.1 Principle of Operation

In this scheme the unwanted offset voltage due to a resistance mismatch (due to process parameter variations) appear between points X and Y (Figure 7.1). To remove this offset, the first step is to send only the sense current through the dummy line and the

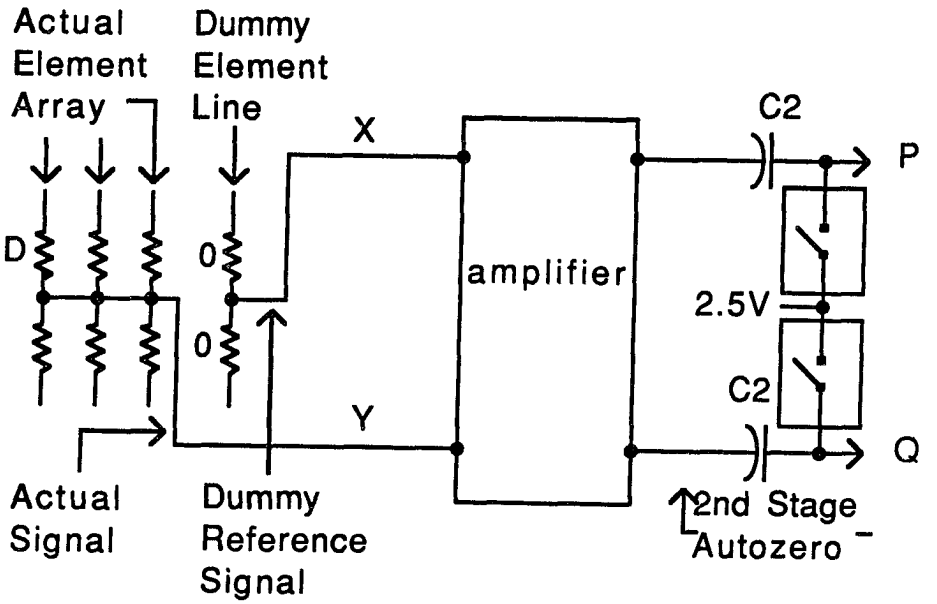


Figure 7.1 Previous single stage auto-zero

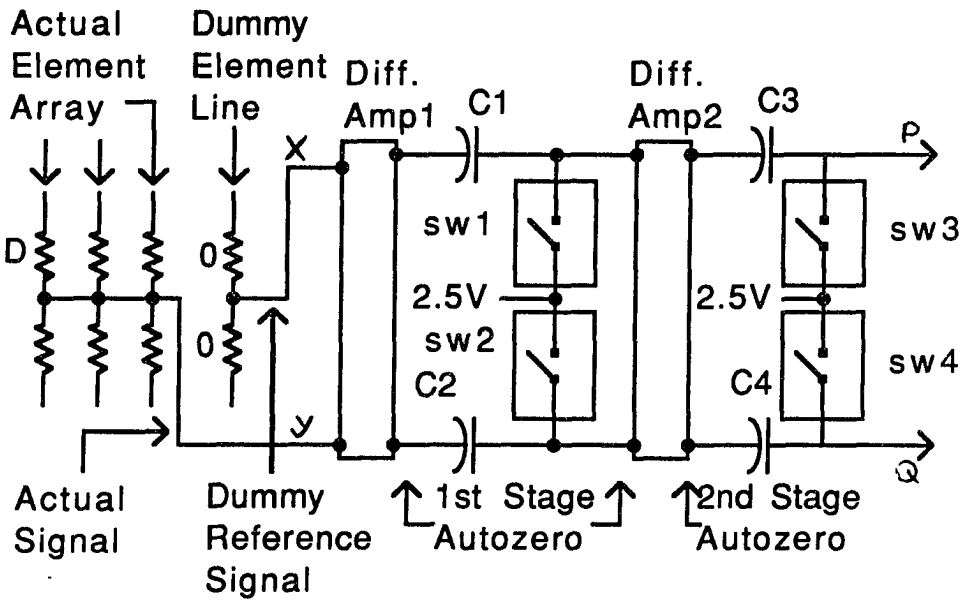


Figure 7.2 Two stage auto-zero

selected actual sense line. Since the word current is not turned on no useful signal is generated. However at this instant the voltage offset appears across the points X and Y. Now the transistor switches

and SW2 are turned on. This charges capacitors C1 and C2 to the voltage offset between X and Y. After the charging process the points P and Q will be at the same voltage with no offset between them. Next the switches

and SW2 are turned off and the word current is applied to the dummy line and the sense line elements. After the switches are turned off any voltage change that occurs on the points X and Y will also occur on the points P and Q. When the word current is applied the useful difference signal appears across the points X and Y and is transmitted to points P and Q unaltered. Thus the points P and Q have the useful signal but have no voltage offset.

7.3.2 Drawbacks of Single Stage Auto-Zero Scheme

This Scheme has a problem due to the thermal noise generated by the element resistances. To remove this voltage offset quickly the time constant of the auto-zero process, which is the RC product (product of the resistance of the switch

and the capacitance of the capacitor C1), must be small. However this small time constant causes a large amount of noise to be generated by the element array. This noise could easily mask the useful signal. On the other hand if a large time constant is used, the charging time of the capacitors C1 and C2 would be very large. This would make the auto-zero time large.

7.4 Two Stage Auto-Zero Scheme

To solve this problem the auto-zero is done in two stages. Figure 7.2 shows this scheme. The two stages are called the first auto-zero stage and the second auto-zero stage.

The first auto-zero stage has a very small time constant. The time constant is made small by making the resistances of the switching transistors very small. The auto-zero process operates in the following manner.

The switches of the first auto-zero stage is turned on first while only the sense current is sent through the dummy and the actual sense line. This removes the voltage offset (where the magnitude is 100 times the useful signal) due to resistance mismatch quickly. Since the time constant of this stage is small, a large amount of noise (comparable to the useful signal) is generated. When these switches are turned off the switches of the second auto-zero stage are turned on. This is also done in the absence of the word current. At this point in time the output of the first auto-zero stage will be only the noise generated by the first auto-zero stage. Since the second auto-zero has a high time constant the noise generated by this stage is very much less. The noise voltage generated by the first auto-zero stage is removed by the second auto-zero by charging the capacitors C3 and C4 to this voltage. The charging time is not high due to the small value of the voltage to be removed. After the charging process the switches of the second auto-zero stage are open and the word current is turned on. Now the useful signal will appear at the output of the second auto-zero stage having the voltage offset due to the resistance mismatch removed. This two stage scheme is faster due to the fast removal of offset while finally producing very little noise.

A differential amplifier (diffamp1) is used to amplify the signal before auto-zero and a differential amplifier (diffamp2) is used to isolate the two auto-zero stages (see Figure 7.2). Each amplifier has a gain of 10.

7.4.1 Diffamp1

Diffamp1 is shown in Figure 7.3 and is used to amplify the differential signal from the magneto resistive array before auto-zeroing. This must be a very low noise amplifier since the input signal is only 0.4mV. It is estimated a noise resistance of 250Ω is ideal [9]. To obtain this low noise resistance the input transistors of the diffamp1 must have a size of at least 200/1.6 [9]. These large transistors have a large transconductance.

The differential gain = - Load resistance x Transconductance.

It is estimated for the gain to be 10 the load resistance must be 4kΩ [9]. Implementation of this resistor using diffusion or tub resistors is not practical due to the large diffusion capacitance associated with them. Thus it is best to use permalloy (Ni,Fe,Co multilayer) resistors which have a sheet resistance of 10Ω/sq. Therefore, the output impedance of Diffamp1 is 4kΩ.

7.4.2 First Stage Auto-Zero

This stage is shown in Figure 7.3 and is used to remove the voltage offset due to process parameter variations and the voltage offset of diffamp1. It is estimated that the maximum value of these offsets is 50mV each [9]. Since the gain of the diffamp1 is 10 the total offset needed to be removed by auto-zero is 1V.

In the first stage auto-zero the resistance of the switching transistors T1 and T2 (of size 5/2.5) is 2kΩ [9]. This 2kΩ resistance, the element and diffamp1 noise resistance, along with the Capacitors (C_1 + C_2) of value 0.3 pF, produce a noise voltage of 0.43mV [9]. This voltage will appear at the output of the first auto-zero stage. The charging time of the first auto-zero stage is estimated to be 60ns. The criteria used for this is the mismatch of

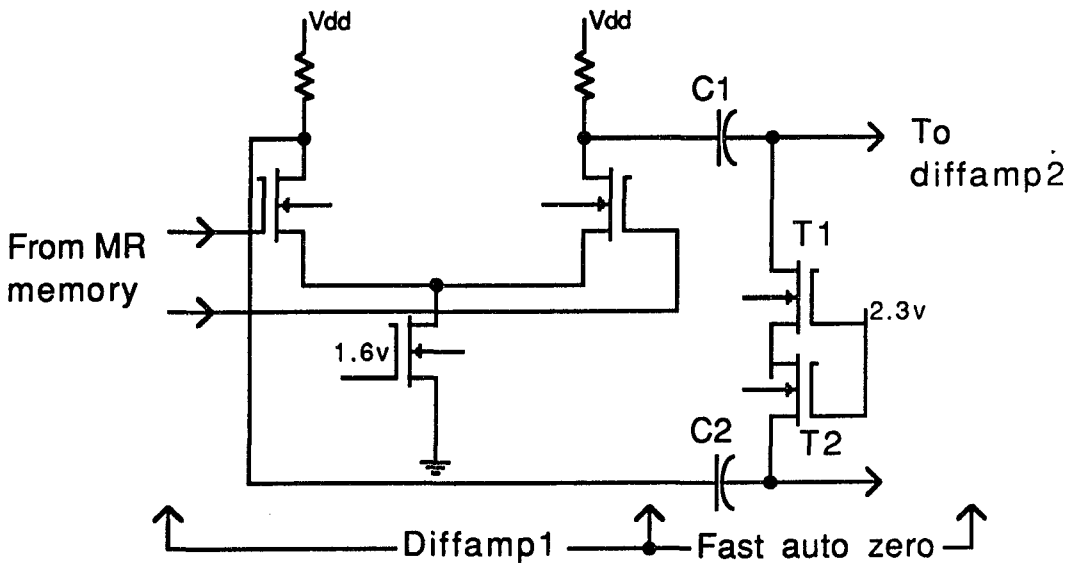


Figure 7.3 Diffamp1 and first auto-zero

the time constants of the two capacitors. After the first auto-zero is complete the voltage at the output of this stage will be a 0.43mV noise voltage.

7.4.3 Diffamp2

The Diffamp2 is shown in Figure 7.4 and is used to isolate the first auto-zero stage from the second auto-zero stage and to further amplify the signal. The useful signal into the diffamp2 is 4mV. To keep the noise to a minimum the signal to noise ratio for the diffamp2 is fixed at 120/1.

The maximum noise that can be generated by diffamp2 is $= 4/120.$

$= [(2/3gm)KT\Delta f]^{0.5}$

Thus transconductance of the input transistors of diffamp2: $gm > 1.23 \times 10^{-5}$ A/V

If the W/L = 9.4/1.6 for transistors 1 and 2 and if the total current through diffamp2 is 0.05mA, the following equation can be used to calculate the gm for these transistors.

$gm = (\beta Ids)^{0.5}$

$= 1 \times 10\text{-}4$ A/V

This value is well above the minimum of 1.23×10^{-5}.

The Gain of the diffamp2 has to be G = 10

Since gain $G = gm \times R1$

Then $R1 = 100k\Omega$

To get the very high resistance of 100K a permalloy resistor, a diffusion resistor, or a saturated load cannot be used due to the large size required. An ohmic transistor with a very high gate length is used for this purpose. The gate of this transistor is tied to Vdd. From the following equation the size of this transistor can be estimated.

$$1/R1 = \beta 1[Vgs - Vt]$$

The size of this transistor is T1 = 2.8/29

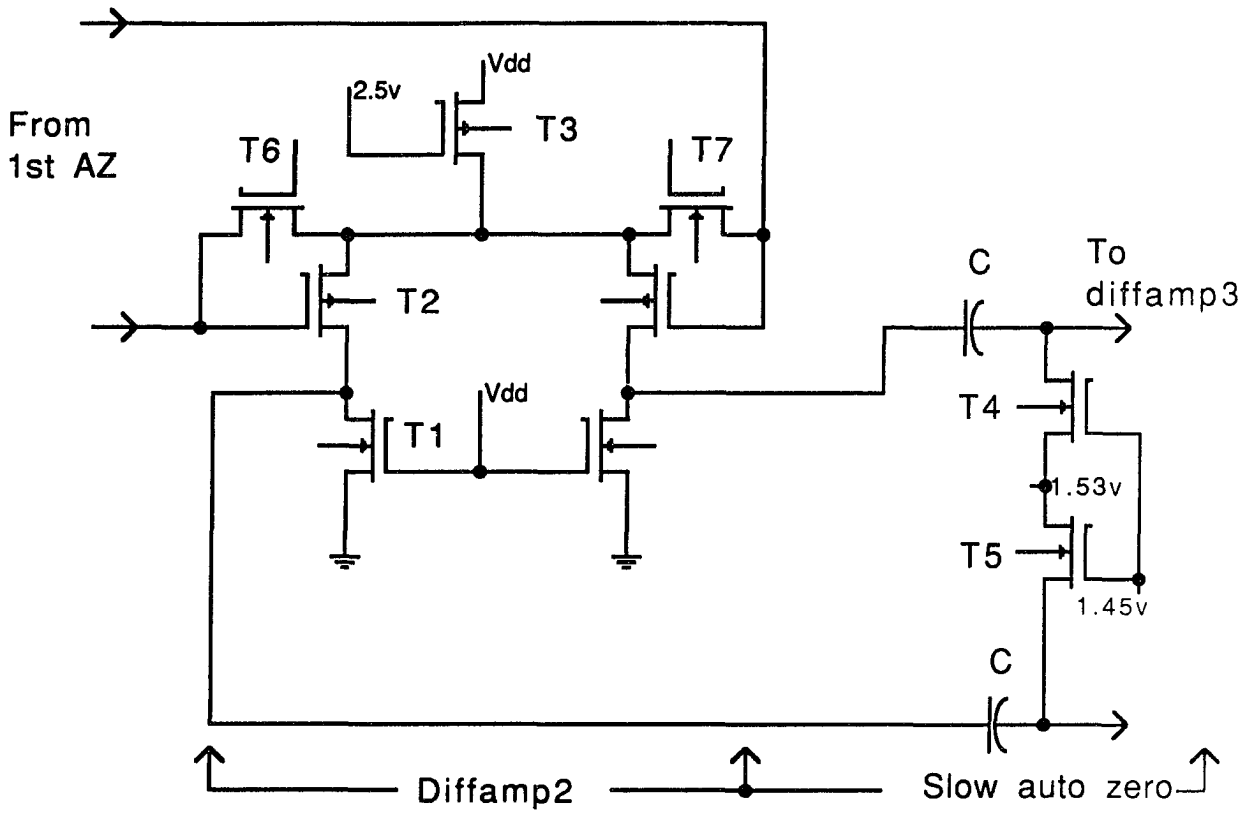


Figure 7.4 Diffamp2 and second auto-zero

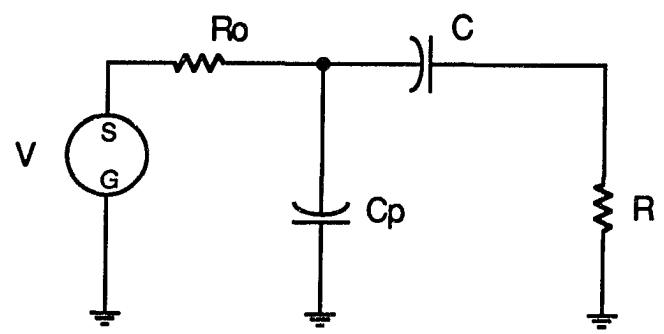


Figure 7.5 Equivalent circuit for diffamp2 output and second auto-zero

To keep T3 in saturation while allowing a common mode input voltage swing of 0.3mV the value of Vr is selected to be 2.55V. Using the following equation the size of this transistor can be estimated.

$$Ids = (\beta/2)[Vgs - Vt]^{0.5}$$

Thus the size of T3 = 5.7/1.6

The transistor pairs T6 and T7 are used to reduce the offset of diffamp2. The offset of this amplifier is mainly caused by the mismatch of the threshold voltages of the input and the load transistor pairs. The offset is estimated to be 50mV and is reduced to 10mV. For this to take place, the transistors T6 and T7 must be kept on for 20nS immediately after the first auto-zero.This offset of 10mV is not critical since it is reduced to 1mV by the second auto-zero stage and the remaining 1mV is cancelled by the sample and hold stage.

This amplifier was tested for following parameter variations.

Temperature variation	= 25 - 65 C
Variation in reference voltage Vr	= + 50mV
Variation in Vt	= + 50mV
Variation in line width	= + 0.1μm
Change in common mode input level	= + 50mV
The rage of gain for these variations	= 8 - 10
The bias output voltage of the amplifier	= 1.5V
The output impedance of the amplifier	= R1
	= 100KΩ
Simulation indicate the bandwidth of amp.	= 15Mhz

7.4.4 Second Auto-Zero Stage

The second auto-zero stage is shown in Figure 7.4. It is used to remove the noise generated by the first auto-zero stage. This stage must have sufficiently low bandwidth to keep the noise generated by this stage very low.

The signal to noise ratio of the first auto-zero stage was estimated to be 40/1 in section 7.2. This signal to noise ratio is mainly determined by the amount of noise generated by the second auto-zero. The bandwidth required to give this signal to noise ratio is determined using the following equation.

Noise generated = $(4KTR\Delta f)^{0.5}$

R = noise resistance of the magneto resistive element array and diffamp1

= 1100Ω

Δf = noise bandwidth required

Since the maximum noise allowed = 0.4mv/ 40

The noise bandwidth required = 5 Mhz

The small signal equivalent circuit for the combination of the diffamp2 and the second auto-zero is shown in Figure 7.5. The resistor Ro is the output impedance of the diffamp2, resistor R is the resistance of the switching transistors T4 and T3, capacitor C is the capacitance of the auto-zero capacitance, and capacitor Cp is the parasitic capacitance of the capacitor C. When the switching transistors T4 and T5 are on, the combination of the diffamp2 and the second auto-zero is an RC lowpass filter with a first order roll off.

For a first order low pass filter the 3dB bandwidth = Effective noise bandwidth/ 1.57.

= 3.2 Mhz

To have a 3.2 Mhz bandwidth the capacitors C3 and C4 are selected to be 0.3pF, and the sum of the resistors Ro and R must be 161KΩ. Since the value of Ro is 100kΩ the value of

R (the resistance of the switching transistors T4 and T5) must be 61kΩ. Simulations indicate that to achieve this resistance the size of these transistors must be 2/3.

The resistors Ro and R also generate noise which must be accounted for. For the equivalent circuit in Figure 7.5 the noise generated by R and Ro is calculated below.

Noise by R $= (4KT/C)^{0.5}$

$= 0.12mV$

Noise by Ro $= (4KT/C)^{0.5} \times R/(Ro+R)$

$= 0.07mV$

(Total noise on one side due to R and Ro) ^{2} = (noise by R) ^{2} + (noise by Ro) ^{2}

$= 0.0225$

Total differential noise due to R and Ro $= 0.21mV$

(offset after second auto-zero) ^{2} = (noise due to R and Ro) ^{2} + (offset remaining after removal of first auto-zero noise) ^{2}

The offset that could be tolerated after the second auto-zero is selected such that the signal to noise ratio of this offset is 100/1. Thus the offset after the second auto-zero is 40mV/100. Substituting this in the above equation results in

$(0.4)^2 = (0.21)^2$ + (offset remaining after removal of first auto-zero noise) ^{2}

Therefore, after removal of the first auto-zero noise the offset is 0.33mV.
Thus the noise produced by the first auto-zero must be reduced 0.33mV by the second auto-zero process.

The noise produced by the first auto-zero after amplification = 0.47mV x Gain of diffamp2

$= 4.7mV$

If the second auto-zero time is t, the remaining offset after removal of noise is given by the following equation.

$V = Vo \exp(-t / T)$

Vo = Noise to be reduced

= 4.7mV

T = Time constant of second auto-zero

= C(Ro + R)

= 48nS

Thus from the above equation t = 144ns. Therefore, the second auto-zero process must take 144ns.

CHAPTER 8 DIFFERENTIAL TO SINGLE CONVERTER AND BANDWIDTH LIMITER

8.1 Differential to Single Converter

This stage converts the differential signal to a single ended signal. For this purpose a differential amplifier is used and is named diffamp3. This amplifier is the same amplifier used for diffamp2 except the output is taken only from one side as shown in Figure 8.1. Since the output is taken only from one side, the gain is half of the differential gain. Thus the gain of diffamp3 is 5. A current mirror type of differential to single converter was not used due to the difficulty in applying negative feedback for both inputs. This is needed to reduce its very high gain (gain must be reduced to avoid saturating the amplifier).

The performance characteristics of diffamp3 are the same as diffamp2. The input offset of 50mV is reduced to 10mV by using feedback transistors. This offset is not critical since it is canceled out by the process of comparison of two samples in the sample and hold stage.

8.2 Bandwidth Limiter

Thermal noise is generated in four instances as explained in section 7.2. The noise generated by the auto-zero steps are determined by the low bandwidth of the second auto-zero stage. The noise generated by the the sampling and comparison steps are controlled by

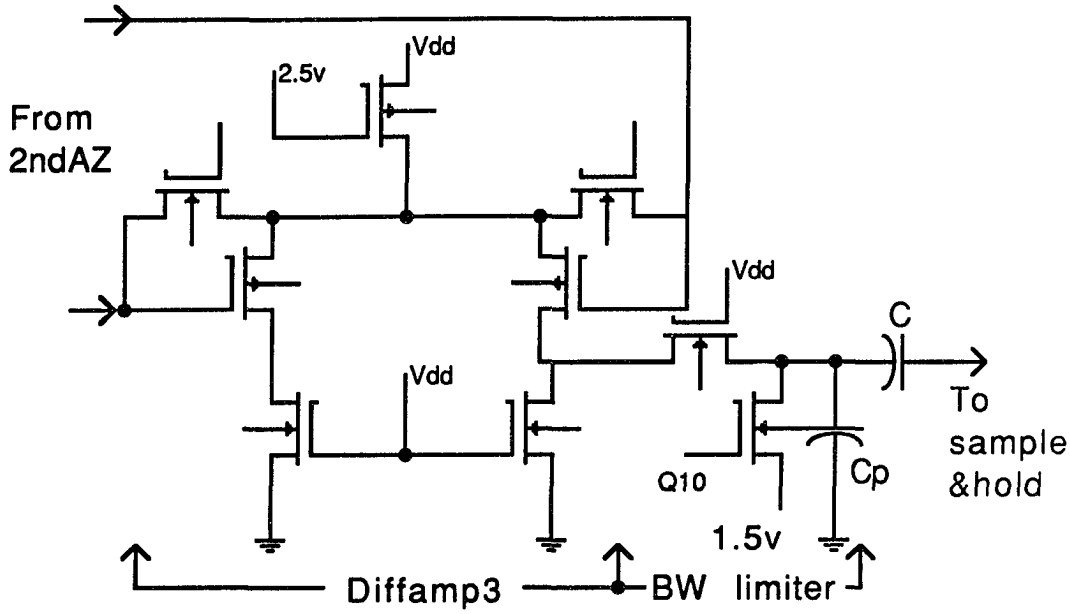


Figure 8.1 Diffamp3 and bandwith limiter

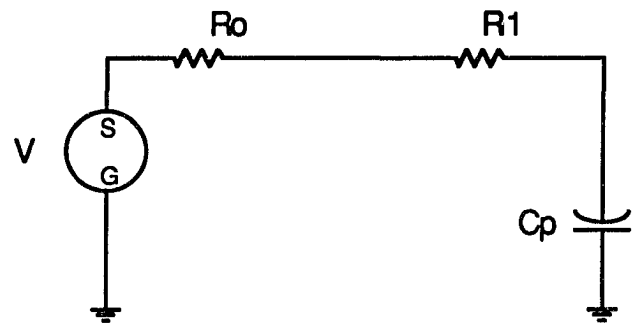


Figure 8.2 Equivalent circuit for diffamp3 output and bandwith limiter

limiting the bandwidth of the signal going into the sample and hold stage. For this purpose the signal is sent through a bandwidth limiter before it is sent to the sample and hold stage. Form section 7.2 the signal to noise ratio of the signal sent to the sample and hold must be 40/1.

Since the signal is 0.4mV the noise that can be tolerated = 0.4mV/ 40

= 10μV

The following equation gives the noise sent out from the bandwidth limiter.

$N = (4KTR\Delta f)^{0.5}$

N = RMS noise coming out of the bandwidth limiter

T = Temperature of the chip (320K)

R = noise resistance of the previous stages (The noise is mainly generated by the magneto resistive array and diffamp1).

= 1100Ω

Δf= noise bandwidth of the bandwidth limiter

From the above equation it can be estimated that for N= 10mV the bandwidth Δf = 5MHz. The bandwidth limiter used is shown in Figure 8.1 and it is a simple first order RC low pass filter. The equivalent circuit for the diffamp3, and the bandwidth limiter is shown in Figure 8.2 . The resistance Ro is the output impedance of the diffamp3 and the resistance R1 is the ohmic resistance of the transistor T1. Cp is the parasitic capacitance of the sample and hold capacitor C. The resistance R of the RC filter is R1 + Ro, where Ro = 100K. The capacitance C of the RC filter is Cp. Since the RC filter is of first order,

3dB bandwidth of the filter = Noise bandwidth of the filter / 1.57

= 3.2 Mhz

The 3 dB bandwidth of the RC filter $= 1/(2\pi RC)$

If Cp is made to be 0.2 pF, the value of R1+ Ro can be estimated to be 248K. Therefore R1 is 148K.

By simulation, the size of the transistor T1 is estimated to be 2/16. The transistor T2 is used to reset the voltage of the point X to the DC bias voltage of diffamp3. This is done during the auto-zero process.

The signal input to the RC filter is 200mV. Thus the rise time allowed for the RC filter determines the percentage of signal present when the output signal is sampled by the sample and hold stage. To have sufficient signal this percentage is chosen to be 90%.

By simulation, it is estimated the rise time to get 90% of the signal is 125nS. Thus the final signal output from the bandwidth limiter is 180 mV and the delay is 125nS.

CHAPTER 9. SAMPLE AND HOLD

In the process of using an actual sense line and a dummy line to obtain a difference signal, unwanted voltage offsets are created due to thermal and process parameter variations. The magnitude of these variations is high and could be eliminated to a certain extent by auto-zeroing (mostly process variations). However the offset after auto-zeroing is too high for comparing the signal with a fixed reference voltage to determine the logic value it represents. Therefore a solution is to compare the signal from an auto-zeroed bit zero with the signal from an auto-zeroed bit one, where both signals are obtained from the same element. This is accomplished by reversing the sense current through the element (for positive current through the element the resulting signal is a zero, while for negative current through the same element the resulting signal is a one). Thus each of these signals should be sampled and compared. A circuit was developed to achieve this with minimum area, complexity and with circuits insensitive to component variation.

9.1 Sample and Compare Method

The entire sensing scheme including the new sample and compare circuit is shown in Figure 9.1. The graphs in Figure 9.1 show the signals at point X in the circuit for a stored zero and a stored one cases.

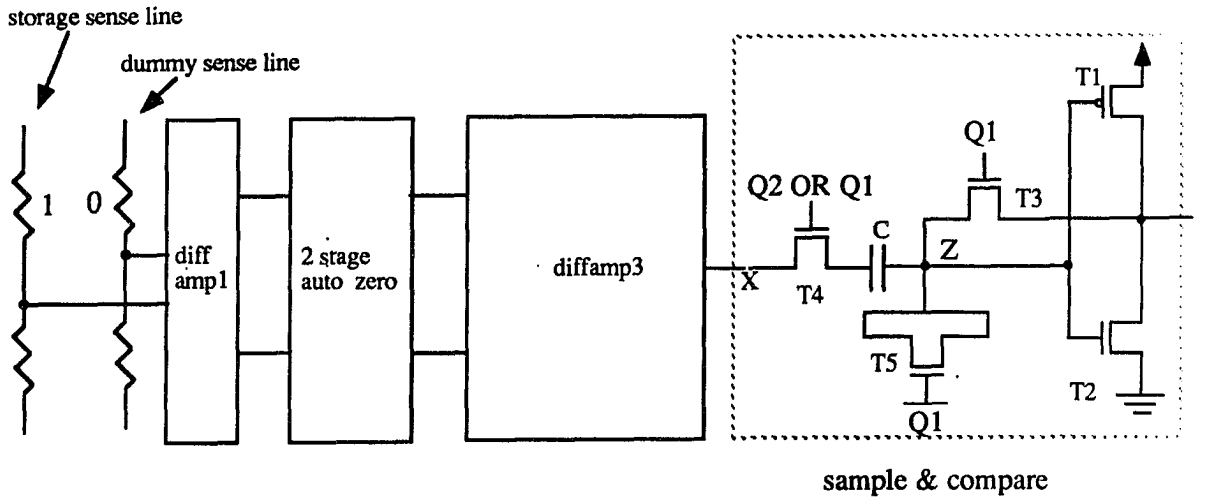


Figure 9.1 Sensing scheme with sample and hold circuit

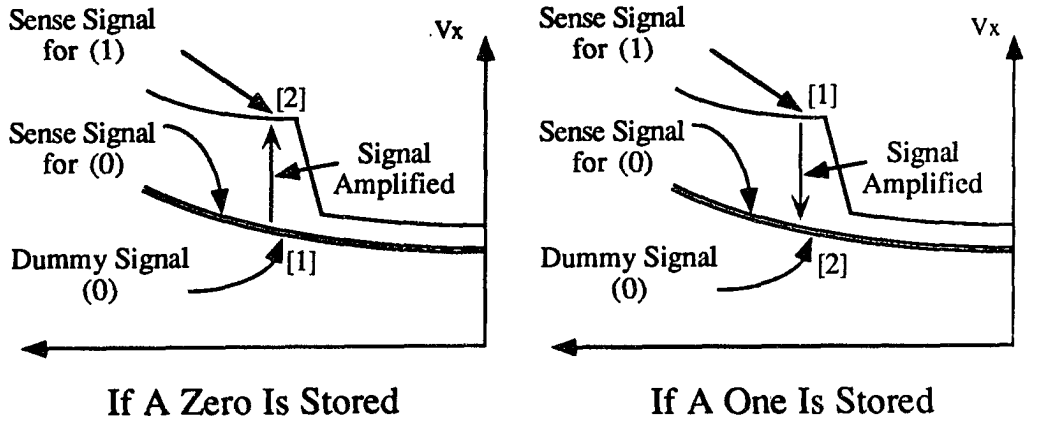


Figure 9.2 Signal input for a stored zero and a stored one

9.1.1 If a Zero is Stored

Consider first that the current through the element is positive (at time t_1) and voltage at X is almost zero since the element containing a zero is auto-zeroed with a dummy element which always contains a zero. Since at time t_1 gate T3 is on (Figure9.1) the output of the inverter of the sample and compare circuit will be fed back to its input ,and the output voltage will stabilize at a voltage that is independent of the process variations. If this feedback is not used, the operating point in the characteristic curve can vary drastically as shown in Figure 9.4.

After the voltage at input (Z) stabilizes, the Vxz(t1) voltage will be stored across the capacitor C. Then transistor T3 is turned off at time t2 and no feedback occurs. At the same time the current through the element is reversed to produce a one, and since at this time Q2 is high, the increase in voltage at X due to the one signal (0.4 V) appears at Z. This drives the inverter output to logic zero state.

9.1.2 If a one is stored:

As in the earlier case at time t_1, feedback occurs and the voltage at X (0.4 V) is stored across the capacitor. Then at time t_2 feedback is stopped, and since the current through the element is reversed voltage at X drops by 0.4 V. This drives the output of the inverter to a logic one.

From the above analysis it is clear that the absolute values of zero and one signals do not affect the output of the inverter, and only the difference affects it. This is a significant advantage in magneto-resistive sensing schemes since the absolute value of zero and one can vary considerably even after auto-zeroing due to component parameter variations and the characteristics of storage and dummy element not being identical for same state. Also as

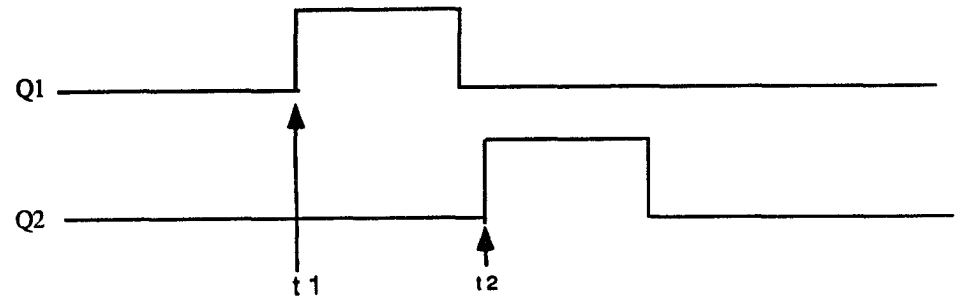


Figure 9.3 Timing for sample and hold

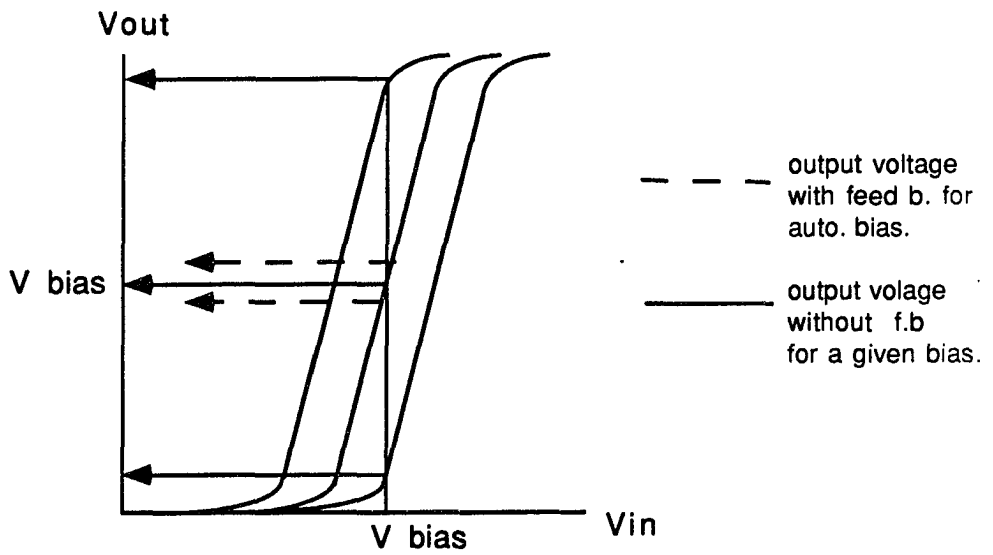


Figure 9.4 Characteristics of inverter amp in sample and hold

seen in Figure 9.4 the existence of feedback reduces the variation of the operating point with component variation, thus providing a larger linear region for amplification.

Simulations indicate that only a signal of + 15mV is required to generate a logic output with a delay of only a few nanoseconds. The signal input to the sample and hold stage is in 180 mV and it is adequate to generate logic level outputs. The transistor T5 is made half the size of the transistor T3 and is used to cancel the voltage swing at point Z which occurs when Q1 is inverted. This voltage swing occurs due to displacement of channel charges in T3.

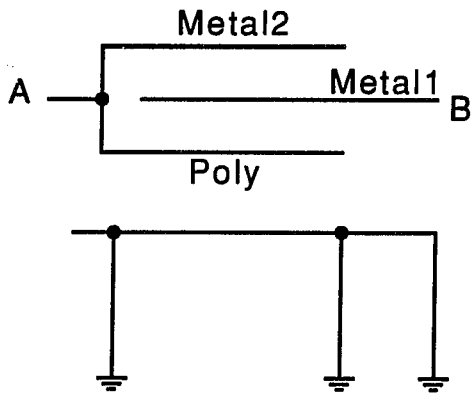
9.2 Capacitor Construction

The capacitor C for sample and compare is made using polysilicon, metal 1, and metal 2. The cross section of such a capacitor and the equivalent circuit for this structure is shown in Figure 9.5. C is the required capacitor and Cp is the parasitic capacitor formed.

$Cp = 6.5 \times 10^{-5}$ Pf/μm^2

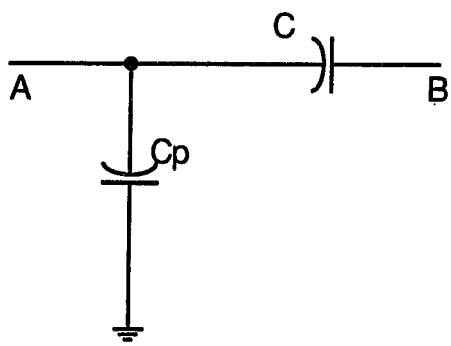
$C = 1.45\ Cp = 1 \times 10^{-4}$ pf/μm^2

Thus the surface area required for a 0.3 Pf capacitance is 3000μm^2. The 0.2pf parasitic capacitance (Cp) is used as the capacitor for the bandwidth limiter. The capacitors in the auto-zero stages are also constructed using the above structure.



Substrate

Structure



Equvelant circuit

Figure 9.5 Capacitor construction

CHAPTER 10. SPECIFICATIONS OF THE 1 MBIT MAGNETO-RESISTIVE MEMORY AND THE SENSING SCHEME

The specifications of a 1 Mbit magneto-resistive memory and a 4 Mbit Dynamic ram is given in order to compare the MR memory with the most popular primary storage technology. The MR memory is superior to the Dynamic ram with respect to number of masks, write cycle time and current. However the Dynamic ram has a much lower read time.

The complete circuit diagram for the sensing scheme is given in Figures 10.1 - 10.3. The timing diagram is given in Figures 10.4 - 10.5. The specifications of each sub block in the sensing scheme are given in tables 10.3 -10.7.

Table 10.1 Specifications of a 1Mbit Magneto-resistive memory and a 4Mbit DRAM

Parameter	1Mbit MR memory	4Mbit Dynamic RAM
Cell size (μm^2)	24 (0.8μm process)	9 (0.8μm process)
Die size (μm^2)	50	75
Number of masks	18	11
Read cycle time (nS)	800/byte	200/bit
Write cycle time (ns)	100/byte	200/bit
Average current (mA)	30	70

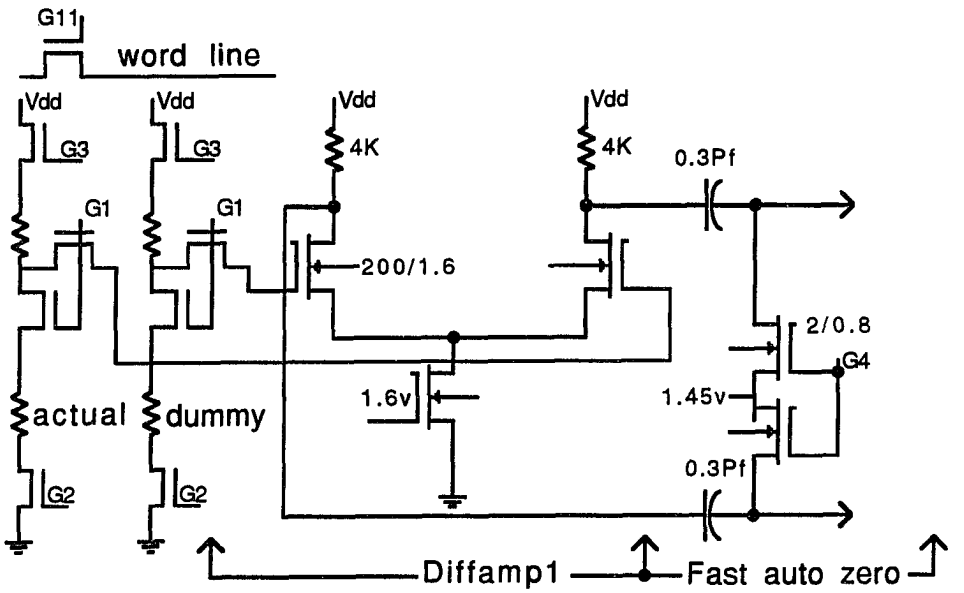


Figure 10.1 Schematic of sensing scheme (diffamp1 and first auto-zero)

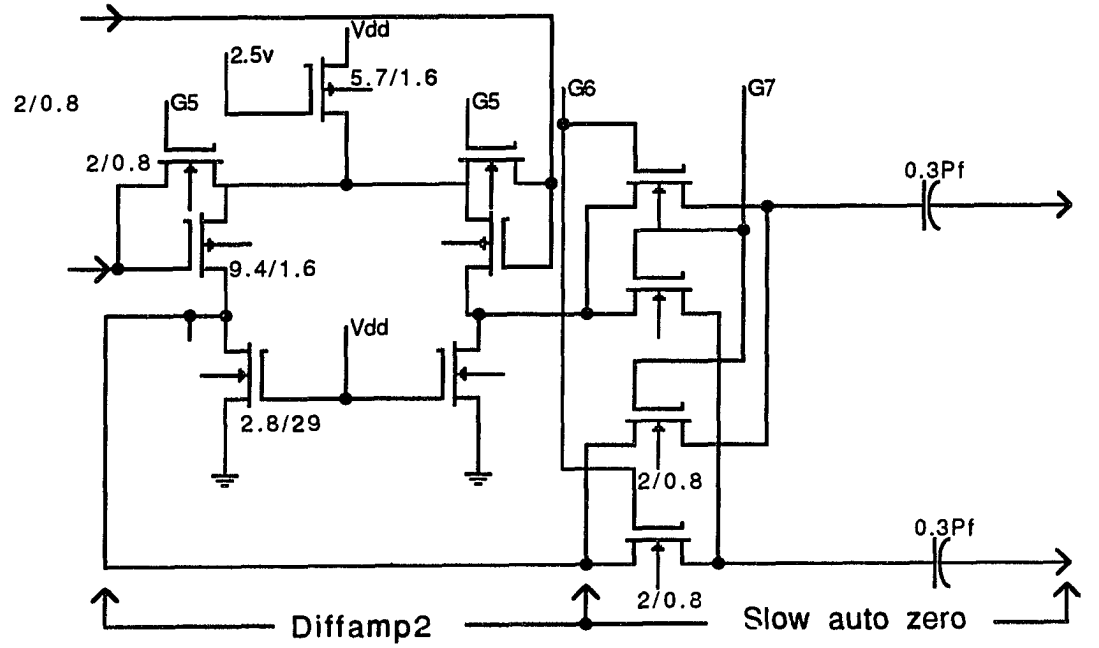


Figure 10.2 Schematic of sensing scheme (diffamp2 and second auto-zero)

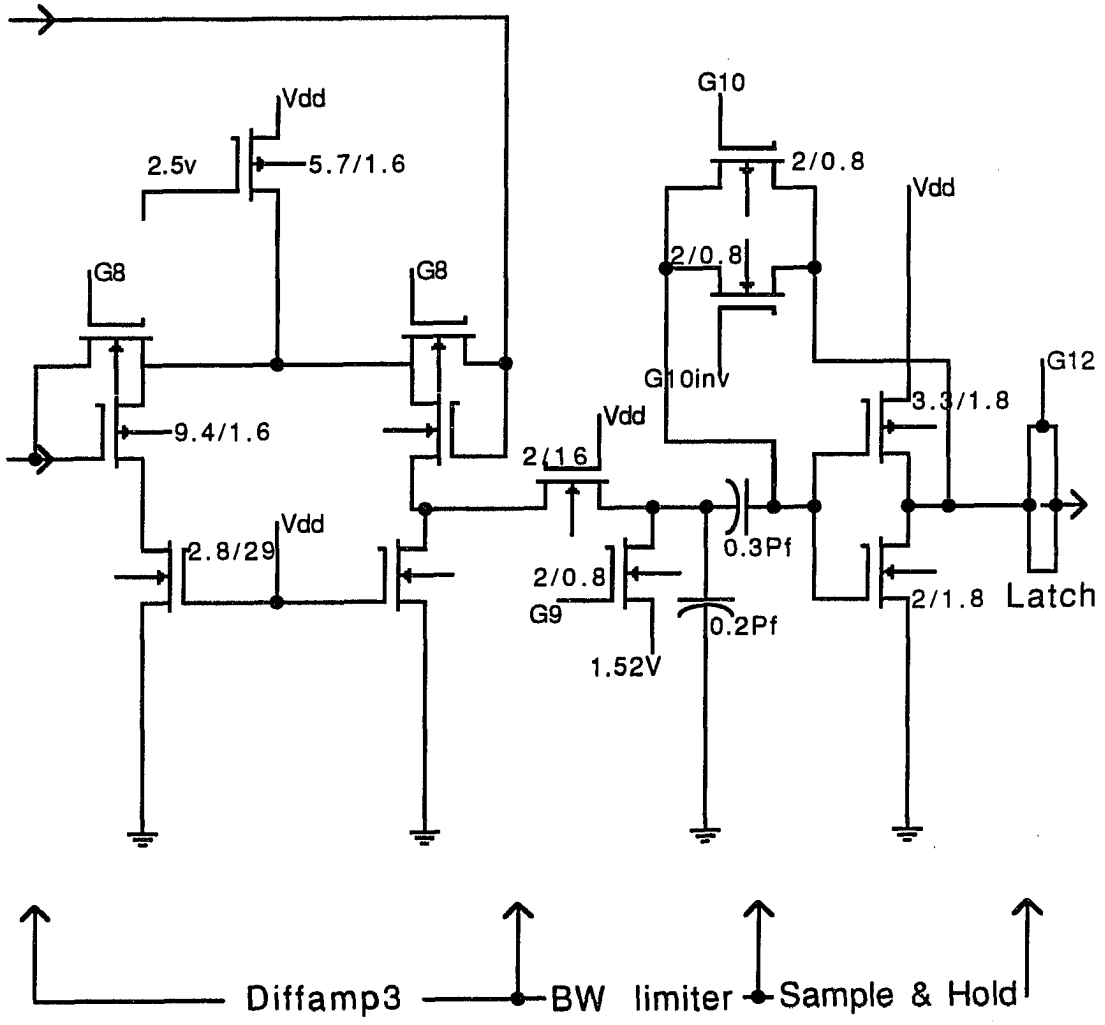


Figure 10.3 Schematic of sensing scheme (diffamp3, bandwith limiter and sample & hold)

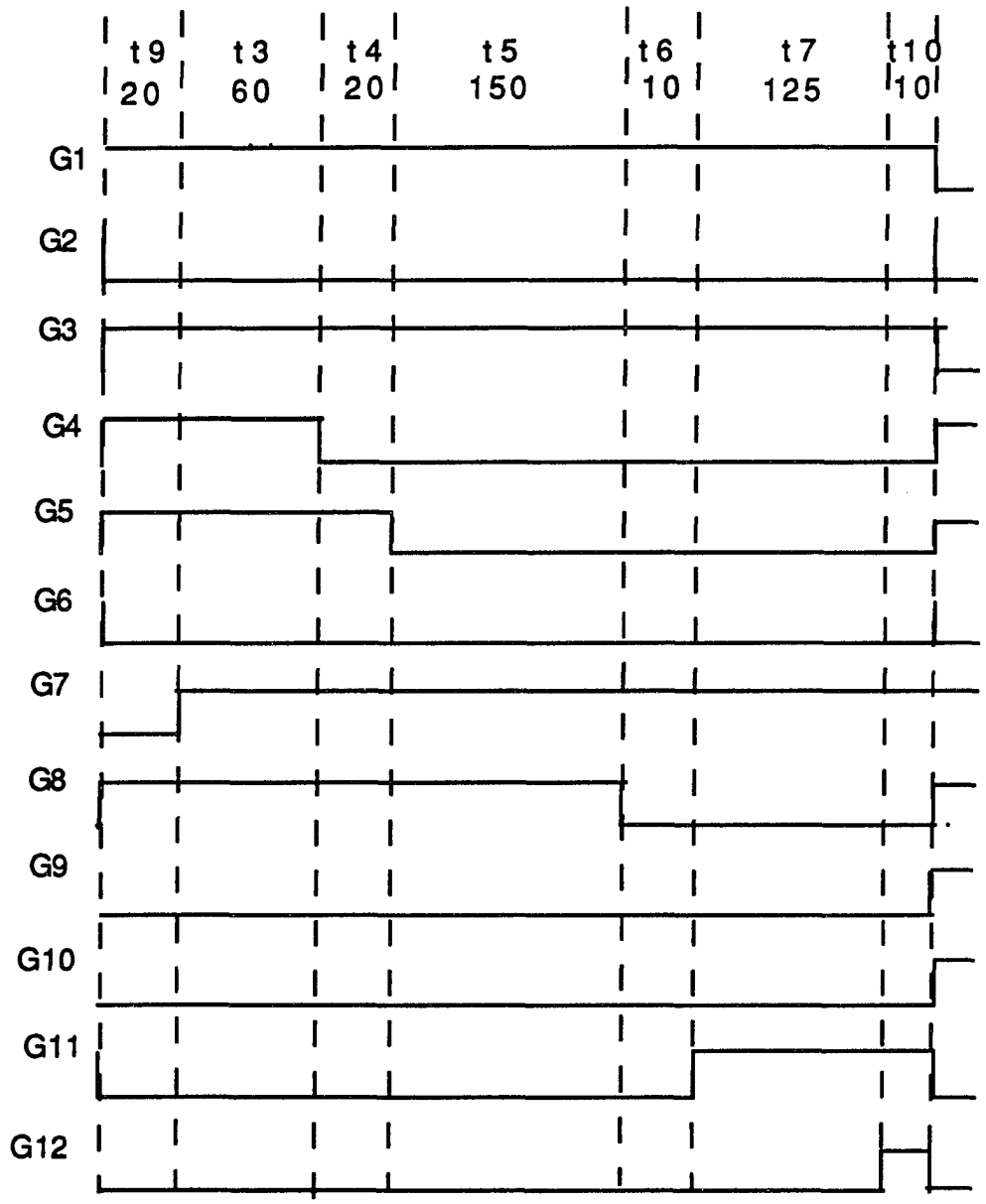


Figure 10.4 Timing diagram for the sensing scheme (first sample)

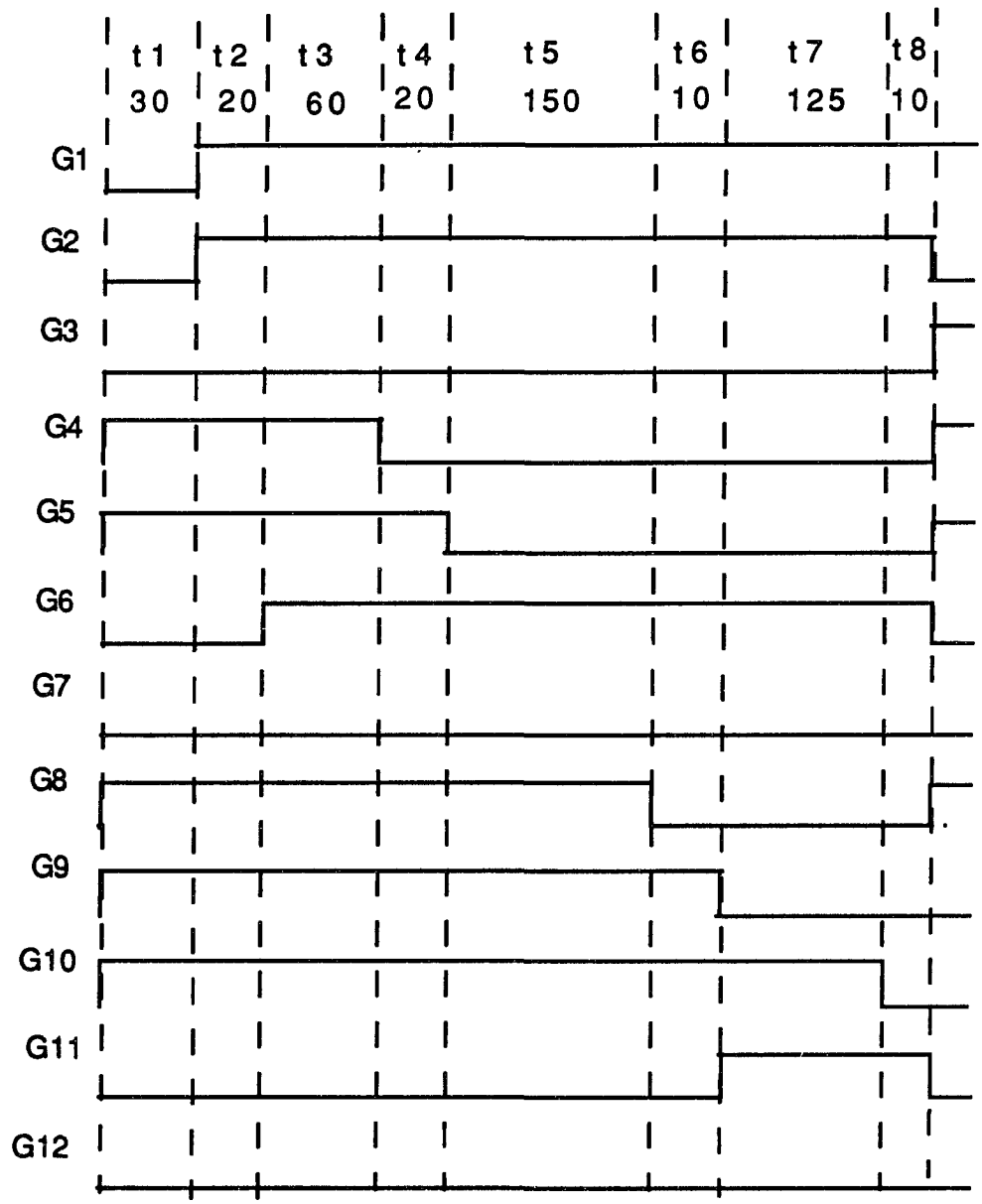


Figure 10.5 Timing diagram for sensing scheme (Second sample)

t1:	Address decoding time	= 30ns
t2:	Switching and settling time for the magneto-resistive array	= 20ns
t3:	Fast auto-zero time	= 60ns
t4:	Diffamp 2 offset removal time	= 20ns
t5:	Slow auto-zero time	= 150ns
t6:	Wait time to turn on the word current	= 10ns
t7:	Delay of bandwith limiter and sampling time	= 125ns
t8:	Wait time before reversing sense current	= 10ns
t9:	Switching and settling time when reversing sense current	= 20ns
t10:	Latching time	= 10ns

Figure 10.6 Timing values for the sensing scheme

Table 10.2 Specifications of amplifiers

Parameter	Diffamp1[9]	Diffamp2	Diffamp3
Gain	10	10	5
Bandwith (MHz)	150	16	16
CMRR	infinity	infinity	-
Current drain (mA)	2	0.1	0.1
Noise (nV/(Hz)$^{0.5}$)	2	-	-
Noise resistance (Ω)	250	-	-
Input offset (mV)	20	5	5
Signal input (mV)	0.4	4	40
Dynamic Range (V)	-1 -> 1	-0.8 -> 0.8	2.1 -> 2.9

Table 10.3 Auto-zero specifications

Parameter	First auto-zero[9]	Second auto-zero	Entire auto-zero
Offset input (mV)	1000	4.4 + 50	1000
Offset output (mV)	5 (due to diffamp1 input offset) 0.44 (due to noise generated)	10 (due to diffamp 2 and 50mV offset) 0.39 (reduced noise offset)	10 (due to diffamps) This is removed by sample & hold stage 0.39 (due to noise)
Offset rejection (dB)	67	21	88
Time constant (nS)	6	50	-
Time taken (nS)	60	150	200
Signal input (mV)	4	40	4

Table 10.4 Sample and compare specifications

Parameter	Value
Sampling rate (MHz)	1.4
Compare time (nS)	5
Minimum signal required to generate logic output (mV)	15

Table 10.5 Bandwith limiter specifications

Parameter	Value
Bandwith (MHz)	3.4
Rolloff (dB/Dec)	20
Rise time (0 - 90%) (nS)	125

Table 10.6 Magneto-resistive element array specifications

Parameter	Value
Resistance of a element (Ω)	50
Signal generated (differential) (mV)	0.4
Source/noise resistance (Ω)	850
Load capacitance (pf)	10
Bandwith (-3dB) (MHz)	28
Noise generated for 28MHz bandwith (μV)	26
Noise generated for 3.4MHz bandwith (μV)	9

Table 10.7 Specifications of the entire sensing scheme

Parameter	Value
Total area required (μm^2)	80x130
Signal amplified (mV)	0.4
Signal to noise ratio	20
Read access time (nS)	800

CHAPTER 11. CONCLUSION

A sensing scheme for 2.4 x 10 μm2 magneto-resistive memory elements has been developed. These elements generate a signal of 0.4mV. The sensing scheme uses a dummy element and a two stage switched capacitor auto-zero to remove the fixed DC offsets.It also uses self referencing to remove the remaining offsets. The glitches induced on the magneto-resistive array is made common mode using a balanced sensing scheme.

The self referencing process increases the bit density by 50% and the two stage auto-zero process reduces the read access time significantly. Simulations indicate a total read access time of 800ns (the write time is 100ns).

This sensing scheme is ideally suited for a 1Mbit memory with 2% magneto resistive coefficient elements. Recently magneto-resistive elements of 6% magneto resistive coefficient has been developed. These elements are called Giant magneto resistive elements. It is possible to fabricate these elements to have a size of 2.8 x 2 μm^2 which makes 16 - 32 Mbit magneto resistive memories viable. These new elements also produce a large signal of 2mV. The techniques and principles of the the sensing scheme developed could also be used in developing a sensing scheme for the new elements. Since the element signal is very much larger the delay of the individual stages of the sensing scheme can be reduced which would result in a significant reduction of read access time.

As the size of the magneto resistive elements continue to drop rapidly and the element signal continue to increase the magneto resistive memories are fast reaching the performance

levels of dynamic RAM's. This indicates a promising future for magneto resistive memories.

REFERENCES

[1] George P., "Magnetic megabits," *IEEE Spectrum*, May 1990, pp 32-38.

[2] Lu A., "Flash memories," *IEEE Spectrum*, Dec. 1989, pp 30-33.

[3] Granly G.B., Daughton J.M., Pohm A.V. and Comstock C S, "Properties of 1.4 x 2.8 micron active area Magneto-resistive elements" *IEEE Transactions on Magnetics*, Mag-27, (Nov. 1991), pp 5517 - 5519.

[4] Ranmuthu I. W., Ranmuthu K. T. M., Eray M., Comstock C.S. and Hassoun M., "Reprogrammable logic array using MR elements," *IEEE Transactions on Magnetics*, Mag-26, (Sept. 1990), pp 2828 - 2830.

[5] Pohm A. V., Comstock C.S. and Hurst A. T., "Threshold properties of 1,2 & 4 micron multilayer Magneto-resistive memory cells," *IEEE Transaction on Magnetics*, Mag-23 (Sept 1987) : CA -B.

[6] Kenkara S. W., "Response of Magneto-resistive memory elements to sub-nanosecond field pulses," *Masters thesis*, Iowa State University, 1989.

[7] Pohm A.V. and Costock C.S., "Quadrupled nondestructive output from Magneto-resistive memory cells using reversed word fields," *Proceedings of the 3M Conference*, Boston, 1989, IEEE, New York.

[8] Yoo H. Y., Pohm A. V., Hur J. H., Kenkare S. W. and Comstock C.S., "Dynamic switching process of sandwitched-structured Magneto-resistive elements," *IEEE Transactions on Magnetics*, Mag-25 (Sept 1989), pp 4269-4271.

[9] Ranmuthu K. T. M., "Low noise small signal sensing scheme for high density Magneto-resistive memories," *Proposal for Doctoral Research*, Iowa State University, March 1992.

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APPENDIX SIMULATION RESULTS

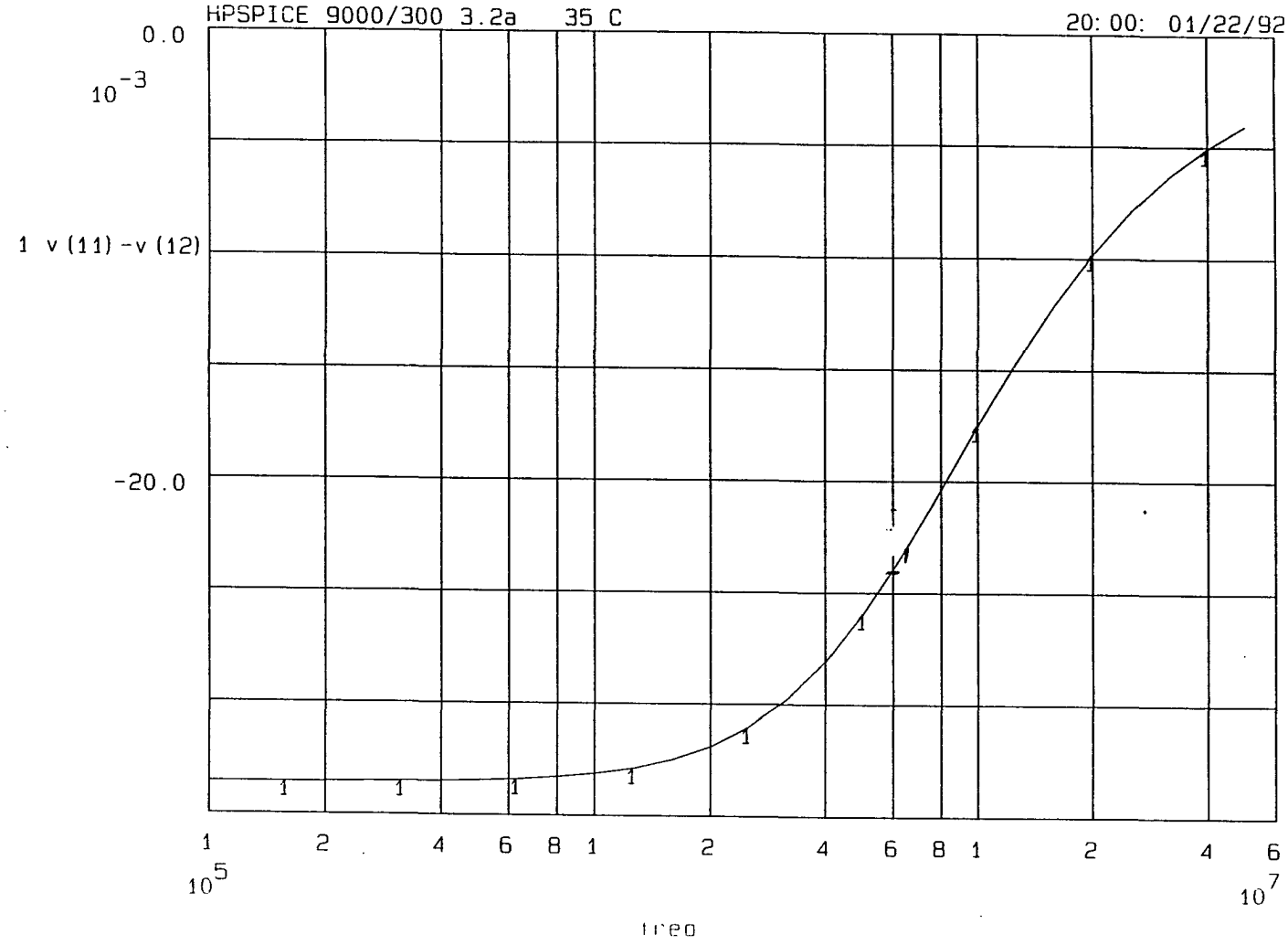

Figure A.1 Frequency response of diffamp2 and second auto-zero (when auto-zero off)

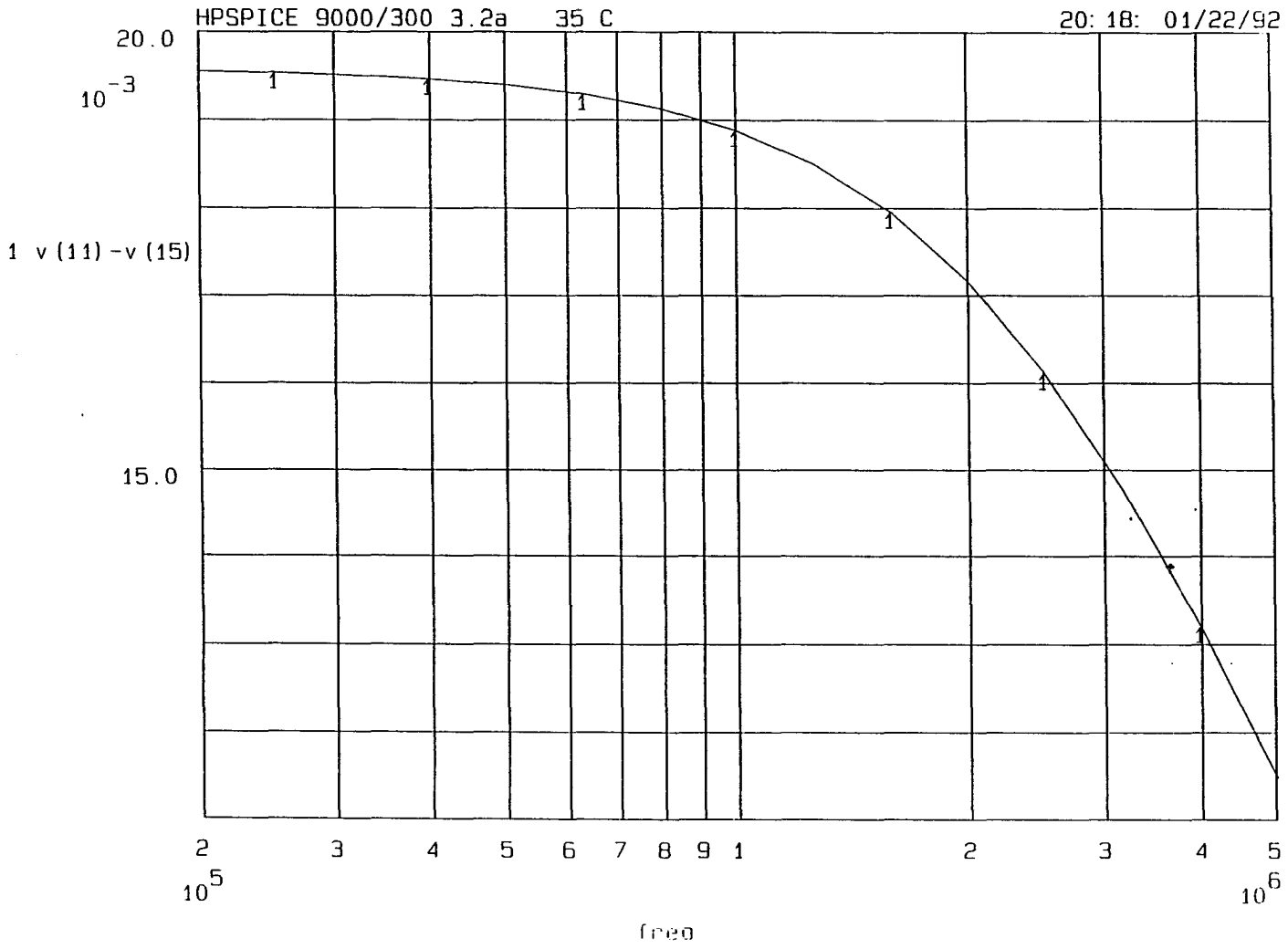

Figure A.2 Frequency response of diffamp2 and second auto-zero (when auto-zero on)

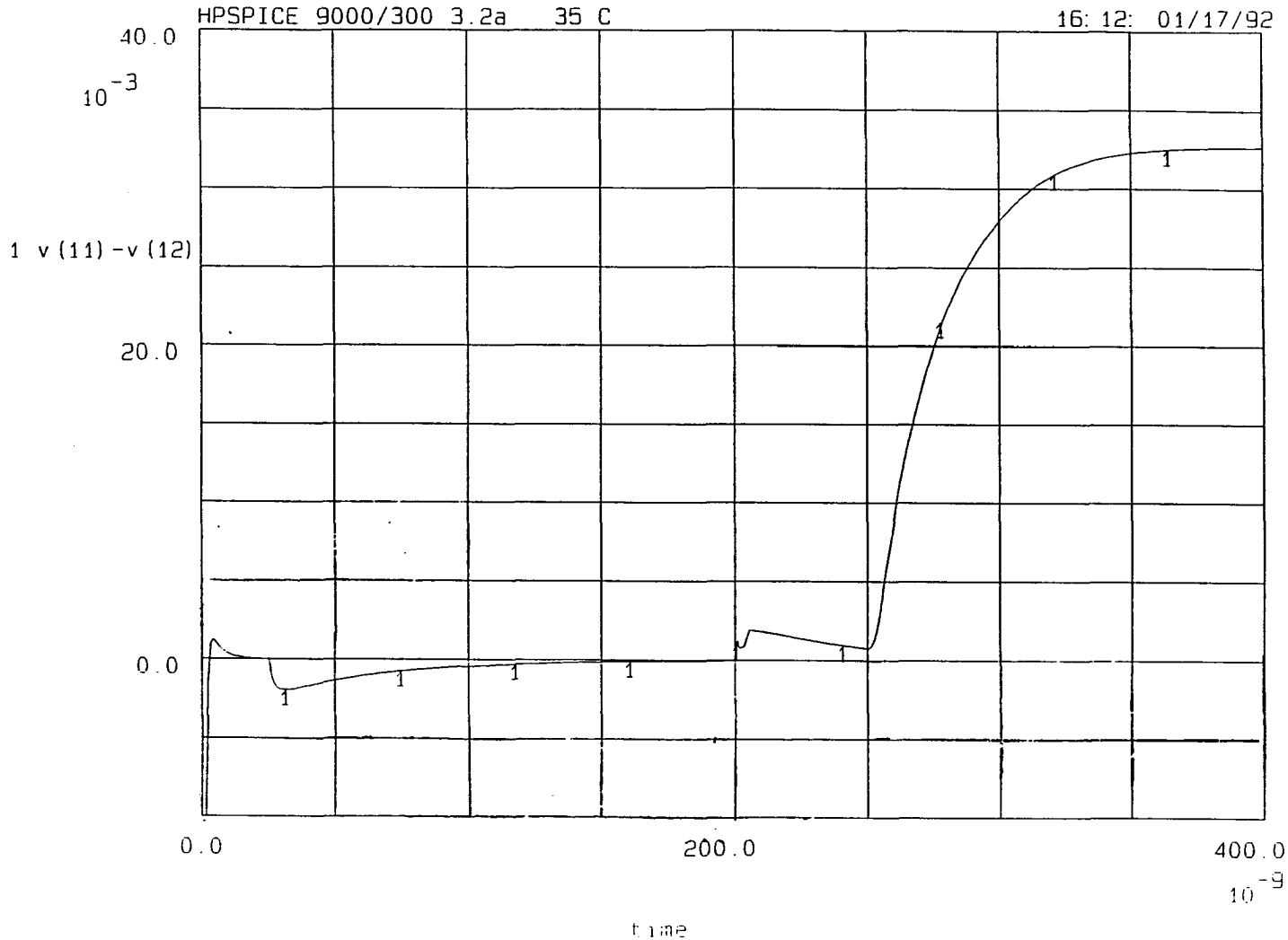

Figure A.3 Removal of a 4mv offset by second auto-zero and amplification of a 4mV signal

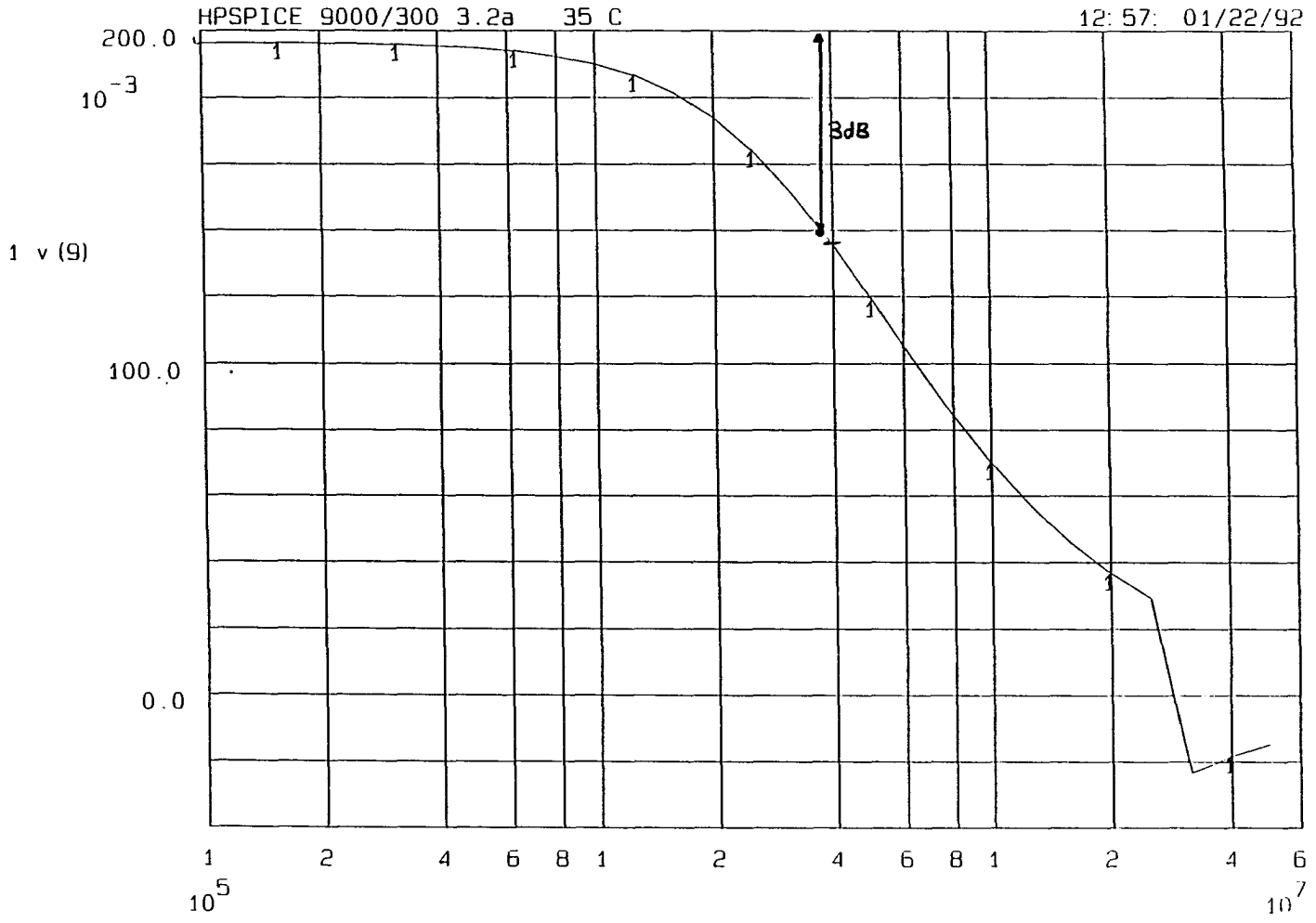

Figure A.4 Frequency response of the bandwith limiter

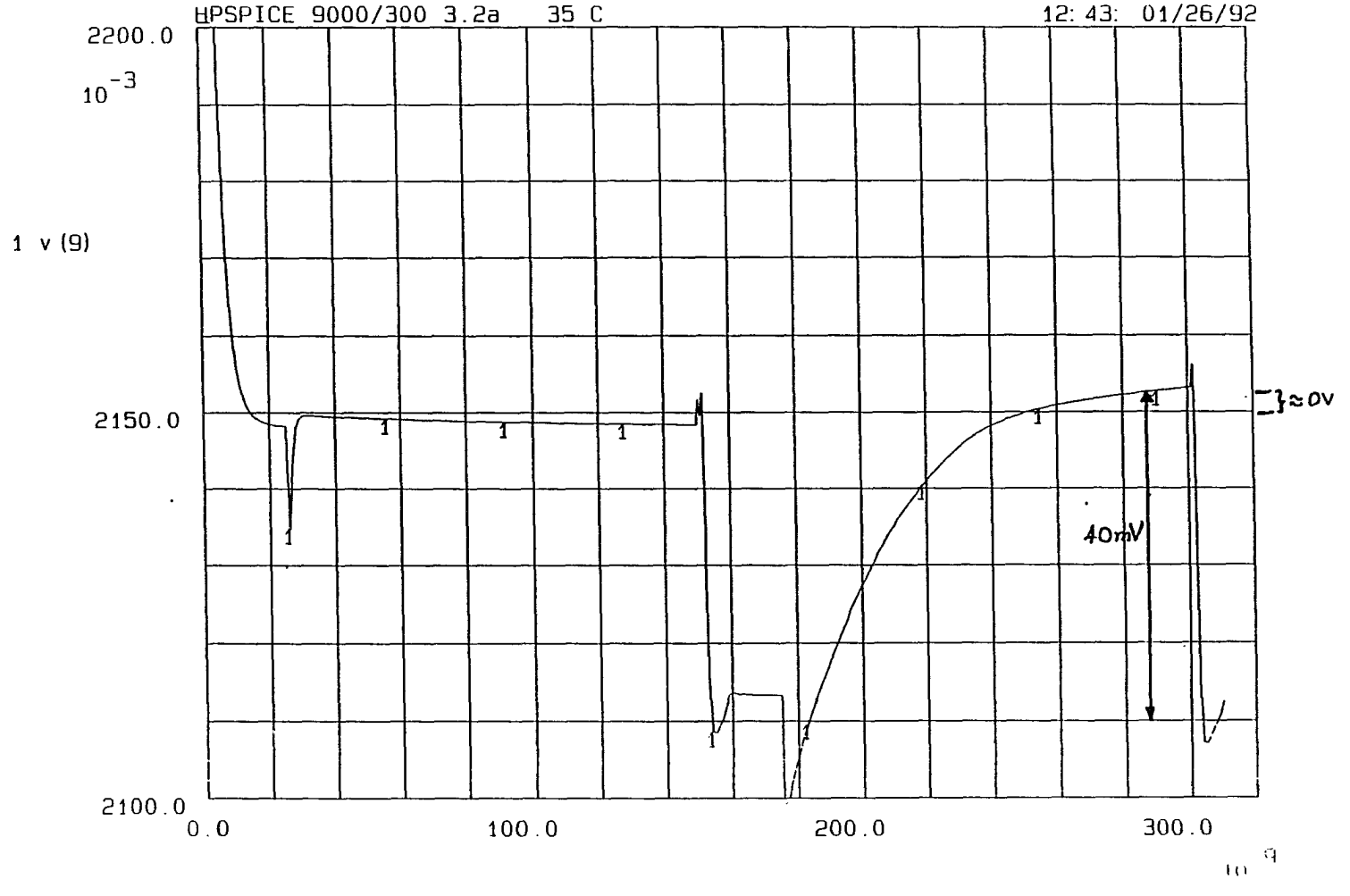

Figure A.5 Sample & h. output when sampling a 40mV signal and comparing with same

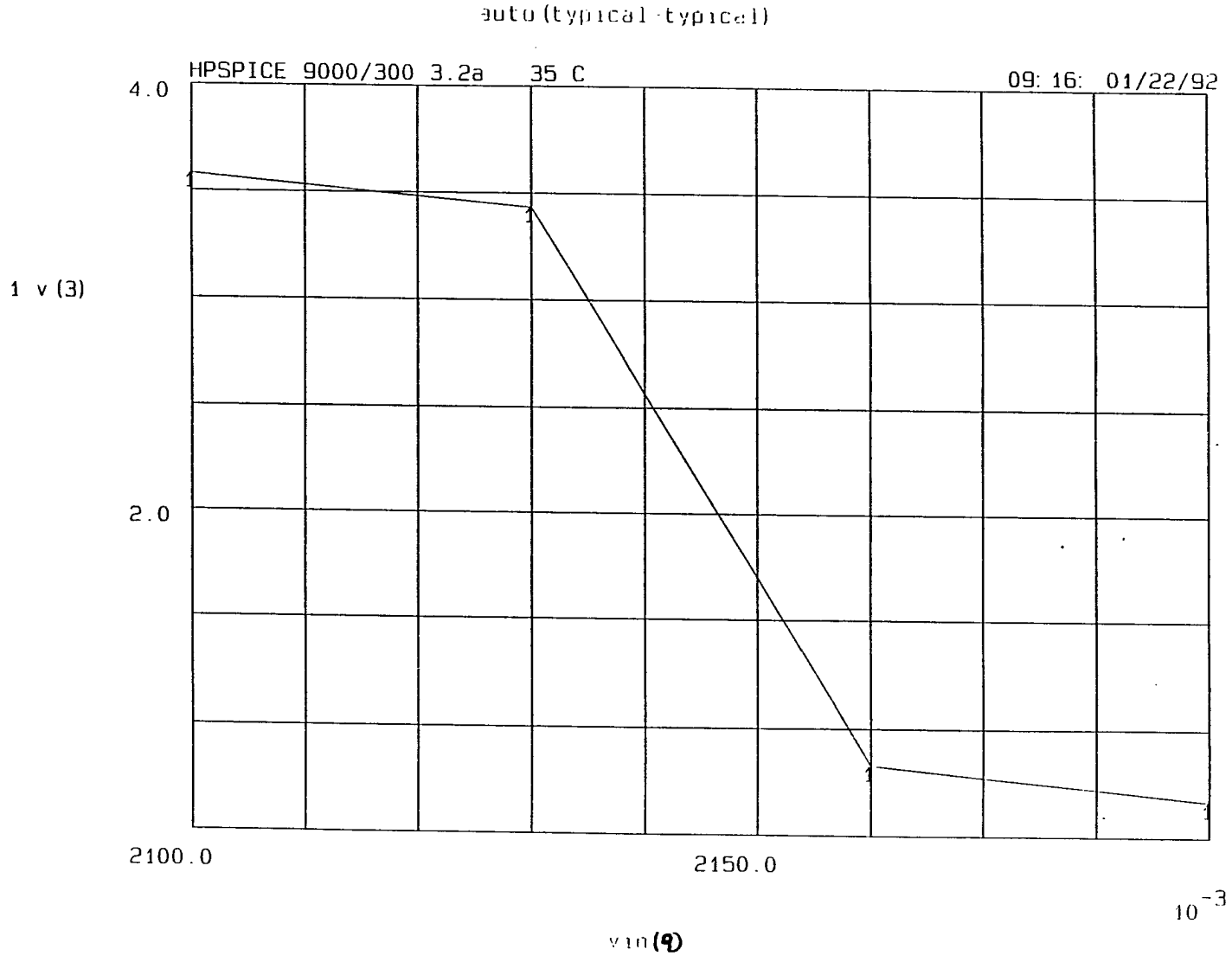

Figure A.6 Transfer characteristics of sample and hold inverter