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Design techniques for ultra low voltage CMOS continuous-time filters and continuous-time sigma-delta modulators

By

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Iowa State University

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ABSTRACT

In recent years, the increasing market and the increasing need of battery-operated portable equipment have pushed the industry to put much more efforts on developing new circuit techniques and new circuit structures to design circuit that can operate at very low supply voltages and with reduced power dissipation. Reducing power supply is a natural solution to reduce power consumption. However, reducing power supply does not always mean almost the same performance and lower power consumption. All of the above facts have produced the urgent necessity to find new circuit design techniques that can produce circuits operating at power supply voltage in the range of 1V to 2V. Although many techniques have been proposed to design discrete time low voltage CMOS circuits recently, few techniques were proposed to design their continuous-time counterparts.

In this dissertation, a technique that can be used to design low voltage CMOS continuous-time analog circuits is proposed. Some biasing current sources are added to the inverting or non-inverting opamp terminals such that the opamp input common-mode voltages could be shifted close to one of the supply rails for allowing low voltage operations.

A digital frequency and Q tuning technique is proposed for low-voltage active RC biquad filters that uses programmable capacitor arrays (PCAs). The proposed technique does not require any peak detectors, which are difficult to implement at low-voltage. Instead, it uses a few analog comparators, a digital comparator and a few binary counters to adjust the PCAs.

A direct digital background tuning technique for the notch frequency of continuous-time sigma-delta modulator is proposed to solve the large SNR loss problem caused by the deviation of the actual notch frequency from the desired value due to process and temperature changes. The converging condition, the converging time constant, the variance of the tuned notch frequency and the in-band noise power for a deviated notch frequency of the proposed tuning technique are analyzed. Many MATLAB simulation results are presented.

To demonstrate the proposed low voltage design technique, the frequency and Q tuning technique, and the notch frequency tuning technique, a 1V continuous-time low pass and band pass filter and a 1.2V continuous-time band pass sigma-delta modulator prototypes are designed, fabricated and tested. For a 5 kHz sine wave input signal, the filter achieves a THD of –60.2 dB for a peak-to-peak output voltage of 600 mV. The measured power consumption for the filter alone consumes about 0.52mW for a supply voltage of ±0.5 V. The measured DR for the 1.2 V modulator is about 40dB(6.5bit) and the peak SNR is 44dB(7bit). The power consumption is 2.1mW.

CHAPTER 1 INTRODUCTION

1.1 Motivation

Designing analog circuits that can operate at low voltages has been gaining an increasing importance in recent years. The demands for low voltage systems are mainly caused by three reasons. The first reason is the rapid increasing demand for battery-operated and solar-powered systems that require lower power consumption to prolong the battery life, and to minimize the number of batteries to reduce the volume and the weight. The other two reasons are due to today's advanced sub-micron technology. Smaller feature sizes result in larger local electrical fields as high as 5MV/cm [1]. This will cause reliability problems unless lower supply voltages are used. In addition, the power consumption per unit area has been increased due to the large integration. In order to reduce the power dissipation, supply voltages have to be reduced since the dynamic power consumption of digital circuits is proportional to the square of power supply. Nevertheless, reducing power supply voltage does not always reduce the power dissipation of analog circuits and sometimes may even increase it. However, in general, the total power consumption of digital and analog circuits, which are integrated in the same chip with the same low supply voltage, will be reduced a lot since most of circuits in mixed mode low voltage systems are digital. Therefore, it is worthy to reduce the power supply voltage along with the scaling process.

At moderate low voltages such as 3.3V or 2.5V, many of the proven circuit design techniques can be directly used as before or with little sacrifice of circuit performance.

According to CMOS technology projection, the power supply voltages will be reduced below 1.5 V [2][3]. For digital circuit design, it is capable to operate them at such low voltage even using the technologies available today [4]. However, scaling the supply voltage down to this range presents a formidable challenge to the design of analog circuits. This challenge comes from the fact that the threshold voltages of MOSFET devices are relatively high for the given supply voltage ranges. For future standard CMOS processes, the threshold voltages may not decrease much below what is available today [2]. Since many proven circuit techniques lose their validity when supply voltage is less than 1.5V, many techniques that can operate at power supply voltages in the range of 1 to 2 V were proposed in the literature recently as discussed below.

Although low voltage analog circuit design can be achieved using **low threshold voltage devices** [5][6], it is a high-cost solution due to the requirement of non-standard processing. Another solution is to use **on-chip DC-to-DC converters** or other **bootstrapping techniques** to increase the internal supply voltage. However, high internal supply voltage may not be tolerable for scaled-down technologies. Therefore, new circuit techniques must be developed to operate analog circuits at a low supply voltage using relatively high threshold voltage devices. It should be noted that these techniques would surely offer the potential for the best utilization of a given technology at any voltage range even if low threshold voltage technologies become standard.

One of the most common building blocks in analog circuit systems is the opamp. To achieve rail-to-rail signal swings at low supply voltages, input stages with rail-to-rail input common-mode ranges have been developed [7] [8] [9] in standard CMOS process with a supply voltage in the range of 1.2 V to 3 V. Supply voltage can go as low as 1 V if the input

differential stage of an opamp is realized using bulk driven MOSFETs [10] or depletion devices available in some specialized BiCMOS process [11]. With these opamps, many low voltage analog circuits such as active RC filters can be realized. However, designing analog circuits that require switches such as sample-and-hold amplifiers at low supply voltages still remains a challenge. When the supply voltage is less than the sum of the threshold voltages of PMOS and NMOS, the switches will fail to pass voltages in the mid-range of the power supply even if transmission gates are used [12]. To deal with this problem, **switched-opamp technique** has been proposed [13]. This technique avoids the use of critical switches to pass voltages in the mid-range by turning on or off the switched opamps. Hence, it can be used effectively whenever the output of an opamp drives the capacitors connected to the inputs of another opamp. Many switched-capacitor circuits can be implemented using switched-opamp technique such as discrete-time filter [12] and sigma-delta modulator [14].

Bulk-driven [15], floating gate and inserting floating battery [16] techniques can be used to design very low voltage continuous time circuits but the first two have severe gain-bandwidth limitations and the third one often requires complicated floating battery generation circuits. In this thesis, an alternative simple low voltage analog circuit technique is proposed to design ultra low voltage continuous time analog circuits. Like switched-opamp technique, it avoids the need to have a wide common-mode input range for opamps. At the same time, no critical switches for passing large swing voltages are needed. Using the proposed technique, a 1V continuous-time active RC filter and a 1.2V continuous time fully differential sigma-delta modulator are implemented in a conventional 1.2 μm and a 1.5μm CMOS process respectively.

1.2 Contributions

1. Literature survey for low voltage circuit design techniques.
2. A circuit technique for designing low voltage continuous-time active RC filters is proposed.
3. A simple digital frequency tuning method with programming capacitor array (PCA) is proposed in low voltage RC filters.
4. A Q tuning method, which does not require any peak detectors, is proposed for ultra low voltage continuous-time filters.
5. A direct digital background technique for tuning the notch frequency of continuous-time sigma-delta modulators is proposed.
6. A 1V band pass and low pass filter is designed, fabricated and tested.
7. A 1.2V continuous-time band pass sigma-delta modulator is designed, fabricated and tested.

1.3 Organization

Chapter 2 summarizes various problems associated with the design of low voltage analog circuits in standard CMOS process when the power supply voltage is in the range of 1-2V. Different low-voltage circuit design techniques are described and their advantages and disadvantages are analyzed and compared.

Chapter 3 introduces the proposed technique for designing low voltage active RC filters and explains in details how to design filters using the proposed technique.

Chapter 4 introduces the proposed Q factor tuning technique suitable for low voltage active RC filters and describes the frequency tuning method used in the low voltage filter prototype.

Chapter 5 describes a direct digital tuning method that can be used to tune the center frequency of BP filter in a continuous-time bandpass sigma-delta modulator. The convergence condition, converging time constant and the co-variance of the notch frequency after tuning are analyzed. Many simulation results are also presented in this chapter.

Chapter 6 presents the design guidelines, analysis, low voltage circuit block designs, simulation results and measurement results of a 1V second-order band pass and low pass filter fabricated in MOSIS AMI 1.2um CMOS process.

Chapter 7 presents the design guidelines, analysis, low voltage circuit block designs, simulation results and measurement results of a 1.2V second-order continuous-time multi-feedback (return-to-zero DAC and half delayed return-to-zero DAC) band pass sigma-delta modulator filter fabricated in MOSIS AMI 1.5um CMOS process.

Chapter 8 concludes the thesis with a discussion about the effectiveness of the proposed low-voltage filter design technique, the proposed frequency and Q tuning techniques and the proposed notch tuning technique according to the test results of the two prototypes. Finally, some possible future works are recommended.

CHAPTER 2 LOW VOLTAGE ANALOG CIRCUIT DESIGN

In this chapter, the issues and challenges along with low voltage circuit design are first discussed. The problems with the design of low voltage analog circuit are then described. Different low voltage circuit techniques available in the literature are presented in this chapter. Finally, the designs of several low voltage building blocks are discussed.

2.1 Introduction

Although it is capable to operate digital circuits at low voltage (1-3V) even using the technologies available today [4]. However, scaling down the supply voltage down presents many formidable challenges to analog circuit designs. These challenges come from the facts that the threshold voltages and the source-drain saturation voltages of MOSFET devices do not scale down at the same rate as the supply voltage or do not scale down at all with the scaling down supply voltages [2]. As a result, many popular circuit structures such as cascode structures lose their functions in low power supply designs.

Another formidable challenge for low voltage circuit design is the degradation of dynamic range. This is mainly due to that the noise floor does not scale down at all within low voltage circuits. Therefore, circuit techniques to reduce noise floor must be developed. To increase the dynamic range, fully differential topologies are frequently used. In some cases, lateral BJT's available in standard CMOS process can be used to provide up to several orders of magnitude of lower 1/f noise corner frequencies compared to the CMOS

counterpart. Larger gm of BJT's also means lower thermal noise. Thus, using lateral BJT's is a smart choice as the input differential pair transistors [17].

To meet the increasing demand for battery-operated systems, many arising issues with low voltage design have been widely studied and many new circuit structures and system topologies that are suitable for low voltage design have been investigated in literature. Several solutions were proposed to directly solve the high threshold voltage problem. Low voltage analog circuit design can be achieved using **low threshold voltage devices** [5][6], but it is a high-cost solution due to the addition of nonstandard processing. Moreover, low V_T transistors often have large leakage currents when they are OFF. The leakage causes the charge on the integrator capacitor to leak away. Usually it is signal dependent and consequently produces harmonic distortion. Another solution is to use **on-chip DC-to-DC converters** or other **bootstrapping techniques** to increase the internal supply voltage. However, high internal supply voltage may not be tolerable for future scaled-down technologies. Therefore, circuit techniques must be developed to operate analog circuits at a low supply voltage using relatively high threshold voltage devices. Several indirect solutions such as **bulk-driving, floating-gate, forward biased bulk-source and self-cascode** have been proposed in literature to circumvent the high V_T problems. It should be noted that these techniques would surely offer the potential for the best utilization to a given technology at any voltage range even if low threshold voltage technologies become standard in future.

Low power supply also presents challenges for analog circuits that require switches such as sample-and-hold amplifiers and switched capacitor circuits. When the supply voltage is less than the sum of the threshold voltages of PMOS and NMOS, the switches will fail to pass voltages in the mid-range of the power supply even if transmission gates are used [12].

To deal with this problem, **switched-opamp technique** has been proposed [13]. This technique avoids the use of critical switches to pass voltages in the mid-range by turning on or off the switched opamps, and hence, it can be used effectively whenever the output of an opamp drives the capacitors connected to the inputs of another opamps. All of these techniques will be briefly discussed after the discussion on the problems related to low voltage analog circuit design is presented.

2.2 Problems with Low Voltage Analog Circuit Design

2.2.1 Loss of square law relationship [19]

With the reduced power supply voltage and the small feature sizes for deep sub-micron transistors, the square law relationship does not hold any more. The crossover value of VGS-VT between the strong inversion and the velocity saturation at high current is approximated by [20],

$$V_{GS} - V_T = 4nL\frac{v_{sat}}{\mu} \tag{2.1}$$

For L=0.25um, it is about 2.5V. For small L, V_{GS}-V_T between the strong and the weak inversion is constant, about 800mV. The strong inversion region with the square-law relationship slowly decreases for smaller channel length and is expected to vanish by the year of 2004. The corresponding value of transconductance per unit current,

$$\frac{g_m}{I_{ds}} = \frac{2}{V_{GSsv} - V_T} \tag{2.2}$$

is low. Beyond V_{GSsv}-V_T, increased current does not yield any increase in transconductance. Hence smaller values of L lead to smaller supply voltages but not necessarily to lower power consumption.

In addition, for most desired low-voltage low-power circuits, the optimized tradeoff among area, power and speed must be carefully evaluated for different transistor operating regions. The best tradeoff is often obtained when transistors operate in the moderate inversion regions. In recent years, some modeling research works have been done to propose a one-equation model for all the operation regions [21][22]. It can be used to optimize circuit performance according to power consumption and speed.

2.2.2 Worse Mismatches[20]

Reduction of power supply directly reduces maximum signal swing. To achieve the same dynamic range, noise and or mismatch errors must be decreased. Noise and mismatch errors improve along with the square root of increased area. The V_T distribution is described by

$$\sigma(\Delta V_T) = \frac{A_{VT}}{\sqrt{WL}} \tag{2.3}$$

With A_{VT} slowly decreasing with L about 10mVum for an NMOS transistor with 0.5um channel length. For the same dynamic range, large silicon areas are required, leading to larger capacitance and hence means larger current and larger power consumption.

2.2.3 Switch Overdrive Voltage Reduction

Supply voltage reduction does not affect the properties of capacitors very much but it does cause some problems for the proper operation of MOS switches and opamps. This is due to the reduction of the overdrive voltage of MOS switches. This leads to the result that

the single MOS switches and even the transmission gate can no longer pass all signals through at low voltage. Figure 2.1 (a) and (b) shows the conductance of NMOS and PMOS transistors varies as the gate voltage Vx changes from 0 to V_{DD} at V_{DD}=5V and V_{DD} = 1.5V respectively. At 5V, their conductance is always higher than a minimum gm. As shown in Figure 2.1 (b), a critical voltage region centered around $V_{DD}/2$ in which both NMOS and PMOS switches are not conducting is present [23].

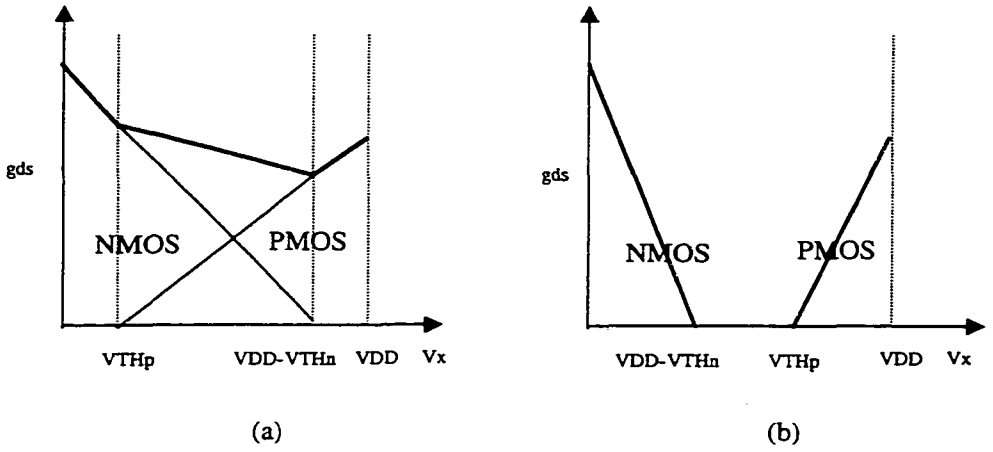


Figure 2.1 Switch conductance for two different supply voltage (a) V_{DD}=5Vand (b) V_{DD}=1.5V

2.3 Low Voltage Analog Circuit Design Techniques

2.3.1 Process Level Techniques

2.3.1.1 Multiple V_T or low V_T Transistors [5][6]

Multiple V_{TH} process or a low V_{TH} process, are two possible solutions to low voltage design from a process point of view. With these two methods, higher V_{TH} devices are used for the digital core to ensure good digital circuit performance and lower V_{TH} devices are used for analog blocks to make the threshold voltage compatible with the reduced power supply

voltage. Generally, low V_{TH} devices often have large sub-threshold leakage currents when they are off. Since several extra process steps are needed to be added, both of them have been proven to be high cost solutions for low voltage circuit design and are incompatible with most mainstream digital CMOS processes.

2.3.1.2 Floating Gate Transistors[19]

In this technique, another layer of poly-silicon is deposited on the canonical gate poly-silicon. The major difference between floating gate transistors and normal transistors is that the floating gate of floating gate transistors is not controlled directly by input signals but by the coupled signals through some poly-to-poly capacitor coupling. The idea behind this technique is that the equivalent threshold voltage seen from the control gates can be programmed by varying the amount of static charge on the floating gate. But the complex programming circuits and high programming voltage limit its wide application in low voltage circuit design. Figure 2.2 (a) and (b) shows the schematic symbol and equivalent circuit of multiple input MOSFET respectively.

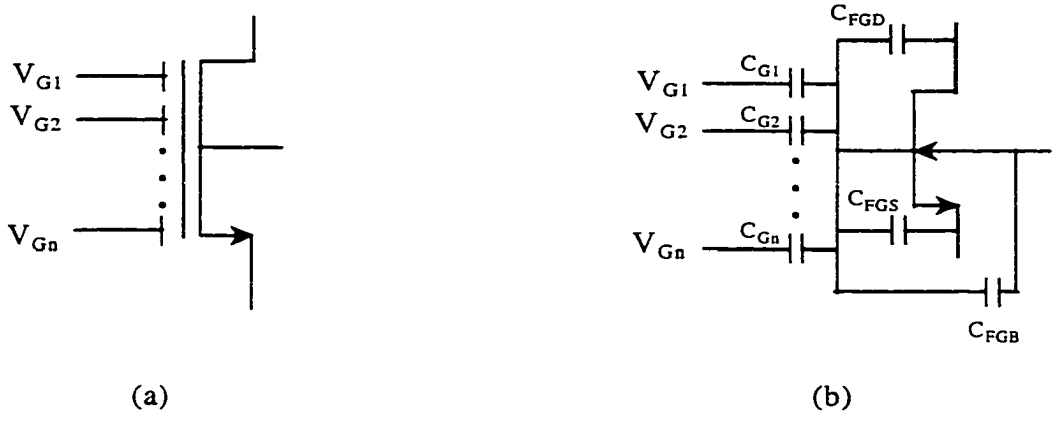


Figure 2.2 Multiple-input floating gate MOSFET
(a) Schematic Symbol and (b) Equivalent Circuit

2.3.2 Circuit Level

At circuit level, several circuit structures suitable for low voltage design such as voltage multipliers, bulk driving, forward biased bulk-source operation and self-cascode are proposed in the literature.

2.3.2.1 Voltage Multiplier

This technique uses an on-chip voltage multiplier to increase the internal voltage supply and hence increase the overdrive voltage of MOS switches, which can be used to solve the problems described in section 2.2.3. These multipliers are used for the critical switches, which have to pass large swing signals, especially for signals passing through the nearby region of $V_{DD}/2$. The disadvantage of this technique is that it can not be used in the deep sub-micron technologies due to the sub-micron process limitations. Another disadvantage of this technique is that it often consumes large area and large power. This technique can not be applied to future advanced processes, which can not withstand the high boosted clock voltage.

2.3.2.2 Bulk Driving MOSFETS

Bulk driven MOS transistor concept was first proposed in 1987[15]. A 1V bulk driven opamp with rail-to-rail input common mode range was designed in [10]. Different from the normal operation of MOS transistor, V_{GS} is kept constant as a bias voltage while input signal is applied to the bulk terminal. The advantages of bulk-driven transistors are [19]: i) depletion characteristics avoiding V_T requirement in the signal path, large signal swing, and very low power supply voltage required; ii) the real gate can be used to modulate the bulk-driven MOSFET. The disadvantages are [19]: i) The gm of a bulk-driven transistor

is substantially smaller than that of a conventional MOSFET, which leads to lower GBW and worse frequency response; ii) The polarity of a bulk-driven transistor is determined by the well type of a process. This limits its wide applications. iii) The equivalent input noise of a bulk-driven MOSFET amplifier is larger than that of a conventional one due to its smaller gm. iv) Prone to turn on the parasitic BJT's, which leads to latch-up problem.

2.3.2.3 Forward Biased Bulk-Source Operation [24]

This technique overcomes the high threshold voltage problem by forward biasing the bulk-source junction of a MOSFET. This can be done either by connecting the bulk to a slightly higher voltage than the source voltage or by injecting a small amount of current through the bulk terminals. V_{BS} is constant in the latter case while it is not in the previous case. By injecting a small current through the bulk terminals of well devices, the total supply voltage requirement of the complementary differential pair can be lowered.

2.3.2.4 Self-Cascode [19]

Self-Cascode structure [25] shown in Figure2.3 provides higher output impedance and larger voltage headroom than that of conventional cascode structures.

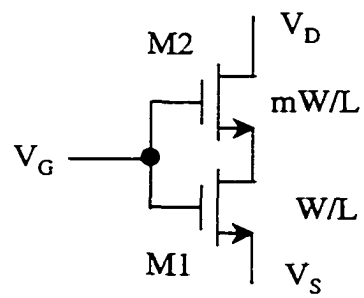


Figure 2.3 Self-cascode MOSFET

The lower transistor M1 operates in triode region as an input dependent resistor while the upper transistor M2 operates in saturation region. The source drain voltage of M1 is so small that there is no significant difference between the saturation voltage of M2 and that of the composite transistor. This advantage of the self-cascode structure can be used in low voltage applications.

The output resistance is roughly proportional to $m=(W/L)_2/(W/L)_1$. In practical cases, for optimal operation m should be larger than 1. Note that it is not necessarily to have different threshold voltages for the two transistors to operate properly. However, it does help to improve the output impedance [6] [27] to have $V_{T1}>V_{T2}$.

2.3.3 System Level

2.3.3.1 Switched Opamp Technique

The switched opamp technique uses the facts that most of the switches in switched capacitor (SC) circuits need not to conduct signal in the middle range of the power supply. Therefore, all these switches can be implemented naturally with PMOS or NMOS transistors depending on whether GND or VDD they are connecting to,respectively. All other critical switches were replaced with "opamp switch". Figure 2.4 (a) shows a typical switched capacitor circuit in which a switch was labeled as a critical one it needs to pass signals in the middle range. Figure 2.4 (b) shows the same circuit but with the critical switch replaced by a "opamp switch".

In this technique, the operation of the critical switch was replaced by the switched opamp. So the critical switch problem is circumvented. Since the switched opamp is often turned on or turned off, its outputs will be valid only during the on phase. During the off phase, its outputs will be pulled up to V_{DD} or down to GND.

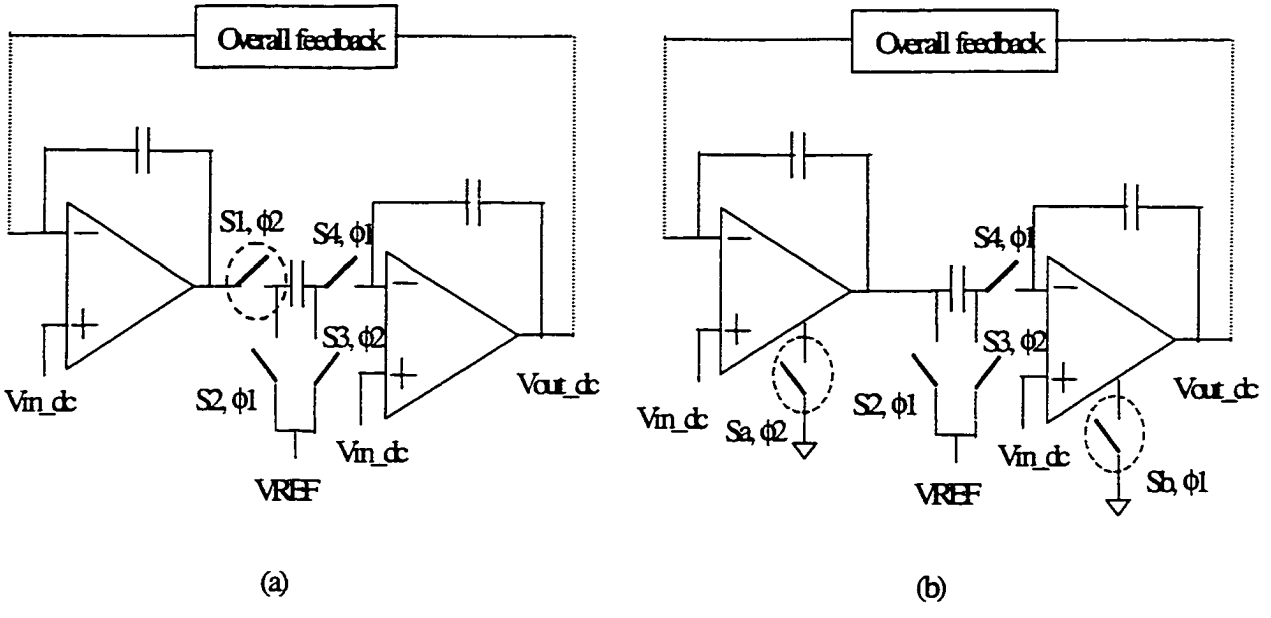


Figure 2.4 (a) Standard switched –capacitor integrator and (b) switched opamp integrator

However, there are three disadvantages of this technique. First, at the front end, critical switches connected to off-chip input signals can not be avoided and direct input through MOSFET switches usually result in a small signal input range [12][28]. Second, the outputs of the opamps in a switched-opamp circuit are always required to swing from one of the supply voltage during one of the clock phases and hence, the output signals may be slew rate limited. Third, this technique can only be used in some low speed systems because of the relatively long delay time of turning on and off the opamps. Despite these disadvantages, switched-opamp technique is a very effective technique to implement low voltage discrete-time analog circuits. Many low voltage switched-capacitor circuits can be implemented using switched-opamp technique such as discrete-time SC filter [12] and sigma-delta modulator [14].

2.3.3.2 Inserting floating battery technique [16]

This technique involves placing a floating battery in series with one of the opamp input terminals as shown in Figure 2.5 (a). The positive opamp input is connected to a DC reference voltage Vref, which is very close to GND or the negative supply rail. Also, a floating battery with the value of Vbias = V_{DD}/2-Vref is connected in series with the negative opamp terminal. This leads to the voltage on the positive terminal Vx ≅ V_{DD}/2. This technique can be regarded as the continuous time counterpart of the switched opamp technique but it also allows switched operation. Figure 2.5 (b) shows the low voltage implementation of an inverting amplifier with a gain $-R_2/R_1$, in which the floating battery was implemented with a resistor and two current sources.

The minimum supply requirements for this technique is:

$$Vsup(min) \cong V_{SG} + V_{ov} + V_{ref} \qquad (2.4)$$

where V_{SG} is the quiescent gate-to-source voltage of the input stage transistor (PMOS transistors are assumed). This technique can be used to design circuits with a single supply close to one transistor's threshold voltage (around 1 V) and with large signal swing.

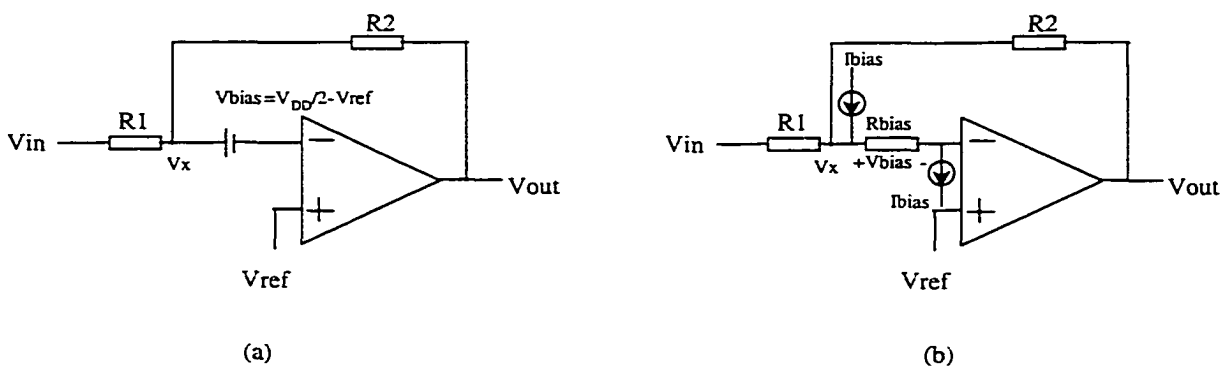


Figure 2.5 (a) Inserting floating battery technique and (b) simple implementation

2.4 Low Voltage Analog Building Blocks

2.4.1 Low voltage Current Mirrors

Current mirror is a very important building component of many analog blocks such as opamp and comparator etc. Due to constraints arising from low power supply voltage, low voltage current mirrors are required to have the following characteristics. i) low AC input resistance and small DC drop at the input node; ii) high output impedance; iii) low output compliance voltage so the maximum output signal swing is allowed; iv) good frequency response for high frequency application; v) a linear current transfer ratio.

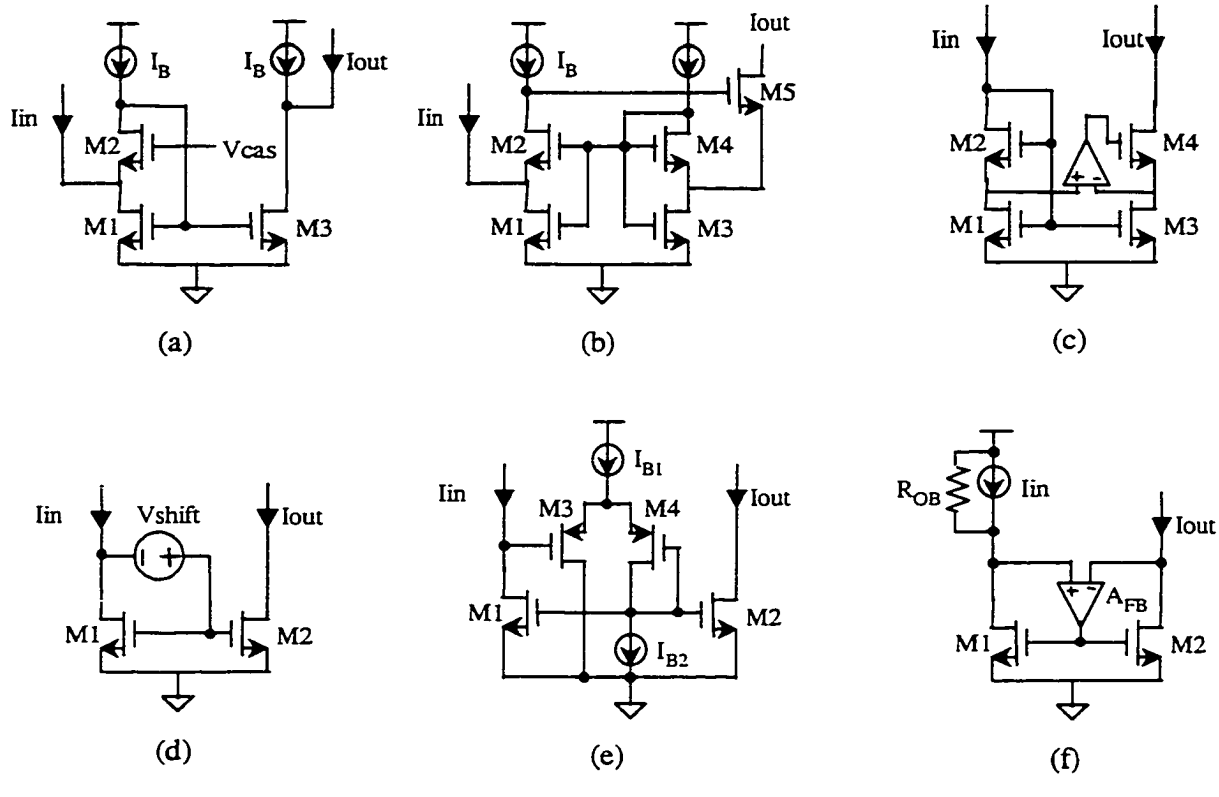


Figure 2.6 Low voltage current mirror (a) High swing current mirror with input current injected to the source of M2, (b) Prodanov's structure [29], (c) Itakura's structure [30],(d,e) Ramirez-Angulo's current mirror with input level shift [31], (f) F. You's structure [32].

A very good review to low voltage current mirrors can be found in [19]. Six different kinds of low voltage current mirrors are shown in Figure 2.6.

2.4.2 Low Voltage Opamp

The most important basic building block in analog and mixed-mode circuits is the operational amplifier. In a well-designed low voltage opamp, the minimum required supply voltage is decided by the differential input stage, and is equal to $V_T + 2V_{DSsat}$. For a typical CMOS process, this is almost 1V.Another main limitation of differential pair is the reduced input common mode (CM) range. For NMOS differential pair, this is limited between $V_{SS}+V_T+2V_{DSsat}$ to V_{DD}, while for PMOS differential pair, it is limited between V_{SS} and $V_{DD}-|V_T|-2|V_{SDsat}|$. In order to ensure rail-to-rail output swing and still to use the single polarity differential pair, the input and output dc levels must be set at different levels. This will be described in detail in chapter 3.

At some medium low voltages (3.3V or 2.5V or more precisely $V_{SUP}>V_{TN}+|V_{TP}|+4V_{DSsat}$), the traditional approach with N-P complementary rail-to-rail input stage [9] [33] [34] [35] [36] can be adopted easily. However, in order to achieve a constant g_m over the entire common mode input range, proper biasing circuits are required.

For very low supply voltage (less than 1.5V), there exists an input CM voltage range in the middle of supply rails, in which it can not turn on both PMOS and NMOS pair. Resistive dynamic level shift technique [33] [37] can be used to get a near rail-to-rail CM input swing with parallel connected NMOS and PMOS structures. In this technique, the input CM signal is adapted to the amplifier-input range by means of a front-end circuit based on a

CM feedback loop. Recently, many other techniques have been proposed to extend the input CM range of low voltage opamps:

- Floating gate MOSFET differential pair can be used to obtain a rail-to-rail input CM range[38]
- Bulk-driven differential pair can be used to achieve low voltage rail-to-rail CM input swing[10]
- Input CM adapter circuits can be used to shift input CM range close to one of the supply rails without having any changes to the input and output differential mode (DM) signals [33]

2.4.3 Low Voltage Analog Comparator

At high voltage circuit design, the comparator is always designed to have a differential pair as the input stage [39]. However, as discussed before, the input common mode range for a differential pair at low voltage is very limited unless some complementary input structures are employed. Another key problem of a low voltage comparator is the reset operation. Usually this is realized by shorting the two outputs at their metastable state with a switch. Again, a switch that can handle a level in the middle of supply rails is needed. To avoid this problem, instead of reset the outputs of a comparator to a middle voltage, they can be pulled up to VDD or pulled down to GND. However, this will limit the highest operating speed of the comparator.

One possible solution for designing a low voltage comparator is to shift the input voltages to an acceptable input common mode range such as one of the supply rails before comparison is done [14]. Another solution is to use resistance loads instead of transistor

loads in the differential stage to increase the input common mode range [40]. However, the most attractive solution is to use a current mode approach [41]. This approach can be used to design a low voltage comparator with a wide range input swing since the comparison of large voltage swing has been converted into current comparison.

2.4.4 Low Voltage Output Stage [19]

For low voltage designs, a rail-to-rail output swing is desirable to efficiently utilize the power supply. The type of loads decides the required driving capability and therefore the type of output stage. Common-drain voltage follower output stage is rarely used in low voltage design due to its small output voltage swing arising from the stacking of $V_{GS,P}$ and $V_{GS,N}$. Instead, common-source class AB configurations are widely used in low voltage designs due to its high output impedance, high voltage gain and rail-to-rail output signal swing. There are two categories of CMOS class AB output stage depending on how the quiescent current is controlled: i) without feedback loop; ii) with feedback loop. Usually, the second method can easily operate at lower supply voltage and has a better accurate control over the quiescent current but it may have stability problem because of the feedback loop.

2.5 Summary

The issues and challenges that analog designer will confront when the power supply voltage is reduced below 3V or even to 1V are reviewed in this chapter. Different low voltage circuit design strategies to implement high performance low voltage circuits are also discussed in this chapter. Finally, several very important low voltage building blocks are discussed in this chapter.

CHAPTER 3 DESIGN TECHNIQUE OF VERY LOW VOLTAGE CMOS CONTINUOUS-TIME ACTIVE RC FILTER

In this chapter, we summarize the issues of designing low voltage analog filters. Although some techniques such as switched-opamp were proposed to design low voltage discrete time filters, we focus on the design of low voltage continuous time analog filter. A proposed technique for converting high voltage continuous time active RC filters into low voltage designs is presented. Similar to switched-opamp technique, it avoids the need to have a wide common-mode input range for opamps. At the same time, no critical switches for passing voltage signals are needed.

3.1 Introduction

Low voltage analog filters are often required as pre- and post-processing blocks in front of and after the A/D and D/A interfaces in many mixed signal systems. It is usually required to integrate these filters with digital signal processing (DSP) circuits in a low-cost CMOS technology. To achieve this integration, Gm-C and MOSFET-C techniques are usually the choices to integrate these continuous-time filters especially for high frequency applications [42][43]. For high linearity and high dynamic range applications such as telecommunication applications, active RC filters based on poly resistors and programmable capacitor arrays are often used [42][43]. However, the supply voltages for advanced CMOS processes have been reduced continuously due to reliability issues and will reduce down to

1.5 V and below in the near future [2][3]. As a consequence, designing analog filters at low supply voltage presents a great challenge.

3.2 Filter Techniques for Very Low Voltage Analog Filters

Low voltage analog filters can be realized with continuous time or discrete time techniques. SC and SI are the two most common discrete time techniques while MOSFET-C, gm-C, current mode circuit and active RC circuits are the most common continuous time choices [44].

We have discussed the key limitations that arise due to the reduction of power supply in chapter 2, namely, small voltage headroom, reduced voltage swing and switch operation problem. All of the above factors must be considered when designing low voltage analog filters with the above techniques.

In chapter 2, three techniques, low V_T process, voltage multiplier and switched opamp, have been proposed to solve the switch problem successfully in the literature and therefore all of them can be used to design low voltage (as low as 1V) SC filters [12].

It is very difficult to make a fair comparison among those continuous time filter techniques. Generally, it depends on the specific application, the performance requirements and the limitations of specific technique. Gm-C technique offers the highest signal bandwidth but they are sensitive to parasitic. While the MOSFET-C filters are insensitive to parasitic, it has a low signal bandwidth. Current mode filter techniques often exhibit simple structure, low voltage implementation capabilities and high frequency potentials but they are sensitive to parasitic and noise [45]. Active RC filters usually achieve high linearity and high dynamic

range. Nevertheless, the cutoff frequencies of all the continuous time filters are inaccurate without tuning, which becomes critical when a continuous time filter with accurate frequency response is desired.

Two common concerns for designing low voltage analog filters are the quick reduction of tunability [44] and the difficulty to realize good peak detectors at low voltage. Companding filter designs based on MOSFET square law [46] are another technique proposed for low voltage filter design in CMOS process. Its disadvantage is that circuit linearity is limited by the non-perfect square-law device characteristic at low voltage as discussed in chapter 1.

Companding filter design based on exponential transistor characteristic has been applied successfully to design continuous time filters with low supply voltage. However, a bipolar or a BiCMOS process is required. To be compatible with CMOS process, MOSFET transistors operated in sub-threshold region that behave like a bipolar transistor can be used. However, the frequency response is limited and the supply voltage is usually higher than 1.5V. In addition, most circuit simulators do not model the sub-threshold region accurately.

3.3 Proposed Technique for Designing Ultra Low Voltage Continuous-Time Active RC Filters

Unlike the discrete time counterparts, fewer research works have been done on the design of continuous-time filters with ultra low voltage. This work mainly focuses on the design of continuous time active RC filters with power supply voltage down to 1V.

When Gm-C and MOSFET-C techniques are used, the minimum required supply voltage is usually greater than $V_{swing} + V_T + V_{OV}$ where V_{swing} is the signal swing and V_{OV} is

the minimum overdrive voltage for a MOSFET [44]. For a 1 V power supply, V_{swing} will be limited to about 100 mV or less, unless a low threshold process or floating gate technique is used.

In this section, a low voltage technique that can be applied to design low voltage active RC filters for high linearity applications is presented [47] [48] [49]. In this technique, several biasing current sources are added to the inverting and/or non-inverting opamp terminals such that the opamp input common-mode voltages could be set close to one of the two supply rails for allowing low voltage operations. In order to complete a practical low voltage filter design, on-chip automatic frequency and Q tuning techniques suitable for low voltage active RC filter using PCAs are also proposed in this thesis and presented in chapter 4.

At low supply voltage, a main problem for designing analog continuous-time filters is the dynamic range degradation. This is even worse in mixed-mode systems due to the interaction between the analog filters and the adjacent digital circuits on the same chip. For this reason, a large signal swing is very important in low voltage system to increase the immunity of the filter from the disturbances produced by adjacent circuits. Usually, the quiescent input and output voltages of the filter must be set at the middle of the supply rails to get a maximum dynamic range. The required close to rail-to-rail signal swing at the filter outputs can be achieved using active filter with inverting opamp configurations as shown in Figure 3.1 (a) but without the current source I_1. For a typical opamp with a PMOS differential pair as the input stage, the maximum input common-mode voltage is equal to $\mathbf{V_{DD} - |V_{TP}| - 2V_{SDsat}}$. To have the quiescent input and output voltages set at the middle of the supply rails, the input common-mode voltage of the opamp should also be set at the

middle of the supply rails. As a result, the minimum required supply voltage is equal to $2(|V_{TP}| + 2V_{SDsat})$, which will be larger than 1 V for $|V_{TP}| > 0.5$ V. In order to use a supply voltage as low as 1V, similar to the switched opamp technique, the quiescent input and output voltages of opamps must be set at different voltages independently.

A proposed solution to implement this is that a current source I_1 is added to the inverting opamp input [50] [51] such that the input common-mode voltage of the opamp can be set at a voltage V_x, which is close to ground or V_{DD} as shown in Figure3.1 (a). If I_1 is implemented with a NMOS transistor as Figure3.1 (b), V_x must be set at least one V_{DSsat} above ground to keep M_1 operating in saturation region. The minimum supply voltage for this Biased inverting opamp structure (**BIOS**) is almost equal to:

$$V_{min} \cong 3V_{SDsat} + |V_{Tp}| \qquad (3.1)$$

which is equal to one V_{Dssat} required for the biasing current source plus the minimum voltage required for the PMOS input differential stage ($2V_{SDsat} + |V_{Tp}|$).

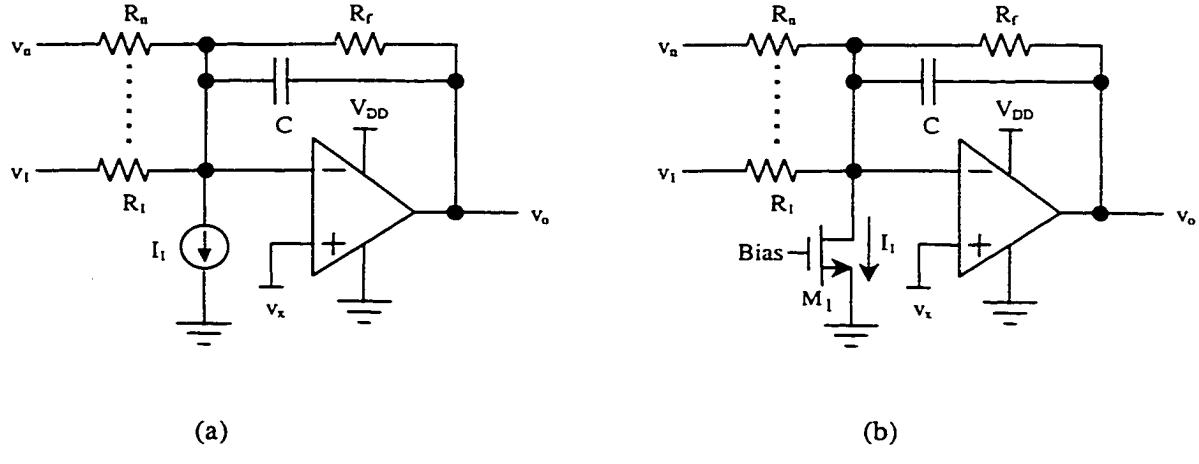


Figure 3.1 Proposed biasing inverting opamp structure for active RC circuit (a) general structure with current source (b) current source implemented with a NMOS transistor (c) current source implemented with a resistor (d) a simple practical BISO example.

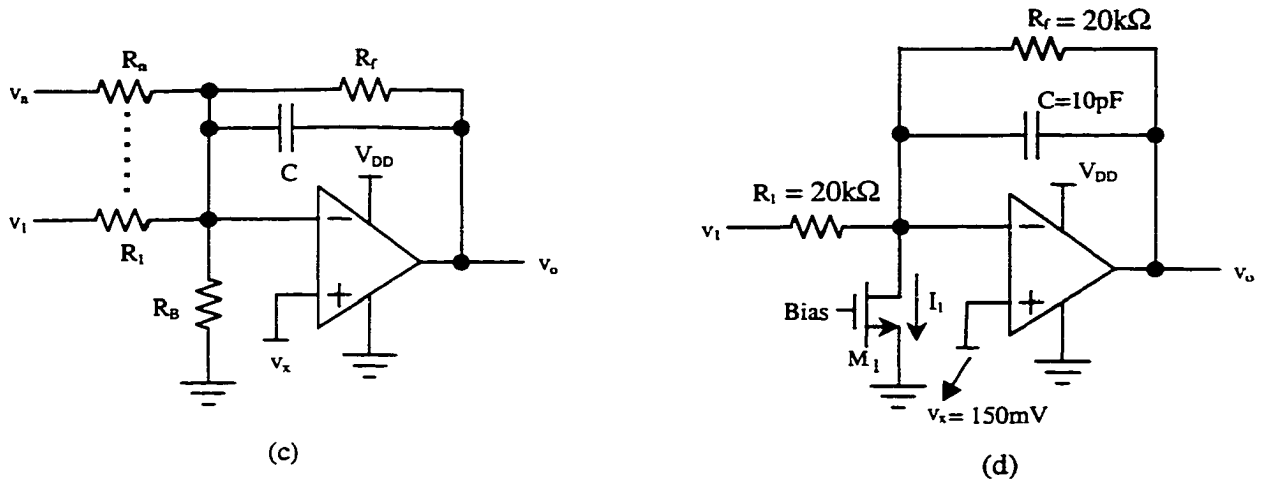


Figure 3.1 (Continued)

If a NMOS input differential stageis used, similar minimum supply voltage can be derived. But the current source is connected between V_{DD} and the negative terminals of the opamp. Vx must be set at least one V_{SDsat} below V_{DD} to keep the PMOS current source operating in saturation region. At lower supply voltage, the headroom voltages and overdrive voltages are reduced. For example, if $V_{Tp} \approx -0.8$ V and $V_{min} = 1$V, the minimum average V_{SDsat} is about 70mV.

If an opamp consumed a total current of I_{bias}, the total power dissipation for a conventional design without additional current sources I_1's is equal to $\mathbf{2n(|V_{TP}| + 2V_{SDsat})I_{bias}}$ where n is the number of opamps used in the design. If the same opamps with the current sources I_1's can be operated at the minimum required supply voltage, then the power dissipation will become $\mathbf{n(|V_{TP}| + 3V_{SDsat})(I_{bias}+I_1)}$. Notice that an extra current of nI_1 is required in the low voltage design. The difference in power dissipation between the low voltage design and the conventional design without I_1's is equal to $\mathbf{n(I_1-I_{bias})|V_{TP}|+n(3I_1-I_{bias})V_{SDsat}}$. If the low voltage design is properly designed (in particular, when each extra

current source I_1 is part of the biasing current for the opamp output stage as discussed in [52]), I_1 will be smaller than I_{bias} and the proposed low voltage technique will have lower power dissipation than the conventional design, especially for $V_{SDsat} < |V_{TP}|$. However, the above argument is only valid when the opamp architecture and the opamp current consumption do not change for different supply voltages and the dynamic ranges of both circuits are not considered. In practical realization, all of these may not be the same when the supply voltages are different. As a result, the proposed low voltage technique may not necessary lead to a low power dissipation design.

From Figure 3.1 (a), the quiescent output voltage of the BIOS can be determined by choosing quiescent input voltage, resistor values and biasing current value using the following equation:

$$V_{out\_dc} = (I_1 - \frac{V_{in\_dc} - V_x}{R_{eq}}) \cdot R_f + V_x \qquad (3.2)$$

Equation (3.2) can also be rewritten as:

$$V_x = V_{out\_dc} - (I_1 - \frac{V_{in\_dc} - V_x}{R_{eq}}) \cdot R_f \qquad (3.3)$$

where $R_{eq} = R_1 // \cdots // R_n$. If $V_{in\_dc}=V_{DD}/2$ and $V_{out\_dc}=V_{DD}/2$ are chosen (usually desired in practice, the required biasing current I_1 can be derived as:

$$I_1 = \left(\frac{V_{DD}}{2} - v_x \right) \left(\frac{1}{R_f} + \frac{1}{R_{eq}} \right) \qquad (3.4)$$

Equation (3.2), (3.3) and (3.4) are the fundamental equations for using the proposed low voltage design technique.

In fact, equation (3.2), (3.3) and (3.4) can also apply to some situations in which the current source is added to the non-inverting opamp input as long as the input common-mode voltage of the opamp is fixed and not dependent on the input signals. This is illustrated by a state-variable filter for jω-axis zero [53] as shown in Figure3.2.

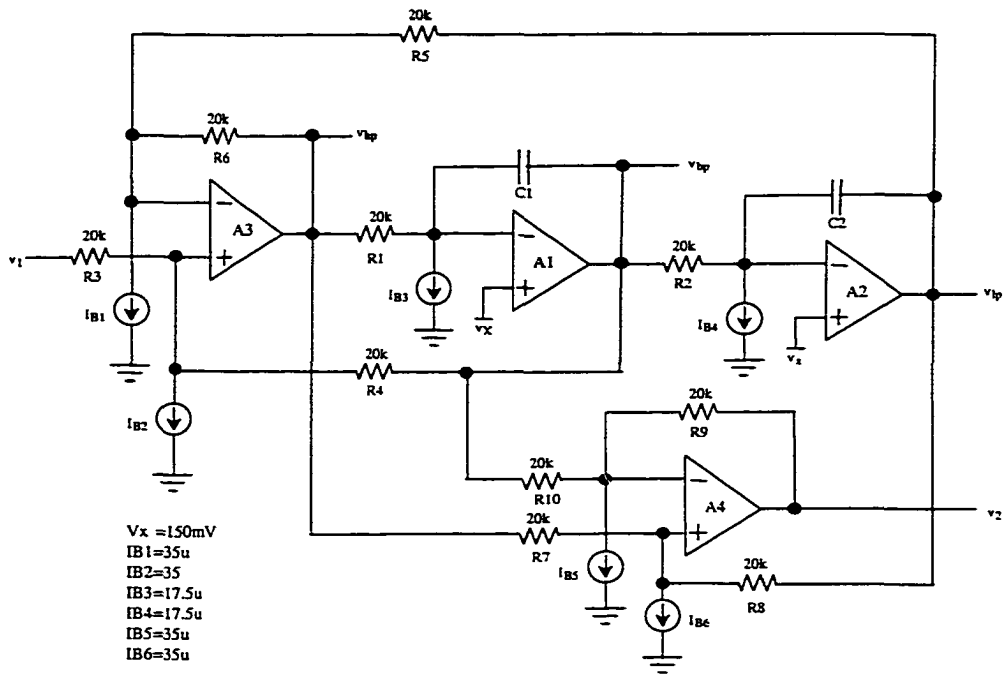


Figure 3.2 A low voltage state-variable filter for jω-axis zeros.

In this four-opamp filter, current sources are connected to the inverting inputs of opamp A1 and A2 and to both the inverting and the non-inverting inputs of opamp A3 and A4. An external reference voltage Vx (150mV) is used explicitly to set the input common-mode voltages for opamp A1 and A2. As there is no DC feedback path for opamp A1 and A2, V_{out_dc}(A3) and V_{out_dc}(A1) can be determined as $V_{DD}/2$ (0.5V) by the known values of R1, R2, IB3 and IB4 in Figure3.2 using the following equation:

$$V_{out\_dc} = R \cdot I_B + V_x \tag{3.5}$$

According to equation (3.3), the input common-mode voltage of opamp A3 can be implicitly determined as V_x using $V1_{in\_dc}$, V_{out_dc}(A1), R3 and R4. Therefore, V_{out_dc}(A2) can be set to $V_{DD}/2$ using equation (3.2). Similar derivations can be applied to opamp A4. Since all the input common-mode voltages and the output quiescent voltages of all opamps in the filter are set to V_x and $V_{DD}/2$ respectively, the filters is converted into a low voltage design with the proposed technique.

From the above analysis, it is expected that the proposed technique can be used in any single or multiple amplifier active RC filters when the input common mode voltages of the opamps are fixed.

Based on the same principle, another approach to bias the opamp input common-mode voltage is to use a resistor or a MOSFET operating in the triode region as shown in Figure 3.1(c). The resistance value of R_B can be determined as:

$$R_B = \frac{V_x}{\frac{V_{DD}}{2} - V_x}(R_f \,//\, R_{eq}) \tag{3.6}$$

The second approach has an advantage of setting v_x to a value lower than one V_{DSsat} (but greater than ground).

In general, both approaches can also be extended to convert a high voltage fully differential inverting opamp configuration into a low voltage design by adding biasing currents to both opamp inputs. In this case, the values of the biasing currents are required to be set according to the input and output common-mode voltages. However, if a current mismatch error ΔI_1 exits between the two biasing currents, a differential output offset voltage

$Vos=R_f\Delta I_1$ will appear at the output. In addition, for practical implementation, the values of the resistors may change due to process variations or temperature change. Therefore, the biasing currents are required to track with the changes in resistance. This will be further discussed in chapter 7 [51].

For any inverting opamp structures, adding current sources to the inverting inputs of opamps as shown Figure 3.1 (a) will induce minimal effects to the A.C response of the BIOS blocks since they are connected to the virtual grounds of the opamps. However, at high frequency, the bandwidths of the two schemes are different. The feedback factor β_i for the biasing scheme that uses current source can be determined as

$$\beta_i = \frac{R_{eq} // r_{ds}}{R_{eq} // r_{ds} + R_f} \tag{3.7}$$

where r_{ds} is the output resistance of the current source. The feedback factor β_r for the resistor scheme can also be expressed similar to (3.7) with r_{ds} changed to R_B. As observed from (3.6), R_B is usually smaller than R_{eq} and r_{ds}. Thus β_i will be larger than β_r and therefore, the scheme that uses current source will have a higher bandwidth given by $\beta_i \cdot f_t$ where f_t is the unity gain frequency of the opamp.

Nevertheless, using the proposed biasing schemes, any circuit that uses inverting opamp configuration such as some continuous time active RC filters can be converted into a low voltage design with a minimum supply voltage approximately equal to $3\ V_{DSsat} + V_t$. This reduction in supply voltage, however, comes with a price of increasing the overall noise.

For BIOS, as the added current source is connected to the virtual ground of the opamp, it will affect the noise performance of the circuit. If the current source is

implemented with an NMOS transistor M_1 as shown in Figure3.1 (b), the mean squared output noise can be derived as

$$v_{noise}^2 = \left(\frac{4KT}{R_{eq}} + \frac{4KT}{R_f} + I_n^2 \right) R_f^2 \frac{\omega_{-3dB}}{4} + v_{na}^2 \left(1 + \frac{R_f}{R_{eq} // r_{ds1}} \right)^2 \frac{\omega_{-3dB}}{4} \tag{3.8}$$

where ω_{-3dB} is the –3 dB frequency of the circuit that is equal to $\omega_T/[1 + R_f/(R_{eq}//r_{ds1})]$ for an opamp with unity gain frequency of ω_T. The effect of the capacitor in Figure 3.1 has been neglected in equation (3.8). The term I_n^2 is the noise current due to M_1 that can be derived as

$$I_n^2 = \frac{16KT}{3} \frac{V_{DD}/2 - V_x}{V_x (R_f \parallel R_{eq})} \tag{3.9}$$

if v_x is set equal to V_{DSsat1}. Although the term due to the equivalent input noise of the opamp v_{na}^2 is usually the dominant noise source for a typical design, the term due to I_n^2 may become significant when v_x becomes too small. If current source is implemented using a resistor, r_{ds1} is changed to R_B, and I_n^2 is due to the equivalent noise current of R_B that can also be described using (3.9) except that the scaling factor 16/3 is now equal to 4. And the term due to v_{na}^2 is usually the domain factor. Since $R_B < R_{eq} < r_{ds}$, the circuit shown in Figure3.1 (b) has lower noise than the circuit shown in Figure3.1(c). Furthermore, due to the term I_n^2, it has a slight higher noise than the case when either R_B or I_B is omitted. For example, if v_{na} = 50 nV/$\sqrt{Hz}$, $R_{eq} = R_f$ = 20 kΩ, V_{DD} = 1 V, v_x = 0.1 V, r_{ds} = 100 kΩ and T = 300 °K, v_{no} with I_B will be equal to 128 nV/$\sqrt{Hz}$, and v_{no} without I_B or R_B will be equal to 103 nV/$\sqrt{Hz}$. This corresponds to about 1.9 dB losses in SNR. Therefore, to minimize I_n^2, v_x cannot be too small. As a result, there is a slight tradeoff between the supply voltage and the noise performance.

Based on the above discussions, a continuous-time filter can be designed based on the proposed BIOS or BNIOS technique. However, the unity gain bandwidth of the opamp is limited due to the fact that only a relatively small V_{DSsat} is available at a low supply voltage. As a result, a suitable filter structure must be chosen to achieve high filter pole frequencies for a given unity gain bandwidth. In the literature, **Ackerberg-Mossberg (AM) biquad** is found to have better performance compared to other biquad structures such as Tow-Thomas biquad [54]. This is due to the fact that the phase lag of the inverting integrator is compensated by the phase lead of the noninverting integrator in the AM biquad. Generally, a filter pole frequency of 5 to 7 times less than the unity gain frequency of the opamp can be achieved.

Similar to Tow-Thomas biquad, the AM biquad is parasitic-insensitive filter architecture because all the capacitors are connected between the opamp virtual grounds and the opamp outputs and hence, they are insensitive to the parasitic capacitance to the ground. Since only inverting opamp configuration is required in the whole AM biquad, it is quite suitable to be implemented at low supply voltage using the above low supply voltage technique. The schematic of the low supply voltage AM biquad is shown in Figure3.3. The biquad is slightly modified from the original AM biquad in which C_B will be omitted and a resistor will be added in parallel with C_A in the first integrator to control the Q factor. The advantage of this modification is that it allows the tuning of the Q factor by adjusting the value of C_B only (instead of adjusting a resistor value) for a given value of C_A. Since if different Q factors were obtained by changing the resistor value, the value of the current source at the opamp input terminal is also needed to change according to equation (3.4) and hence, a more complicated tracking circuit design for the current sources will be required.

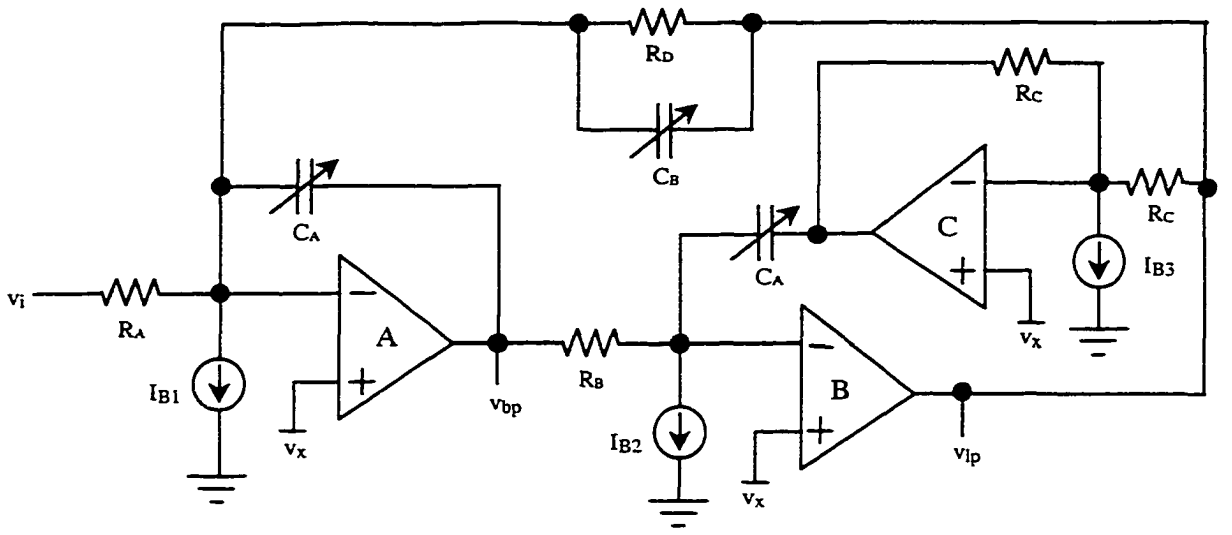


Figure 3.3 Low voltage modified Ackerberg-Mossberg biquad filter

The disadvantage of this modification is that the Q-tuning and frequency-tuning is not totally orthogonal and the tuning range for the Q factor will be dependent on the value of the pole frequency for given tuning ranges of C_A and C_B. The transfer functions for the low voltage filters in Figure 3.3 are derived as:

$$\frac{Vbp(s)}{Vi(s)} = -\frac{s/R_A C_A}{s^2 + s\dfrac{1/R_B C_A}{C_A/C_B} + 1/R_B R_D C_A^2} \tag{3.10}$$

$$\frac{Vlp(s)}{Vi(s)} = -\frac{1/R_A R_B C_A^2}{s^2 + s\dfrac{1/R_B C_A}{C_A/C_B} + 1/R_B R_D C_A^2} \tag{3.11}$$

If assuming R_A=R_B=R_D=R, ideally, the pole frequency ω_o and the Q factor of the biquad are given as $1/RC_A$ and C_A/C_B, respectively, and a tunable biquad can be designed with capacitors C_A and C_B as programmable capacitor arrays (PCAs). PCAs have both area and frequency advantages over other types of passive component arrays [42]. However, for

low supply voltage, the switch in series with each capacitor in the PCAs may not be able to pass voltage at the middle of the supply rails even if transmission gate is used as discussed in section 2.2.3. This has been addressed in detail in [3][12][13][14][23]. Fortunately, based on the above low voltage technique, the quiescent voltages of the PCA terminals that are connected to the negative opamp input terminals are equal to v_x. Therefore, by placing NMOS switches in series with the capacitors at these terminals, the switches will have sufficient overdrive voltage, which is equal to

$$V_{OV} = V_{DD} - V_m - V_x \tag{3.12}$$

For a 1 V power supply and $V_m \approx 0.6$ V, the overdrive voltage is between 0.2 V and 0.3 V.

NMOSs with minimum channel length are used for the switches in the PCAs. These switches introduce parasitic resistance and capacitance into the circuit. The parasitic resistance combined with the feedback capacitor in the integrator will produce a parasitic zero, which may alter the transfer function of the filter. In our design, this parasitic zero has been placed more than an order of magnitude higher than ω_o by choosing proper transistor widths. However, increasing the transistor widths will increase the parasitic capacitance to the opamp inputs. As a result, it may degrade the phase margin of the closed-loop opamp response and may affect the overall stability. All these effects must be carefully considered and simulated during the design phase. Furthermore, the active compensated circuits in the AM biquad may have stability problem. To ensure stability problem, HSPICE simulation is employed. Simulation results show that the phase margins of the loop consisting of opamp B and C, Ca, Rb and Rc are 77° and 96° respectively when all of NMOS switches in PCA Ca are OFF and ON, respectively.

3.4 Summary

A low voltage design technique for continuous-time active RC filters is proposed in this chapter. The minimum required supply voltage is achieved by adding extra current sources or resistors at the opamp inputs to set the opamp input common-mode voltages close to one of the supply rails. Detail procedure for applying this technique, noise analysis and AC analysis are presented. The effect of input offset voltages to differential circuits caused by current source mismatch to the filter, the possible stability problem caused by active compensation technique and the effects of low voltage switches in PCA to the AC response of the filter have been briefly discussed. This low voltage continuous-time filter technique can achieve high linearity with close to rail-to-rail output signal swing. When realized in a conventional sub-micron CMOS process, continuous-time filters with frequency range of a few MHz to tens of MHz are possible.

CHAPTER 4 ON-CHIP AUTOMATIC TUNING TECHNIQUES FOR LOW VOLTAGE ACTIVE RC FILTERS

An on-chip automatic frequency and Q tuning technique suitable for low voltage continuous-time active RC filter is presented in this chapter. By changing the values of the programmable capacitor arrays (PCAs), the filter can be tuned to the desired frequency response and the desired Q factor. The proposed tuning technique does not require any peak detectors, which are difficult to implement at low-voltage. Instead, it uses a few analog comparators, a digital comparator and a few binary counters to adjust the PCAs.

4.1 Introduction

To account for process variations and environment influences, calibration circuits for tuning the RC time constants of an active RC filter have been proposed [42][43] [55]. Usually, frequency and Q tuning is desired to account for the non-ideal integrator effects when the center or the cut-off frequency of the filter is near the opamp unity gain frequency. For Gm-C or MOSFET-C filters, tuning techniques have been proposed but they may not be suitable for tuning active RC filters using PCAs. Furthermore, peak detectors are usually needed in the Q tuning circuit [39]. However, peak detectors are difficult to implement for low supply voltage (1V). In this section, automatic frequency and Q tuning techniques are proposed for low voltage active RC filters using PCAs and no peak detectors are required. In

chapter 6, the practical design of a 1V second order filter with on-chip automatic frequency and Q tuning will be discussed.

When the desired center frequency and/or cut-off frequency ω_o is close to the unity gain frequency of the opamp, the value of ω_o will deviate from $1/RC_A$ due to the effect of finite opamp bandwidth. In addition, the product of R and C_A can be varied from the nominal value due to process variations and temperature changes. To tune the filter to the desired ω_o and Q factor, an on-chip automatic tuning circuit is required. For Gm-C and MOSFET-C filters, a conventional tuning circuit based on VCO as shown in Figure 4.1 is widely used [39].

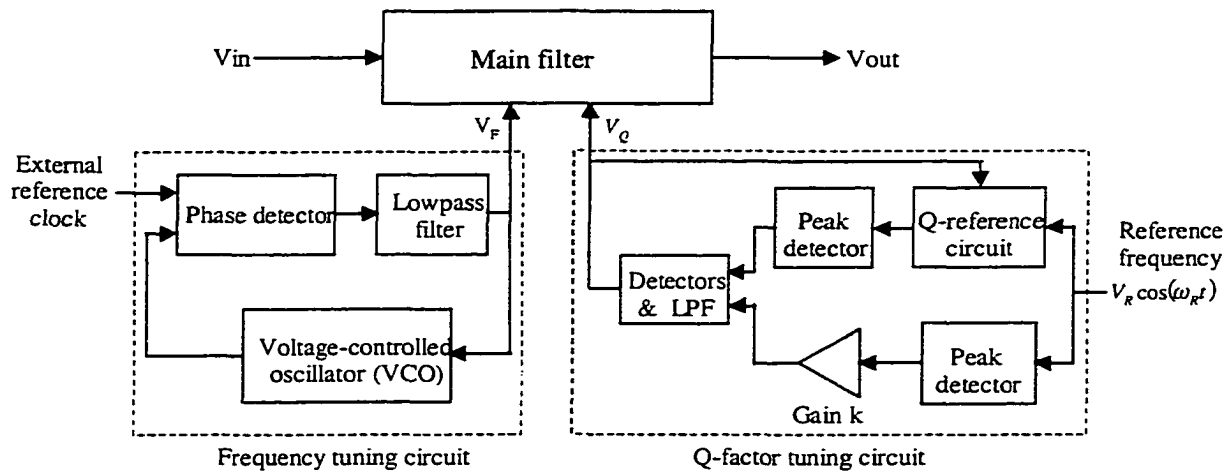


Figure 4.1 Conventional frequency and Q tuning circuit based on VCO

However, this tuning circuit is not suitable to tune active RC filter with PCAs. First, the output of the loop filter in the PLL and the output of the Q control loop are analog voltages, which cannot be interfaced directly with the PCAs. Second, it is difficult to realize the peak detectors used in the Q control loop with reasonable output signal swing at low

supply voltage (1 V) since any peak detectors using diodes or MOSFETs will have voltage drops of at least 0.6 to 0.8 V from the peak input value. This will cost a large part of the voltage headroom for a low voltage design.

4.2 Frequency Tuning Technique

The proposed automatic tuning circuit for the low voltage active RC biquad is shown in Figure 4.2 [47] [56]. The frequency-tuning loop consists of the oscillator, the reference filter, the analog comparator 1, the m-counter, the digital comparator and the f-counter. The analog comparator 1 is for converting the sine wave signal from the oscillator to a square wave signal to drive the m-counter. It can be realized as a simple pseudo NMOS inverter.

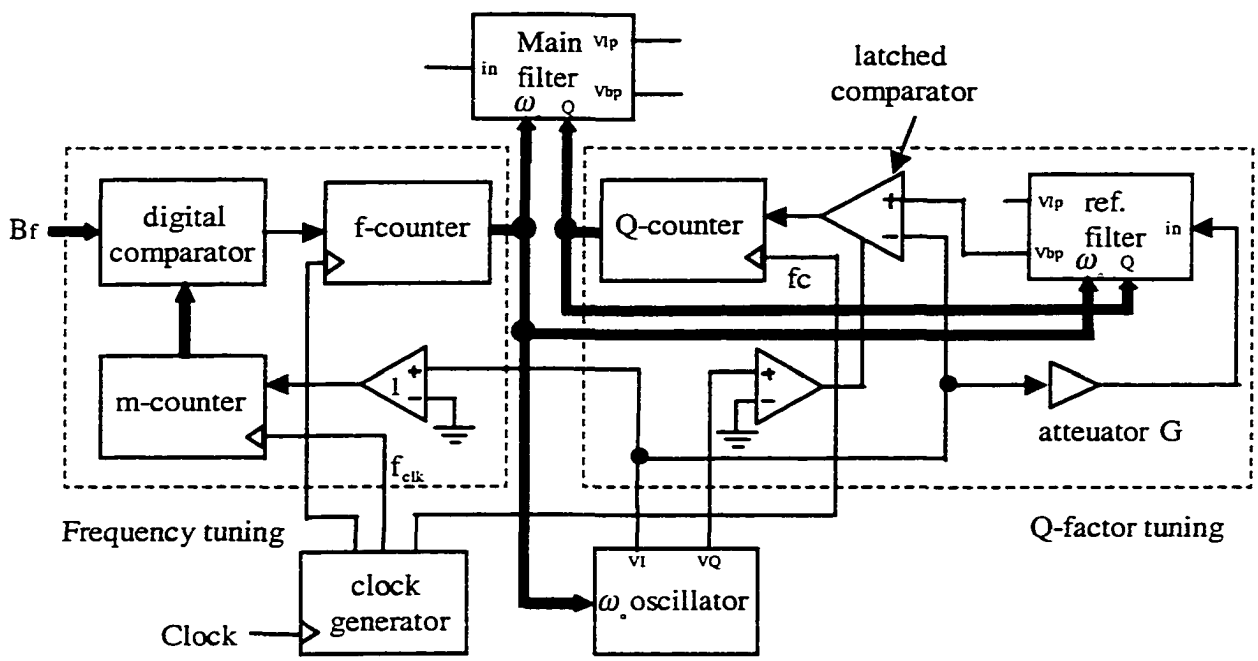


Figure 4.2 Proposed automatic tuning circuits for the low-voltage active RC biquad

The oscillator is realized as the biquad shown in Figure 3.3 with the damping capacitor C_B is removed. Since the Q factor is infinite ideally, the in-phase output v_I (v_{bp} in Figure 3.3) and the quadrature-phase output v_Q (v_{lp} in Figure 3.3) of the oscillator will oscillate at ω_o. Therefore, by tuning the oscillation frequency f_{osc} of the oscillator, ω_o can be tuned. f_{osc} is first measured by the m-counter, which is controlled by an reference clock signal f_{clk}. The value of the m-counter is latched at the end of each clock period T_{clk} and then compared with the digital input word B_f using the digital comparator. When the value of the m-counter is less (greater) than B_f, this indicates that f_{osc} is lower (higher) than the desired value. Then the f-counter that controls all the PCA C_A's will decrement (increment) by 1. When the value of the m-counter is equal to B_f, f_{osc} reaches the desired value and the f-counter will remain unchanged. Ideally, f_{osc} will be equal to $B_f f_{clk}$. Hence, the desired ω_o is:

$$\omega_\circ = 2\pi B_f f_{clk} \tag{4.1}$$

However, due to the error from measuring f_{osc} and the finite PCA resolutions, ω_o may deviate from the ideal value. The percentage of error from measuring f_{osc} can be shown to be

$$\left|\frac{f_{meas} - f_{osc}}{f_{osc}}\right| \le \frac{f_{clk}}{f_{osc}} \tag{4.2}$$

Therefore, the reference clock signal should have a relatively long period together with a long m-counter to minimize this error. If the PCA C_A is realized as a fixed capacitor of C_{Amin} in parallel with a n-bit binary weighed PCA and with C_{Au} as the unit capacitor in the PCA, then the percentage of error on ω_o due to finite PCA resolution can be shown to be

$$\left|\frac{\omega - \omega_\circ}{\omega_\circ}\right| < \frac{C_{Au}}{C_{Amin}} \qquad \text{at } \max\{\omega_o\} \tag{4.3}$$

and $$\left|\frac{\omega-\omega_o}{\omega_o}\right| < \frac{C_{Au}}{C_{Amin}+2^n C_{Au}} \quad \text{at } \min\{\omega_o\} \tag{4.4}$$

As a result, a high resolution PCA with a small ratio between C_{Au} and C_{Amin} is required to improve the accuracy without scarifying the tuning range.

Similar to the conventional frequency-tuning scheme that uses a PLL, the frequency-tuning accuracy of the proposed tuning technique is strongly dependent on having a good match between the oscillating frequency f_{osc} and the center frequency of the filter ω_o.

Another factor that may cause systematic errors in frequency tuning is the relationship between oscillating frequency and oscillating magnitude. In order to have a good matching between f_{osc} and f_o, the oscillating amplitude range must be within the opamp's output range.

Some simulation results will be presented in chapter 7 for the above two problems.

4.3 Q Factor Tuning Technique

After ω_o has been tuned to the desired value, the Q factor of the main filter is tuned by first passing the in-phase output of the oscillator v_I to an attenuator with a gain of G and then on to the input of the reference filter. Ideally, when v_I is at ω_o, the bandpass output of the reference filter v_{bp} is equal to $-GQv_I$ where Q is the filter Q factor. If Q is equal to 1/G, then the magnitude of v_{bp} will be equal to the magnitude of v_I. Therefore, Q tuning can be achieved by comparing the magnitudes of v_I and v_{bp}, and then adjusting PCA C_B's until the magnitudes of v_I and v_{bp} are equal. Unfortunately, peak detectors for storing the magnitudes

of v_I and v_{bp} are difficult to design at low supply voltage. To avoid the use of peak detectors, we propose to use a latched comparator to compare v_I and v_{bp} at their peak values. Since the oscillator provides in-phase and quadrature-phase outputs, the quadrature-phase output v_Q can be used as the latch signal for the latched comparator after v_Q goes through an analog comparator (implemented by an pseudo NMOS inverter) as shown in Figure 4.2. The output of the latched comparator is then fed to the Q-counter, which controls the values of the PCA C_B's. When v_{bp} is higher than v_I, the value of the Q-counter will increment by one and vice versa. The updating rate of the Q-counter is determined by an external clock signal f_c. A slow update rate is preferred to allow v_{bp} settle to the steady state after each Q adjustment such that an accurate comparison can be made between v_I and v_{bp}. When v_{bp} and v_I is equal, the desired Q factor is:

$$Q = \frac{1}{G} \tag{4.5}$$

As a result, the output of the latched comparator will fluctuate between high and low, and the values of the C_B's will change back and forth from one value to another. This may cause some undesired noise at the main filter output. If the value of the Q-counter is latched after some period of time, this effect can be greatly eliminated. Alternatively, a simple digital detector that detects a sequence of alternating 1's and 0's can also be used for checking this state and stop the Q-counter.

According to the filter structure, the tuning range of the Q factor depends on ω_o and the range of C_B since Q can be written as

$$Q = 1/(\omega_o R C_B) \tag{4.6}$$

Therefore, for a fixed range of C_B, the maximum achievable Q factor decreases when ω_o

increases. On the contrary, the minimum achievable Q factor increases when ω_o decreases. If the PCA C_B's can be written as $C_{Bmin} + 2^L C_{Bu}$ where C_{Bmin} and C_{Bu} are two different constant capacitance, then C_{Bu}/C_{Bmin} should be small and the value of L should be large enough to achieve a high Q tuning accuracy and a wide Q factor tuning range. In addition, unlike other Q tuning schemes that use peak detectors, the accuracy of the proposed scheme is affected by any undesired phase shift of the attenuator. In addition, when the input frequency of the reference filter $2\pi f_{osc}$ is slightly deviated from the bandpass filter center frequency ω_o, the filter output phase will deviate from the idea phase output and it will produce a similar effect caused by the phase shift of the attenuator. The effect caused by the phase shift of the attenuator is illustrated in Figure 4.3.

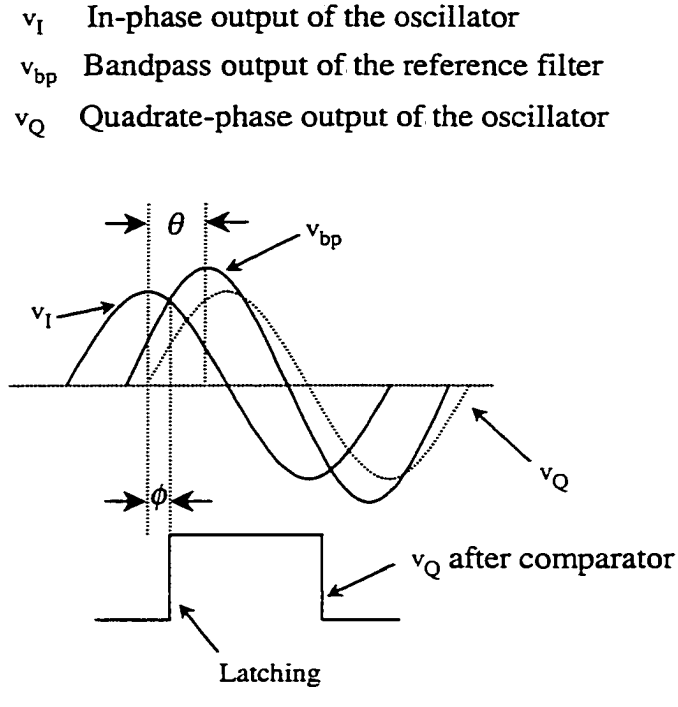


Figure 4.3 Proposed Q-factor tuning technique for low-voltage active RC biquad

When the attenuator has a phase shift of θ radians relative to v_I, the phase shift of the reference filter output v_{bp} is also equal to θ approximately. If the latched comparator latches according to v_Q but have a delay of ϕ radians relative to the peak value of v_I due to some delays, the Q tuning loop will force the instantaneous values of v_I and v_{bp} at ϕ radians after the peak value of v_I to be the same. As a result, the actual magnitudes of v_{bp} and v_I will not be equal and the actual Q factor after tuning Q_{actual} becomes

$$Q_{actual} = \frac{\cos(\phi)}{\cos(\phi - \theta)G} \tag{4.7}$$

From the above equation, it is interesting to observe that even if the comparator has a delay, Q_{actual} will be equal to the desired value (1/G) when the attenuator has no phase shift (i.e. θ = 0). For less than 2 % error on the Q factor, θ and ϕ must be less than 10°. These requirements can usually be achieved using an on-chip attenuator and a reasonable performance latched comparator if the frequency of v_I, which is at ω_o, is less than tens of MHz.

4.4 Summary

In this chapter, a digital tuning technique with PCAs for tuning the frequency and the Q-factor of low voltage active RC filters is proposed. A low-voltage latched comparator is used for detecting and comparing the peak values of the reference filter output and the oscillator output. As a result, no accurate peak detector is required. The above techniques can be used in the design of low voltage (down to 1V) continuous-time filters in a standard CMOS process without using any other extra process step or on-chip voltage multiplier.

CHAPTER 5 DIRECT BACKGROUND DIGITAL TUNING TECHNIQUE FOR CONTINUOUS-TIME SIGMA-DELTA MODULATOR

5.1 Introduction

In the past few years, oversampling discrete time [57] [58] and/or continuous time (CT) [59] [60] [61] band pass A/D converters based on sigma-delta ($\Sigma\Delta$) modulation have been widely used to robustly digitize the narrow band intermediate frequency (IF) signals that arise in radios and cellular systems. Digitization of the IF signal directly brings several advantages in a receiver, including greater reliability, potentially lower power consumption, and improved performance as technology scales. Furthermore, by converting analog signal to digital signal at the IF location, the problems of low frequency (1/f) noise and dc offset are avoided.

CT $\Sigma\Delta$ modulator has an advantage of achieving potentially higher sampling ratio due to the absence of input sampling and settling requirements. In addition, it contains an implicit anti-alias filtering in comparison to the discrete-time modulator, which is a significant advantage for bandpass A/D conversion. However, CT $\Sigma\Delta$ modulator is vulnerable to clock jitter. Furthermore, excess loop delay between the quantizer clock edge and the time when a change in output bit is seen at the feedback point in the modulator can cause stability problems.

When designing a continuous-time sigma-delta modulator with the popular $\frac{1}{4}f_s$ method, the expected resonating frequency of the continuous time bandpass filter used in the

modulator is at $f_s/4$, where f_s is the sampling frequency for the comparator, is or the equivalent discrete-time notch center frequency for the quantization noise is right at $f_s/4$. Figure 5.1 shows a block diagram of a continuous-time sigma-delta bandpass (CT BP ΣΔ) modulator with a single bit quantizer.

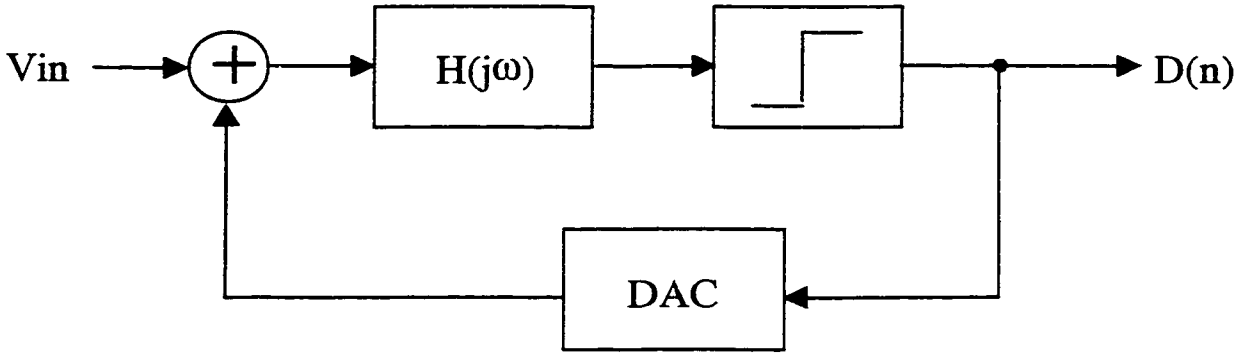


Figure 5.1 Continuous-time bandpass ΣΔ modulator

The CT BP filter H(jω) is assumed to have an ideal center frequency of ω_o. As the resonators used in continuous-time sigma-delta modulators are always designed with some on-chip or off-chip components such as gm-C, L-C and RC, the transfer function of the resonator will vary a lot due to the changes of gm, L, R and C along with process and temperature variations. If the actual notch center frequency for the quantization noise ω_{oa} is away from ω_o by some $\Delta\omega$ due to process and temperature variations, the SNR at the modulator output D(n) will be degraded for a fixed input signal bandwidth BW. This effect is illustrated in Figure 5.2. The x-axis expresses the percentage difference of the actual notch frequency relative to the desired frequency.

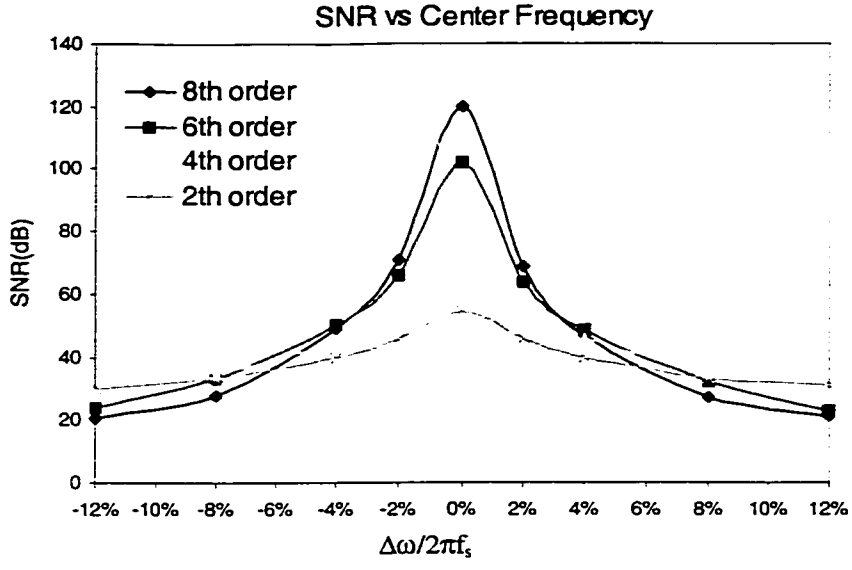


Figure 5.2 SNR versus the percentage difference of the actual notch frequency relative to the desired frequency.

In these simulations, a single tone at $f_s/4$ with amplitude of 0.6 is used as the input and a series of 32768-point FFTs is performed. The BW is assumed to be $f_s/200$ centered at ω_o, which is equal to $f_s/4$ where f_s is the sampling frequency. When $\Delta\omega$ is equal to zero, the modulator has a maximum SNR determined by the order of the BP filter. When ω_{oa} is not equal to ω_o, the SNR starts to degrade, especially for high order modulators where a slightly shift in center frequency results in a significant degradation in SNR. For a 2^{nd} $\Sigma\Delta$ modulator, a 2% error for the notch frequency leads to around 10dB loss. Thus, tuning is generally required for CTBP $\Sigma\Delta$ modulators and especially for high-speed operation. A more detail analysis on the degradation of SNR will be presented in section 5.2.3.

One of the major challenges of tuning the center frequency of CTBP $\Sigma\Delta$ modulator is that it is not easy to check the spectrum characteristic of the output bit stream in real time. Although some methods have been proposed, generally, complicated hardware is needed to

calculate FFT. Another challenge is that tuning circuits will add complexity to the sigma-delta system and possibly will produce some unwanted noise especially for high-speed ΣΔ modulators.

Several tuning methods are proposed for the filters in continuous-time ΣΔ modulators in the literature. One of them is the master-slave approach [59]. This technique is very similar to the conventional frequency-tuning scheme for continuous time filters and thus it strongly depends on the frequency matching between the master filter and the slave filter. The best accuracy with this technique is often within 2%. A much better tuning accuracy can be achieved if a direct tuning scheme can be used [62]. However, extra DAC and/or ADC may be required to tune the CT filter, and the normal operation of the modulator may need to interrupt during the tuning phase.

In this chapter, a new direct tuning scheme is proposed for CT BP ΣΔ modulator. It does not require any extra analog components. It only requires information from the modulator digital output that is extracted in the background by directly processing the digital output without the need to interrupt the normal operation of the modulator. It estimates the noise power density at two frequency locations and then update some filter parameters according to the relation of the two estimated noise power densities. All operations for the proposed technique are done in digital domain.

5.2 Proposed Digital Tuning Technique

This tuning technique can be understood by first considering the output spectra of the modulator for different ω_{oa}'s as shown in Figure 5.3. n_A and n_B are the modulator output

power spectral densities at points A and B, which have frequencies at ω_A and ω_B, respectively. The points A and B are assumed to be symmetrical about the desired center frequency ω_o and outside the input signal bandwidth BW.

Assume that (a) the quantizer output noise is white and signal independent; (b) the magnitude of the noise transfer function of the modulator is symmetric around the center frequency ω_{oa} (i.e. $|NTF(j(\omega_{oa} + \omega_x))| = |NTF(j(\omega_{oa} - \omega_x))|$) where $\omega_x < \omega_{oa}$ for different ω_{oa}; (c) there are no signal energy at ω_A and ω_B. Assumption (b) is usually valid for choosing $2\pi\omega_o = \frac{1}{4} f_S$ with a small ω_x [63] and for high order modulators with a high Q BP filter as well as a large oversampling ratio. Therefore, for $\omega_{oa} = \omega_o$, the noise spectral densities at points A and B, given as n_A and n_B will be equal as illustrated in Figure 5.3(a). For $\omega_{oa} < \omega_o$, n_A will be less than n_B as shown in Figure 5.3(b). Similarly, n_A will be greater than n_B for $\omega_{oa} > \omega_o$ as shown in Figure 3(c). Therefore, the location of ω_{oa} can be estimated by knowing the difference between n_A and n_B.

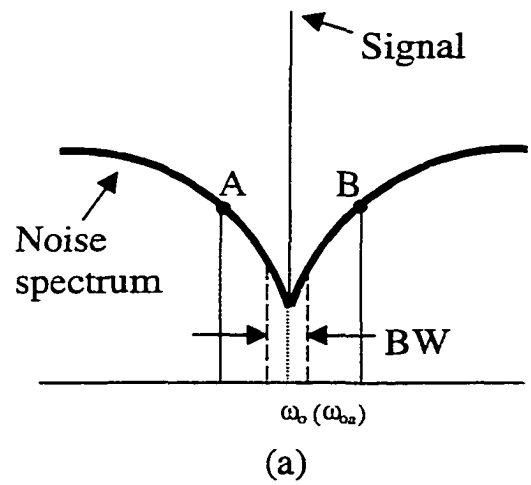
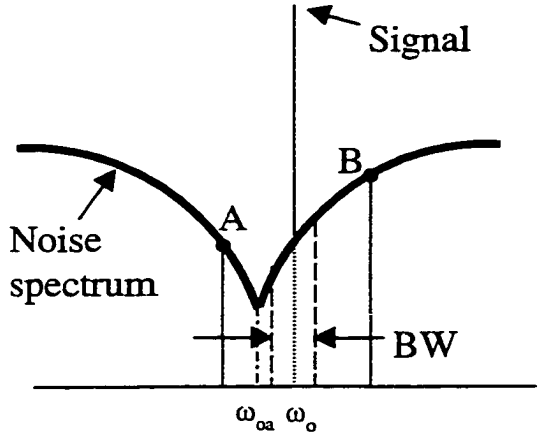
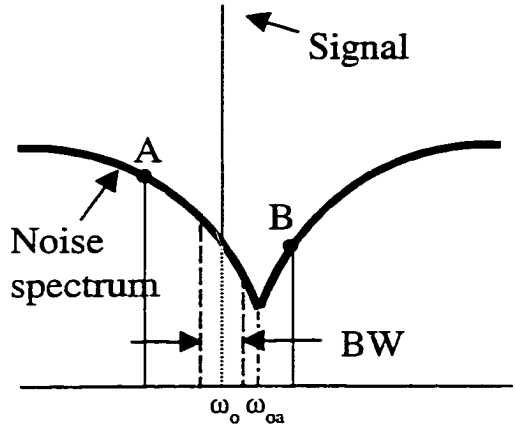


Figure 5.3 Conceptual output spectrum (a) $\omega_{oa} = \omega_o$ (b) $\omega_{oa} < \omega_o$ (c) $\omega_{oa} > \omega_o$



(b)



(c)

Figure 5.3 (Continued)

If we further assume that ω_{oa} is a monotonic function of a tuning code or a tuning voltage/current given as tc(i) where i is the iteration step, then we can tune the notch frequency using the following updating formula

$$tc(i+1) = tc(i) - \mu(n_A - n_B) \qquad \textbf{(5.1)}$$

where μ is a constant, which affects the time constant for convergence and the stability of tuning.

A simple way to implement equation (5.1) is to use a binary up/down counter as discussed in chapter 4. In this case, the updating equation will become

$$tc(i+1) = tc(i) - \mu(n_A - n_B)/|n_A - n_B| \qquad (5.2)$$

There are several advantages for the proposed tuning technique. First, there is no stimulus required to inject to the modulator input and hence, no extra DAC is required. Second, n_A and n_B can be directly measured from the modulator digital output using digital signal processing (DSP) techniques and therefore, no extra ADC is required. In addition, n_A and n_B can be measured on the background. In the section 5.3, simple techniques for estimating n_A and n_B are discussed.

5.2.1 System convergence condition and convergence time constant

Assume that (a) $\omega_{oa}(i) = K \cdot tc(i)$; (b) the noise spectral density of the quantizer is equal to δ^2; (c) $NTF(j\omega, \omega_o) = NTF(j\omega)$ is the ideal noise transfer function after tuning and $NTF(j\omega, \omega_i)$ is the untuned transfer function at tuning step i as shown in Figure 5.4; (d) the estimation of the spectral densities at ω_A and ω_B has no error; (e) the initial $\omega_{oa} = \omega_o'$ is close to ω_o.

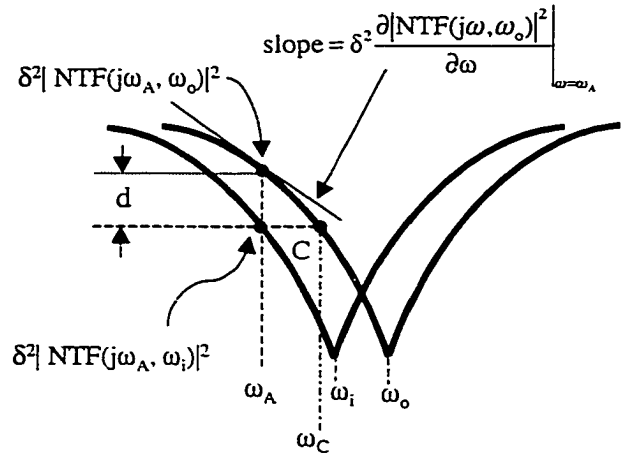


Figure 5.4 Derivation of convergence constant

It can be seen from Figure 5.4, at point C, $\delta^2|NTF(j\omega_C, \omega_o)|^2=\delta^2|NTF(j\omega_A, \omega_i)|^2$ and $\omega_C-\omega_A\approx\omega_o-\omega_i$. Assume ω_i is close to ω_o, for the first order approximation,

$$\delta^2 \mid NTF(j\omega_C,\omega_o) \mid^2 \approx \delta^2 \mid NTF(j\omega_A,\omega_o) \mid^2 +(\omega_C-\omega_A)\delta^2 \frac{\partial|NTF(j\omega,\omega_o)|^2}{\partial\omega}\Bigg|_{\omega=\omega_A}$$

$$\approx \delta^2 \mid NTF(j\omega_A,\omega_o) \mid^2 +(\omega_o-\omega_i)\delta^2 \frac{\partial|NTF(j\omega,\omega_o)|^2}{\partial\omega}\Bigg|_{\omega=\omega_A} \qquad \textbf{(5.3)}$$

The noise power density difference between point A and point C, d, can be written as

$$d = \delta^2|NTF(j\omega_A, \omega_o)|^2 - \delta^2|NTF(j\omega_A, \omega_i)|^2$$

$$= \delta^2|NTF(j\omega_A, \omega_o)|^2 - \delta^2|NTF(j\omega_C, \omega_o)|^2$$

$$\approx \delta^2|NTF(j\omega_A, \omega_o)|^2 - \delta^2|NTF(j\omega_A, \omega_o)|^2 - (\omega_o-\omega_i)\delta^2 \frac{\partial|NTF(j\omega,\omega_o)|^2}{\partial\omega}\Bigg|_{\omega=\omega_A}$$

$$= -(\omega_o-\omega_i)\delta^2 \frac{\partial|NTF(j\omega,\omega_o)|^2}{\partial\omega}\Bigg|_{\omega=\omega_A} \qquad \textbf{(5.4)}$$

By dropping ω_o, equation (5.4) can be written as

$$d \approx -(\omega_o-\omega_i)\delta^2 \frac{\partial|NTF(j\omega)|^2}{\partial\omega}\Bigg|_{\omega=\omega_A} \qquad \textbf{(5.5)}$$

Due to the assumption (b) in the previous section, it is easy to see the noise power density difference between point A and point B is

$$n_A-n_B = 2d \approx -2(\omega_o-\omega_i)\delta^2 \frac{\partial|NTF(j\omega)|^2}{\partial\omega}\Bigg|_{\omega=\omega_A} \qquad \textbf{(5.6)}$$

Using the assumption (a) in this section, equation (5.1) can be written as

$$\omega_{i+1} = \omega_i - \mu K(n_A - n_B)$$

$$\approx \omega_i + 2\mu K(\omega_o - \omega_i)\delta^2 \left.\frac{\partial|NTF(j\omega)|^2}{\partial\omega}\right|_{\omega=\omega_A} = \omega_i + \mu\lambda(\omega_o - \omega_i) \qquad (5.7)$$

where $\lambda = 2K\delta^2 \left.\frac{\partial|NTF(j\omega)|^2}{\partial\omega}\right|_{\omega=\omega_A}$

Rearrange equation (5.7),

$$\omega_{i+1} \approx (1+\mu\lambda)\omega_i + \mu\lambda\omega_o \qquad (5.8)$$

Assume the initial value of the notch frequency is at ω_o', the notch frequency at tuning step i can be obtained as

$$\omega_{i+1} \approx (1+\mu\lambda)^i\omega_o' + [1-(1+\mu\lambda)^i]\,\omega_o \qquad (5.9)$$

According to equation (5.9), for convergence of the proposed tuning system, two conditions must be met: $(1+\mu\lambda)^i$ close to zero and ω_i close to ω_o when i goes to infinite. This requires $|1+\mu\lambda|\leq 1$ or the condition for convergence can be approximated as

$$\left|1 + 2\mu K\delta^2 \left.\frac{\partial|NTF(j\omega)|^2}{\partial\omega}\right|_{\omega=\omega_A}\right| \leq 1 \qquad (5.10)$$

where the derivative of $|NTF(j\omega)|^2$ at $\omega = \omega_A$ is assumed to be equal to the negative value of the derivative of $|NTF(j\omega)|^2$ at $\omega = \omega_B$. For high order modulator, a small μ should be used since the derivatives of $|NTF(j\omega)|^2$ at $\omega = \omega_A$ or ω_B can be quite large. The time constant for convergence can be then derived as [64]

$$\tau = \frac{T_{update}}{4\mu\lambda} \qquad (5.11)$$

where T_{update} is the required time for each tuning step.

5.2.2 Variance of the tuned notch frequency

In practice, due to the error in estimating noise power density, after the system converges, there are still some very small fluctuations for the tuned notch frequency. Assume that e_i is the combined error on the estimations of n_A and n_B, equation (5.8) can be rewritten as

$$\omega_{i+1} \approx (1+\mu\lambda)\omega_i + \mu\lambda\omega_o - \mu K e_i \tag{5.12}$$

A general equation for ω_i can be approximated as:

$$\omega_{i+1} \approx (1+\mu\lambda)^i\omega_o + \mu\lambda\omega_o \sum_{j=0}^{i-1}(1+\mu\lambda)^{j} + \mu K \sum_{j=0}^{i-1} e_j (1-\mu\lambda)^j$$

$$\approx \omega_o + \mu K \sum_{j=0}^{i-1} e_j (1+\mu\lambda)^j \tag{5.13}$$

Thus, the co-variance of the tuned notch frequency can be expressed as

$$E[(\omega_i-\omega_o)^2] \approx \mu K \cdot E[(\sum_{j=0}^{i-1} e_j (1+\mu\lambda)^j)^2]$$

$$= \mu K E[e_0^2(1+\mu\lambda)^0 + e_1^2(1+\mu\lambda)^1 + e_2^2(1+\mu\lambda)^2 + \ldots]$$

$$\approx \mu K \cdot E[e^2] \sum_{j=0}^{i-1}(1+\mu\lambda)^j \tag{5.14}$$

When i is equal to infinite,

$$E[(\omega_i-\omega_o)^2] \approx \mu K \cdot E[e^2] \frac{1}{1+\mu\lambda}$$

$$\approx \mu K \cdot E[e^2](1-\mu\lambda) \tag{5.15}$$

With equation (5.15), we can approximately predict what value of μ should be used if the specification for the allowable variations on ω_{oa} is known and $E[e^2]$ can be estimated.

5.2.3 In-band noise power for a deviated notch frequency

In this section, the degradation on SNR for ω_{oa} slightly deviated from the ideal ω_o is analyzed. Based on this analysis, one can predict the allowable range of ω_{oa} and hence the acceptable value for μ.

Assume that an ideal discrete time signal transfer function $\frac{-z^{-2}}{1+z^{-2}}$ can be achieved for a 2nd order sigma-delta modulator and there is a pair of zeros for the noise transfer function, the equivalent noise transfer function can be written as

$$NTF(Z) = (Z-Z_1)(Z-Z_2)/Z^2 \qquad \textbf{(5.16)}$$

where $Z = e^{j2\pi f/f_s}$ and f_s is the sampling frequency.

The zeros Z_1 and Z_2 will be on the unit circle ideally and they have a form given as $Z = e^{j2\pi fa/f_s}$, where f_a is the actual location of the zero or the untuned notch frequency. When Z_1 and Z_2 are at the ideal location, $Z_{1ideal} = e^{j2\pi fo/f_s}$ and $Z_{2ideal} = e^{-j2\pi fo/f_s}$.

Now substitute $Z = e^{j2\pi f/f_s}$ into (5.16) and assumed f is close to f_a. Then,

$$NTF(e^{j2\pi f/f_s}) \approx (e^{j2\pi f/f_s} - e^{j2\pi fa/f_s})/(e^{j4\pi f/f_s}) \qquad \textbf{(5.17)}$$

For an N-th order modulator with all the zeros located at the same locations ($e^{j2\pi fa/f_s}$ and $e^{-j2\pi fa/f_s}$)

$$NTF(e^{j2\pi f/f_s}) \approx (e^{j2\pi f/f_s} - e^{j2\pi fa/f_s})^{N/2}/(e^{j2N\pi f/f_s}) \qquad \textbf{(5.18)}$$

where N is the order of the modulator and it is an even number.

Assume that $\Delta f = f - f_a$,

$$NTF(e^{j2\pi f/f_s}) \approx (e^{j2\pi(\Delta f+fa)/f_s} - e^{j2\pi fa/f_s})^{N/2}/(e^{j2N\pi f/f_s})$$

$$\approx e^{j2\pi\frac{N}{2}fa/f_s}(e^{j2\pi\Delta f/f_s}-1)^{N/2}/(e^{j2N\pi f/f_s}) \tag{5.19}$$

Assume $\Delta f << f_s$, $NTF(e^{j2\pi f/f_s}) \approx e^{j2\pi\frac{N}{2}fa/f_s}(j2\pi\frac{\Delta f}{f_s})^{N/2}/(e^{j2N\pi f/f_s})$

$$|NTF(e^{j2\pi f/f_s})| \approx |2\pi\frac{f-f_a}{f_s}|^{N/2} \tag{5.20}$$

Assume BW_2=BW/2, the total noise power within BW is

$$Pe = \int_{fo-BW_2}^{fo+BW_2} Se^2|NTF(e^{j2\pi f/f_s})|^2 df \approx \int_{fo-BW_2}^{fo+BW_2} Se^2|2\pi\frac{f-f_a}{f_s}|^N df \tag{5.21}$$

where Se is the noise spectral density of the quantizer.

$$Pe \approx Se^2(\frac{2\pi}{f_s})^N[\int_{f_a}^{fo+BW_2}(f-f_a)^N df + \int_{fo-BW_2}^{f_a}(f-f_a)^N df]$$

$$\approx Se^2(\frac{2\pi}{f_s})^N\frac{1}{N+1}[(f-f_a)^{N+1}\Big|_{f_a}^{fo+BW_2} + (f-f_a)^{N+1}\Big|_{fo-BW_2}^{f_a}]$$

$$\approx Se^2(\frac{2\pi}{f_s})^N\frac{1}{N+1}[(f_o+BW_2-f_a)^{N+1}-(f_o-BW_2-f_a)^{N+1}]$$

Define the difference between the ideal notch frequency and the untuned frequency as $\Delta f_o = f_o - f_a$

$$Pe \approx Se^2(\frac{2\pi}{f_s})^N\frac{1}{N+1}[(BW_2+\Delta f_o)^{N+1}+(BW_2-\Delta f_o)^{N+1}] \tag{5.22}$$

For N=2,

$$Pe \approx Se^2(\frac{2\pi}{f_s})^2\frac{1}{3}(BW_2^3+3BW_2^2\Delta f_o+3BW_2\Delta f_o^2+\Delta f_o^3+$$

$$BW_2^3-3BW_2^2\Delta f_o+3BW_2\Delta f_o^2-\Delta f_o^3)$$

$$\approx Se^2(\frac{2\pi}{f_s})^2\frac{1}{3}(2BW_2^2+6BW_2\Delta f_o^2)$$

where $6BW_2\Delta f_o^2$ is the excessive noise due to notch not at the ideal location.

Similarly, for N=4,

$$Pe \approx Se^2(\frac{2\pi}{f_s})^4\frac{1}{5}(2BW_2^5+20BW_2^3\Delta f_o^2+10BW_2\Delta f_o^4)$$

where $20BW_2^3\Delta f_o^2 + 10BW_2\Delta f_o^4$ is the excessive noise. The term $10BW_2\Delta f_o^4$ can be neglected when $BW_2 >> \Delta f_o$.

For N=6,

$$\text{Pe} \approx \text{Se}^2 \left(\frac{2\pi}{f_s}\right)^6 \frac{1}{7}\left(2BW_2^7 + 42BW_2^5\Delta f_o^2\right)$$

where $42BW_2^5\Delta f_o^2$ is the excessive noise. By neglecting the high order power terms of Δf_o, a general form of Pe for any N is given by

$$\text{Pe(N)} \approx \text{Se}^2 \left(\frac{2\pi}{f_s}\right)^N \frac{1}{N+1}\left[2(BW_2)^{N+1} + N(N+1)BW_2^{N-1}\Delta f_o^2\right] \qquad \textbf{(5.23)}$$

for $BW_2 >> \Delta f_o$. Otherwise, equation (5.22) should be used.

Substitute $Se^2 = \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}$ where Δ is the difference btween two adjacent quantization levels [39] and BW_2=BW/2 into (5.23),

$$\text{Pe(N)} \approx \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\left(\frac{2\pi}{f_s}\right)^N \frac{1}{N+1}\left[2\left(\frac{BW}{2}\right)^{N+1} + N(N+1)\left(\frac{BW}{2}\right)^{N-1}\Delta f_o^2\right] \qquad \textbf{(5.24)}$$

Assume the input signal is a sinusoidal wave, its maximum peak value without clipping is $2^M(\Delta/2)$, where M is the number of bits for the quantizer. For this maximum magnitude, the signal power Ps [39] is

$$\text{Ps} = \left(\frac{2^M(\Delta/2)}{\sqrt{2}}\right)^2 = \frac{\Delta^2 2^{2M}}{8} \qquad \textbf{(5.25)}$$

The maximum SNR for an N-th order bandpass $\Sigma\Delta$ modulator when the notch frequency is not at the desired frequency,

$$SNR_{max} = 10\log(\frac{Ps}{Pe})$$

$$\approx 10\log \frac{\frac{\Delta^2 2^{2M}}{8}}{(\frac{\Delta^2}{12})\frac{1}{f_s}(\frac{2\pi}{f_s})^N \frac{1}{N+1}[2(\frac{BW}{2})^{N+1} + N(N+1)(\frac{BW}{2})^{N-1}\Delta f_o^{\,2}]}$$

$$\approx 10\log(\frac{3}{2}2^{2M}) - 10\log\{\frac{(2\pi)^N}{f_s^{N+1}}\frac{1}{N+1}[\frac{BW^{N+1}}{2^N} + N(N+1)(\frac{BW}{2})^{N-1}\Delta f_o^{\,2}]\} \quad \textbf{(5.26)}$$

From the above analysis, it can be observed that when $\Delta f_o \neq 0$, the maximum SNR can be degraded significantly, especially for higher order modulator.

5.3 Noise Spectral Density Estimation

There are many different DSP techniques that can be applied to measure n_A and n_B. The first one is based on Discrete Fourier Transform (DFT). The estimated n_A and n_B can be written as

$$n_y = \left|\sum_{n=0}^{N-1} D(n)e^{-j2\pi nK_y/N}\right|^2 \quad \textbf{(5.27)}$$

where $y \in$ [A or B], $K_A = 2\pi\omega_A N/f_s$ and $K_B = 2\pi\omega_B N/f_s$. N is the number of samples of D(n) in the DFT calculation. Based on (5.27), the extra digital hardware required for the proposed technique is illustrated in Figure 5.5. The Q and I signals for ω_A and ω_B can be generated using two digital biquads with infinite Q that oscillate at these frequencies. Nevertheless, the variations on n_A and n_B can be significant even for large N. The simplest solution is to estimate n_A and n_B by averaging a number of results calculated according to (5.27).

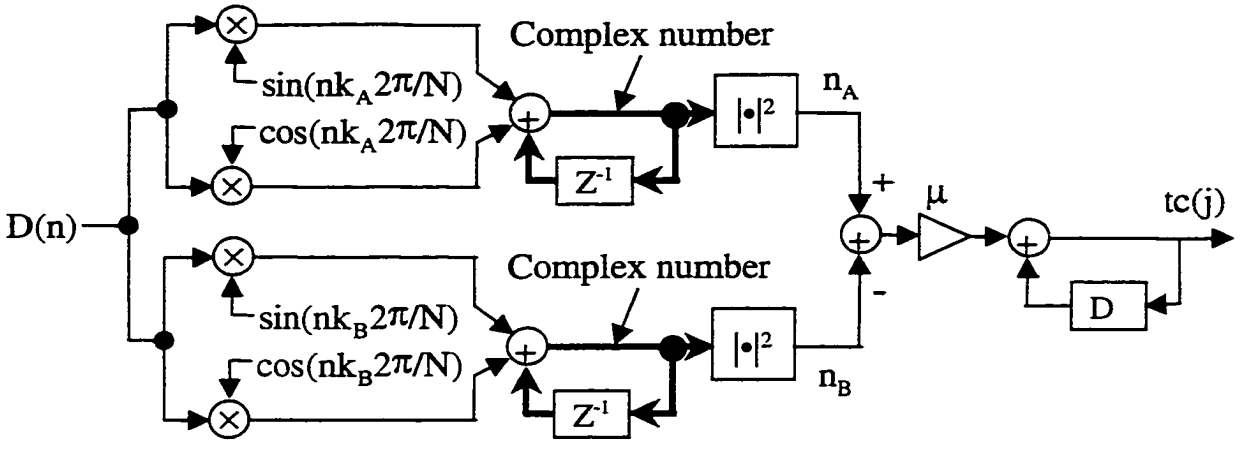


Figure 5.5 Tuning algorithm based on DFT

The second method is to have two high Q digital biquads with center frequencies set at ω_A and ω_B connected to the modulator output and then calculate the filter output powers. This method is illustrated in Figure 5.6. The hardware requirements for both cases are almost compatible.

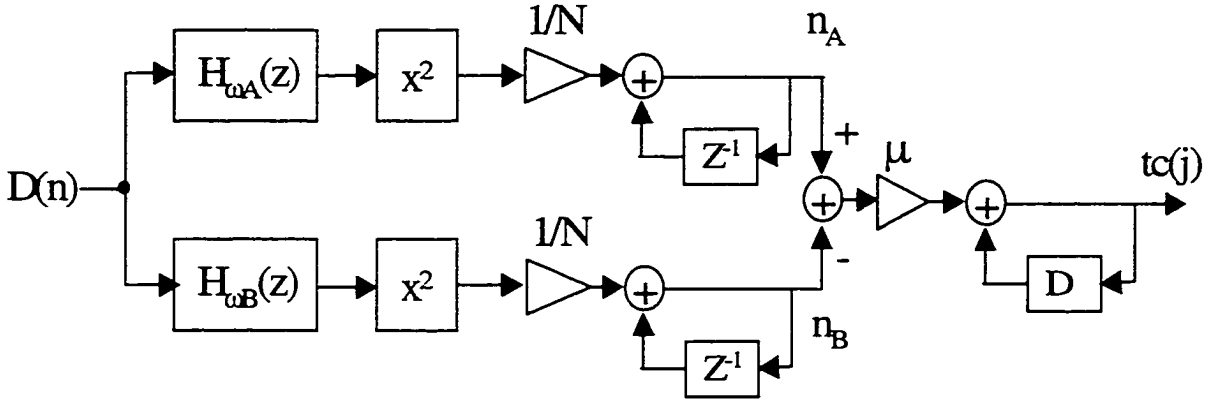


Figure 5.6 Tuning algorithm based on narrow band digital filters

In Figure 5.6, the narrow-band filter was used to extract the noise power. The center frequency of the band pass filter was designed at frequency ω_A and ω_B. A biquad with very good noise and pole sensitivity properties [65] or other narrow-band band pass filter can be applied in this method. Let D(n) be the input digital data for the band pass filter from the sigma-delta modulator and y(n) be its output data. Since the noises at point A and point B have zero mean, the estimated noise power density is given by [66]

$$n_A \propto \frac{1}{N-1}\sum_{n}^{N}(y_A(n))^2 \tag{5.28}$$

$$n_B \propto \frac{1}{N-1}\sum_{n}^{N}(y_B(n))^2 \tag{5.29}$$

where N is the number of bits that are used in the estimation.

5.4 System Parameters Selection

5.4.1 Point A and point B

Since the positions of point A and point B directly determine the magnitude of noise power densities at these two points, they have to be outside BW in order to avoid picking any input signal power in the estimations of n_A and n_B. To achieve high tuning accuracy, a comparatively large frequency difference between ω_A and ω_B should be chosen. Otherwise, two small noise density values must be compared when ω_{oa} is close to ω_o. This will lead to a large comparison error in addition to the estimating errors. However, point A and point B can not be too far way from each other. Otherwise, some other problems will result. First, n_A will almost equal to n_B even if ω_{oa} is not equal to ω_o as shown in Figure 5.7.

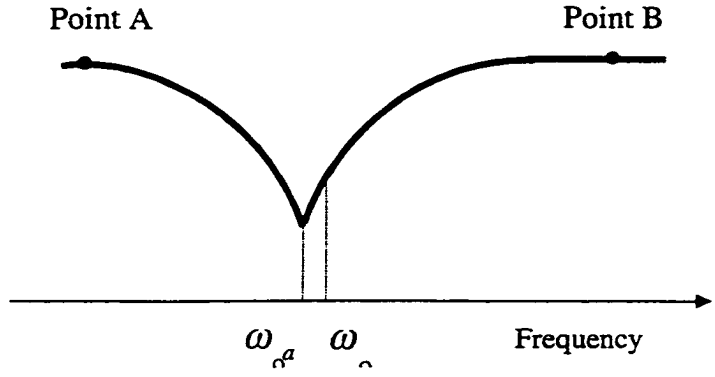


Figure 5.7 $n_A \equiv n_B$ even if $\omega_{oa} \neq \omega_o$

The second problem is that in practice the previous assumption of symmetric about ω_{oa} is not valid due to ω_{oa} too far away from ω_o or due to parasitic poles in the BP filter of the loop.

Another special case for $n_A = n_B$ is that the initial ω_{oa} is too far away from ω_o and point A and B are located in the far end of the same side of the noise transfer function as shown in Figure 5.8. MATLAB simulation results will be presented in section 5.6 to demonstrate these situations.

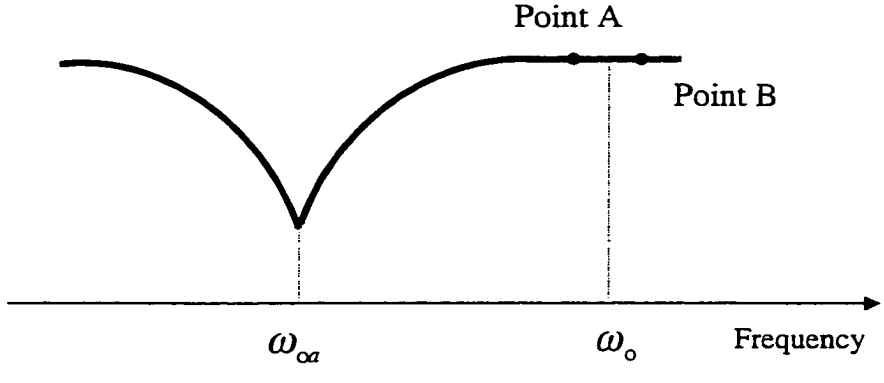


Figure 5.8 Point A and B located in the far end of the same side of the noise transfer function

For the scheme based on digital filter, due to the finite bandwidth of the filter, some noise power from the nearby region will surely be counted into the final estimated result. In addition, the input signal will contribute some energy to the estimated noise power even if it has been attenuated by the narrow-band filters. However, as two symmetrical point are chosen, the input signal have almost equal contributions to the two estimated noise powers and they will cancel with each other.

5.4.2 Coefficient μ

According to equation (5.1), μ is a very important parameter for the proposed technique because it directly decides the feedback amount to the updating circuit. From equation (5.10) and (5.15), it can be observed that μ also affects the system's converging condition, converging speed and tuning accuracy. For fixed Q factor and bandwidth for the two digital bandpass filters, if the value of μ is too small, it will take a long time for the system to settle. If the value of μ is too large, the system will keep running back and forth around the desired center frequency or it will not settle at all. Thus, a proper range for μ must be carefully found out through the analysis presented in section 5.2 and through MATLAB simulation. Some typical MATLAB simulation results for different values of μ will be presented in section 5.6.

5.4.3 Q factor and center frequency gain of the digital filters

For the technique based on narrow band digital filters, the Q factors of the digital filters determine the contribution of nearby noise in the estimation of the noise power densities. Higher Q means less extra noise power and higher tuning accuracy can be achieved. The center frequency gains of the digital filters will scale the estimated noise

power. If it is too small, two small values of n_A and n_B will be compared. A large gain is helpful for tuning accuracy but too large gain will include more extra noise power into the estimation.

5.5 CTBP ΣΔ Modulators with the Proposed Tuning Technique

The entire system including the BP sigma-delta A/D converters and the proposed background digital tuning technique based on DFT is shown in Figure 5.9. Shown in the bottom part of Figure 5.9 is the proposed tuning system.

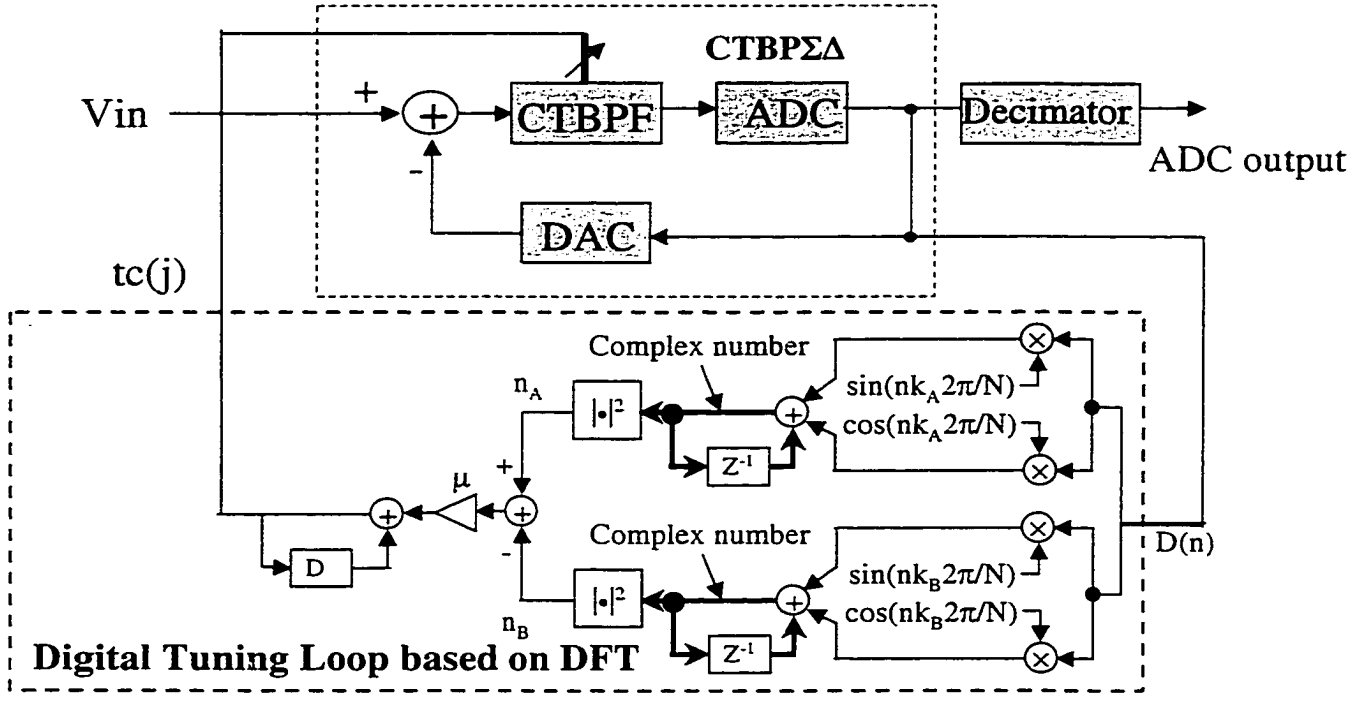


Figure 5.9 Continues-time bandpass sigma-delta ADC system structure with the proposed digital tuning technique based on DFT

The entire system including the BP sigma-delta A/D converters and the proposed background digital tuning technique based on digital filters is shown in Figure 5.10. Shown in the bottom part of Figure 5.10 is the proposed tuning system.

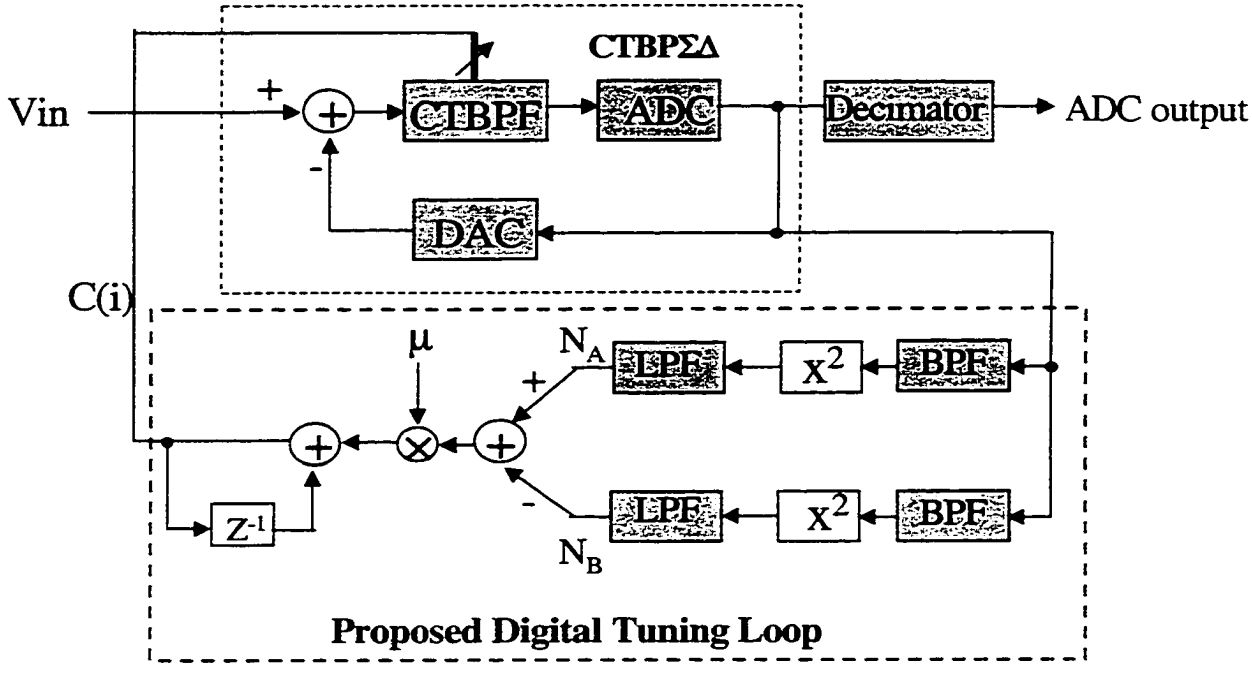


Figure 5.10 Continues-time sigma-delta ADC system structure with the proposed digital tuning technique based on narrow band digital filter

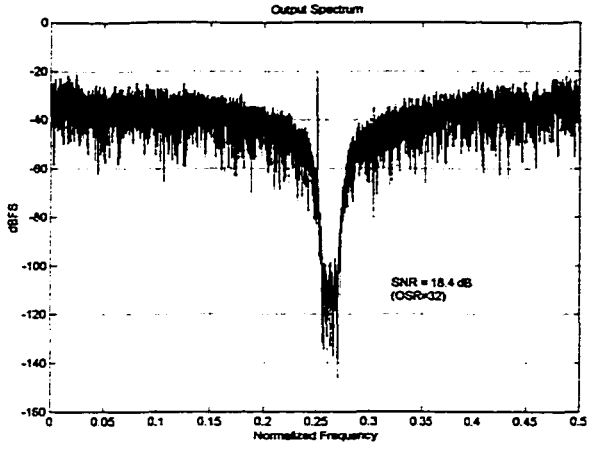
The low pass filter in Figure 5.10 can be an integrator or a low cutoff frequency filter. It can be implemented in many different ways. One simple implementation example was shown in Figure 5.6 where N is a very large value. The larger the value of N, the more accurate the estimation can be made. However, more hardware and computations are needed. The multiplier and the lowpass filter in Figure 5.10 are used to accumulate the squared-sum. Thus, no full FFT calculations are needed in this scheme. This scheme requires less computer resources than that of calculating a full FFT and it is preferred if minimal computational capability is available on-chip.

5.6 MATLAB Simulation Results

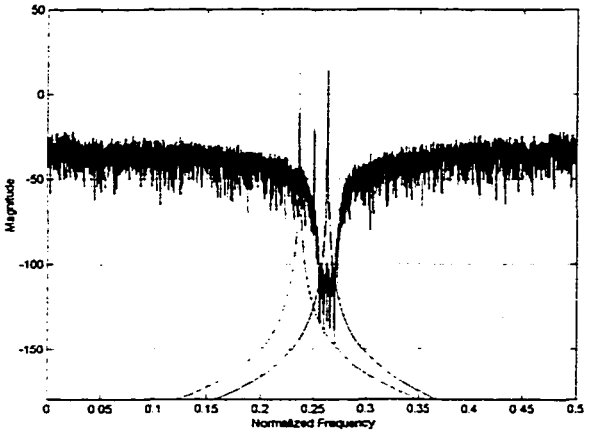
To demonstrate the feasibility of the proposed tuning technique, a series of MATLAB simulations have been done. In order to write a simple code to verify the whole tuning system, an 8^{th} order discrete-time sigma-delta modulator was used in the final MATLAB code, even though this technique is proposed to tune continuous-time bandpass sigma-delta modulator. However, it does demonstrate the proposed tuning method. The normalized center frequency of the discrete time BP filter in the modulator was controlled by a tuning parameter, which is updated using the proposed technique. The updating equations in (5.1) and (5.2) were both employed in the MATLAB code. More details are presented in the appendix.

To understand how the system shown in Figure 5.10 works, it is instructive to know the typical spectrums at various points of the tuning system as shown in Figure 5.11. Figure 5.11 (a) shows an output spectrum in which the notch frequency was shifted to a higher frequency. In Figure 5.11 (b) the transfer functions of the two narrow-band filters were imposed on the shifted output spectrum. Figure 5.11 (c) and (d) show the output spectrums for the left narrow-band digital filter and the right narrow-band digital filter respectively. Figure 5.11 (e) shows the calculated noise power or the two estimated noise power density. The solid line represents the values of n_A while the dotted line represents the values of n_B. In this case, normally n_A is larger than n_B although big value changes exists in n_A. This tells that the notch frequency was shifted to a higher frequency.

(a)



(b)



(c)

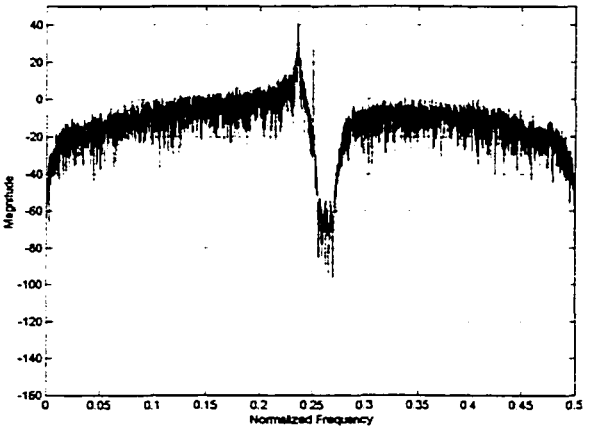
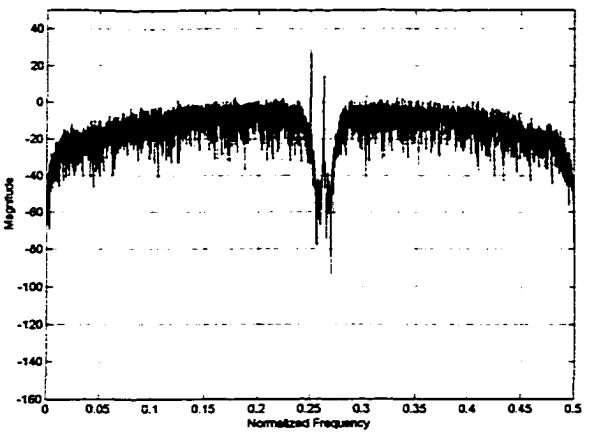


Figure 5.11 Typical spectrum at different points of the tuning system

(d)



(e)

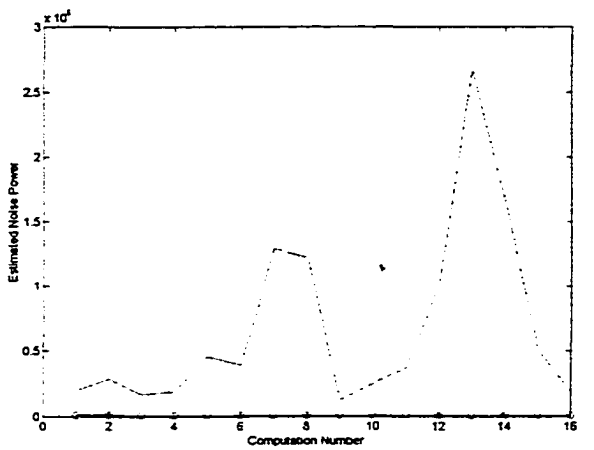


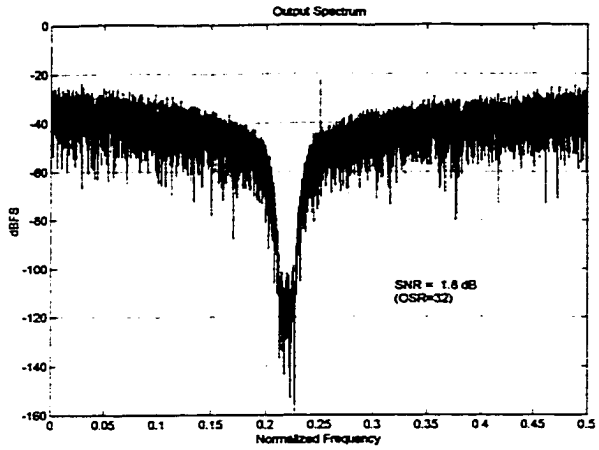
Figure 5.11 (Continued)

5.6.1 Simulation for the simple updating scheme

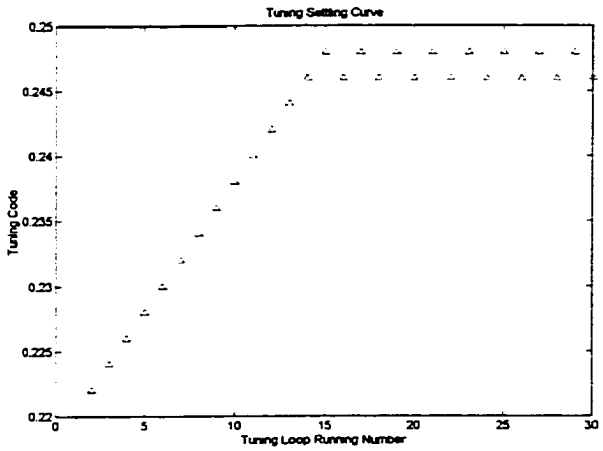
In this section, simulation results with the simple updating scheme that uses equation (5.2) are presented. For all the simulations in this section, μ is equal to 2e-3 and the center frequency difference of the two filters is 1/3. Shown in Figure 5.12 and 5.13 are the tuning processes, in which Q is equal to 100 with the initial notch center frequency shifted to 0.22 and 0.28 respectively. As Q is comparatively low, the system is settled finally but fluctuating between 0.246 and 0.248, and the final SNR is around 42dB. Shown in Figure 5.14 and 5.15 are the tuning processes, in which Q is equal to 200 with the initial notch center frequency shifted to 0.22 and 0.28 respectively. After Q is increased from 100 to 200, the system is settled finally and the center frequency fluctuates between 0.25 and 0.248, and the final SNR is about 63.8dB. Similar simulation results can be achieved when Q is equal to 2000 (corresponding waveforms not shown).

Compared with the complicated updating scheme, the simple updating scheme has a linear convergence process initially and an equal amount of modification is updated to the tuning parameters in every tuning cycle. For the simple updating scheme, careful attention must particularly be paid to the selection of μ in (5.2). With a smaller μ, a long settling time is expected but with a higher accuracy. On the contrary, shorter settling time and larger tuning errors or not settling are expected for large μ. Different from the complicated updating scheme, the parameter being tuned will obviously fluctuate between two values after the system is converged. So, some methods are needed to stop the tuning process after a specified accuracy goal is already achieved or the tuning process is designed to be turned off after some time automatically.

(a)



(b)



(c)

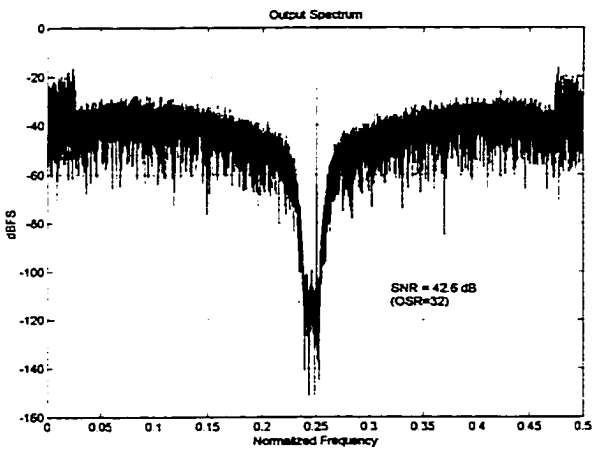
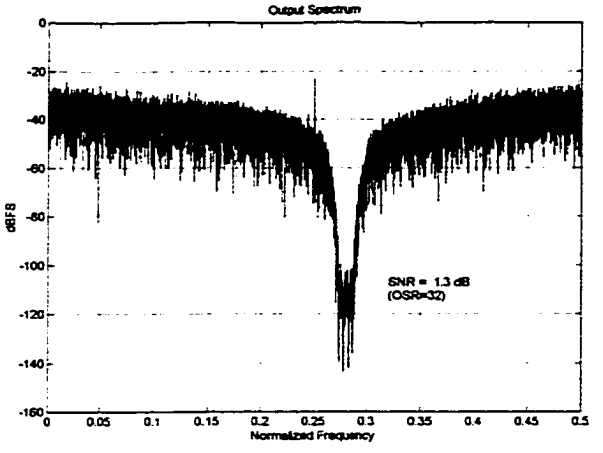
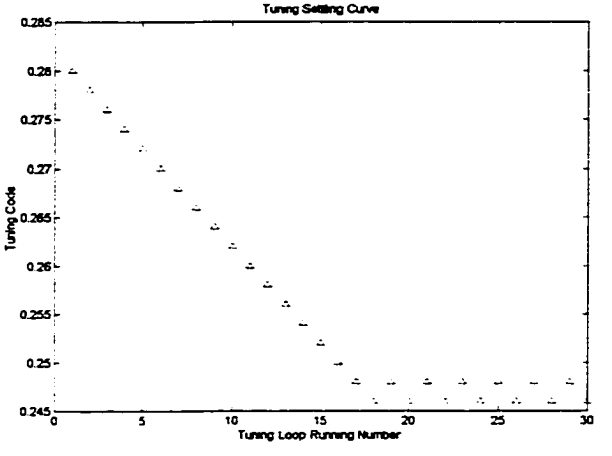


Figure 5.12 Illustration of the tuning technique that is based on the simple updating scheme when the normalized center frequency is initially shifted to 0.22 (with μ=2e-3 and Q=100) (a) initial output spectrum;(b) tuning process; (c) output spectrum after tuning settled.

(a)



(b)



(c)

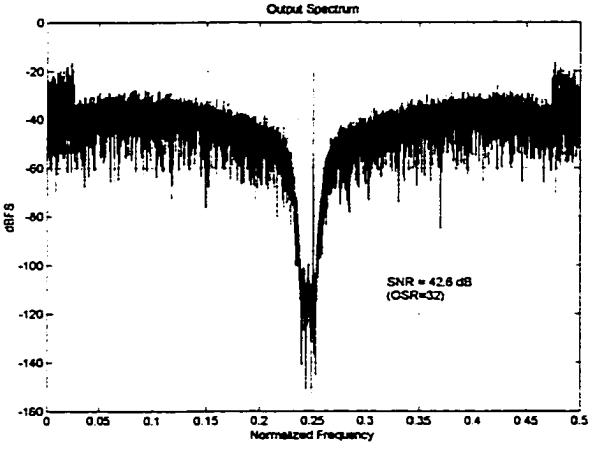
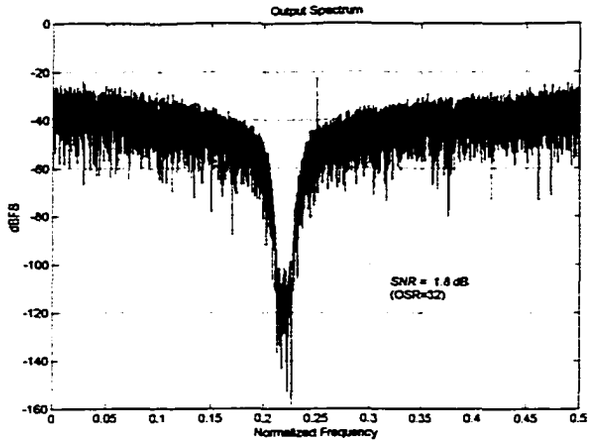
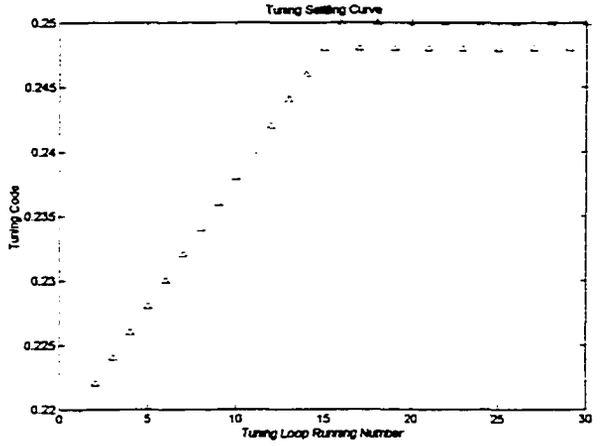


Figure 5.13 Illustration of the tuning technique that is based on the simple updating scheme when the normalized center frequency is initially shifted to 0.28 (with μ=2e-3 and Q=100) (a) initial output spectrum; (b) tuning process; (c) output spectrum after tuning settled.

(a)



(b)



(c)

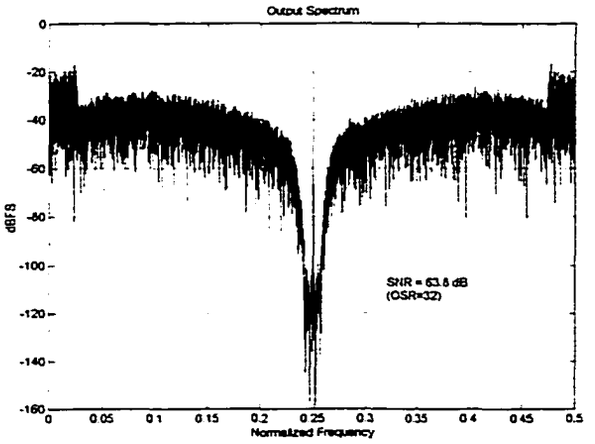
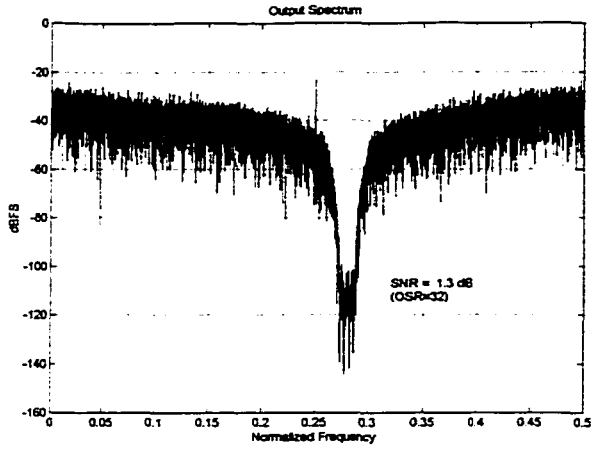
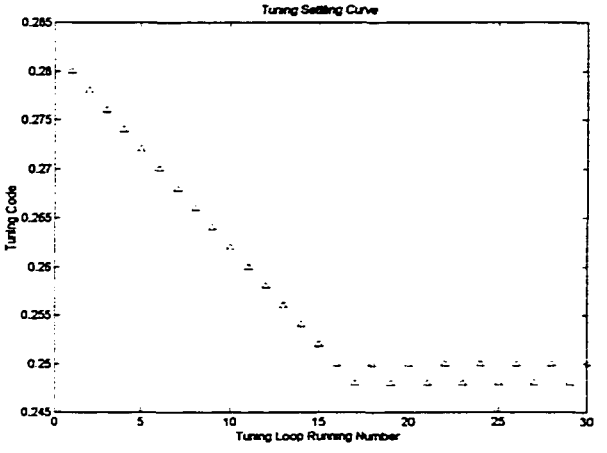


Figure 5.14 Illustration of the tuning technique that is based on the simple updating scheme when the normalized center frequency is initially shifted to 0.22 (with μ=2e-3 and Q=200) (a) initial output spectrum; (b) tuning process; (c) output spectrum after tuning settled.

(a)



(b)



(c)

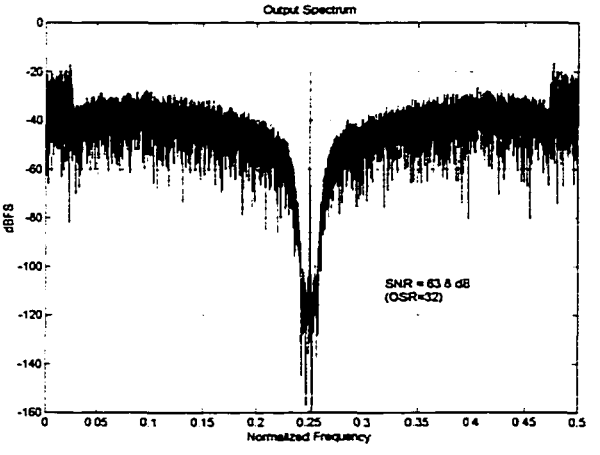


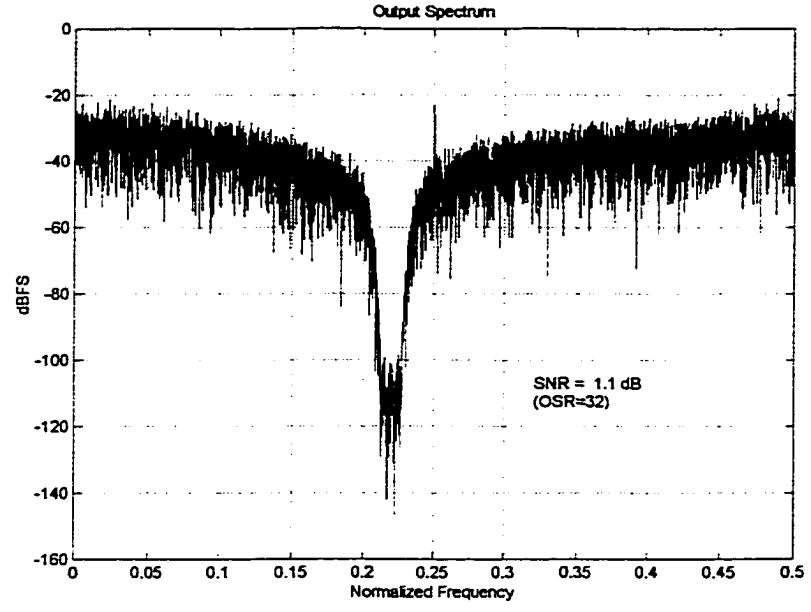
Figure 5.15 Illustration of the tuning technique that is based on the simple updating scheme when the normalized center frequency is initially shifted to 0.28 (with μ=2e-3 and Q=200) (a) initial output spectrum; (b) tuning process; (c) output spectrum after tuning settled.

5.6.2 Simulation for the complex updating scheme

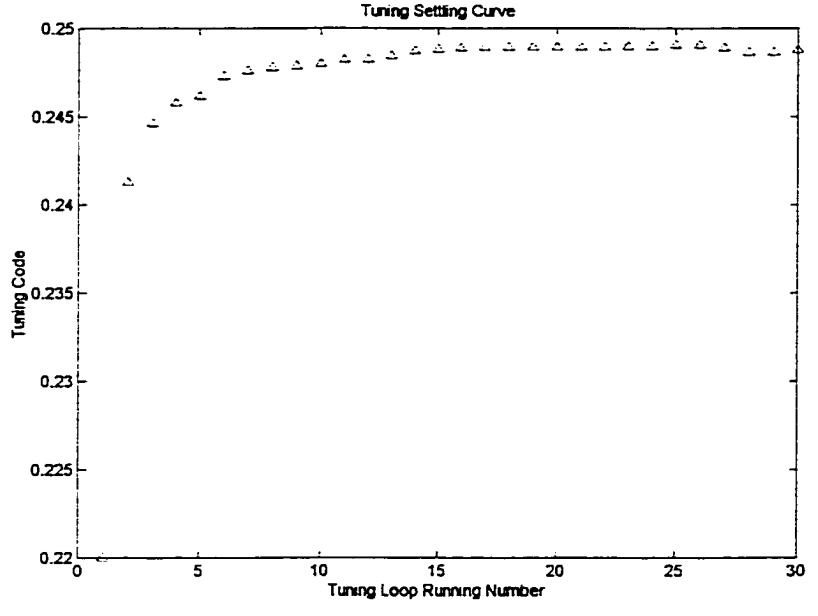
Figure 5.16 demonstrates the tuning process for the complex updating scheme that uses equation (5.1) when the normalized center frequency was initially shifted to 0.22. In this case, the updating coefficient μ was set to 1e-7. Figure 5.16 (a) shows the original output spectrum with SNR = 1.1dB. Figure 5.16 (b) shows the entire converging process after the tuning loop has iterated for 30 times. The normalized center frequency converges to a final value, which is a little bit less than 0.25, after the loop repeated only 15 times. Figure 5.16 (c) shows the output spectrum of the bit stream after the tuning loop has iterated 30 times. The final SNR is 58.7dB.

Figure 5.17 demonstrates the tuning process when the normalized center frequency was initially shifted to 0.28. In this case, the updating coefficient μ was also set to 1e-7. Figure 5.17 (a) shows the original output spectrum with SNR = 0.9dB. Figure 5.17 (b) shows the entire settling process after the tuning loop has iterated for 30 times. Similar to Figure 5.16 (b), the normalized center frequency converges to a final value, which is a little bit less than 0.25, after the loop repeated about 10 times. Figure 5.17 (c) shows the output spectrum of the bit stream after the tuning loop has iterated for 30 times. The final SNR is 60.4dB.

From Figure 5.16 and 5.17, it can be seen large SNR improvements can be achieved in both cases. However, the finally converged normalized notch frequency was not ideally equal to 0.25 in both cases. This is mainly caused by the non-idealities of using the narrow-band filters and the simple noise estimation method. The variance of the tuned center frequency has been given in (5.14). More discussions and MATLAB simulation results will be presented in the following sections.

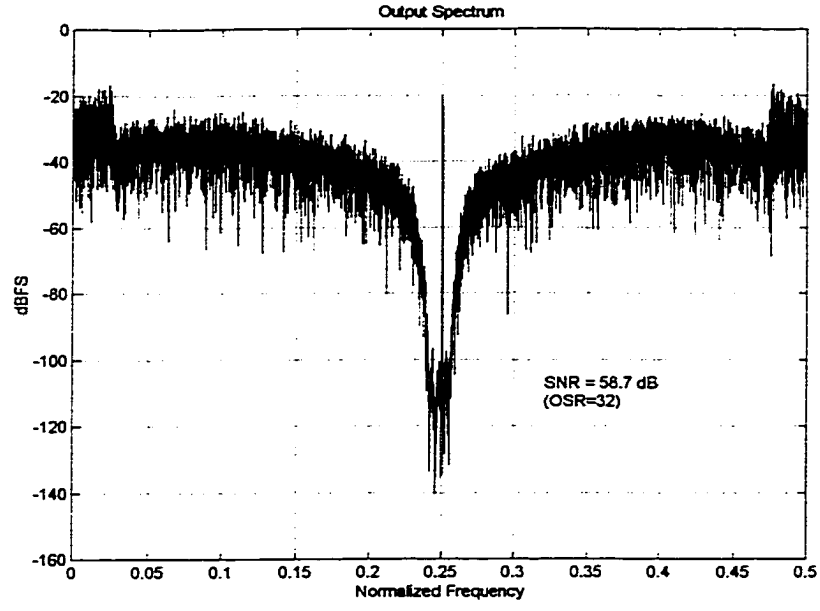


(a) Output spectrum with the normalized notch frequency at 0.22



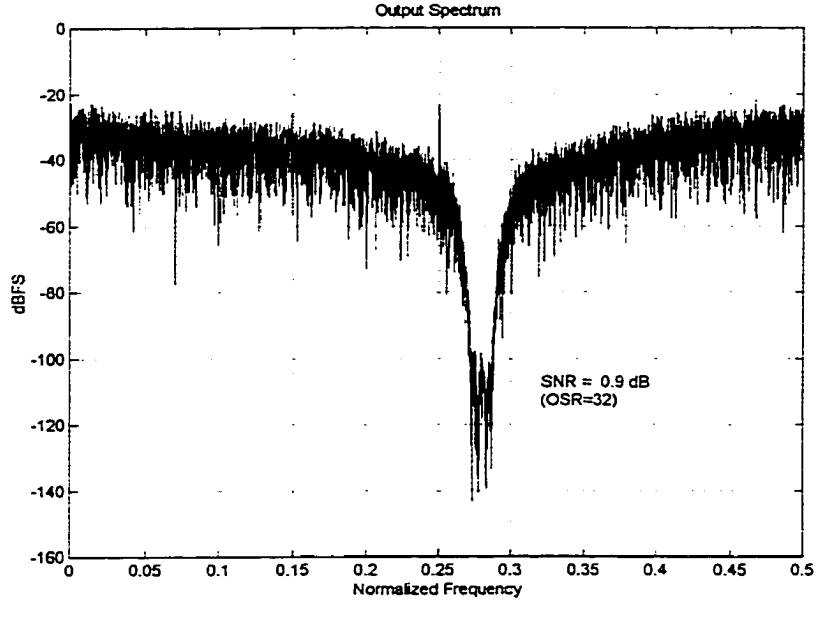
(b) Settling process with the initial normalized notch frequency at 0.22

Figure 5.16 Illustration of the tuning technique that is based on the complex updating scheme when the normalized center frequency is initially shifted to 0.22 (with μ=1e-7 and Q=1000)



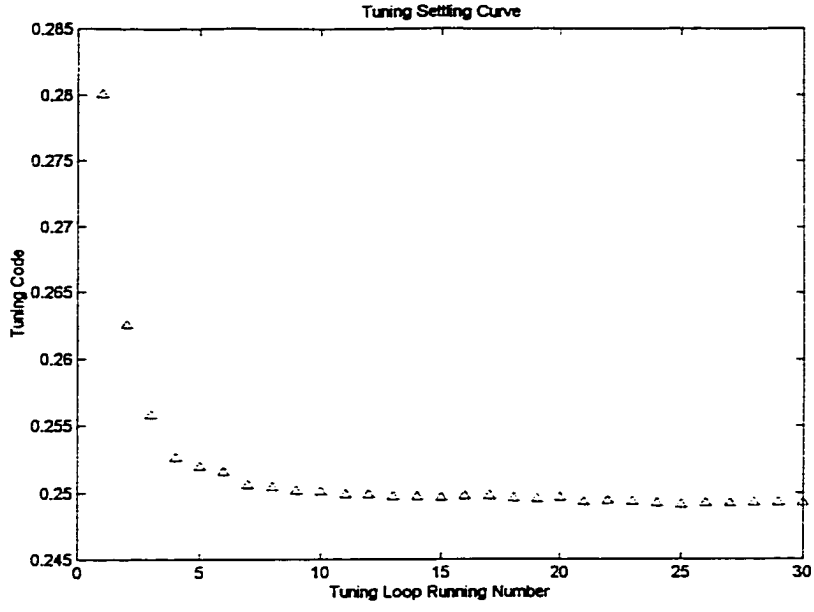
(c) Output spectrum after the tuning loop running 30 times

Figure 5.16 (Continued)

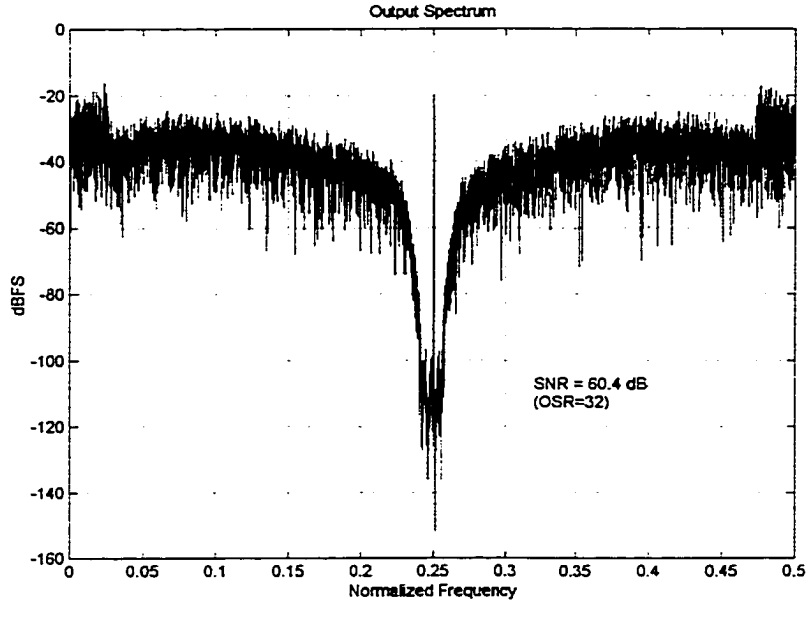


(a) Output spectrum with the normalized notch frequency at 0.28

Figure 5.17 Illustration of the tuning technique that is based on the complex updating scheme when the normalized center frequency is initially shifted to 0.28 (with μ=1e-7 and Q=1000)



(b) Settling process with the initial normalized notch frequency at 0.28



(c) Output spectrum after the tuning loop running 30 times

Figure 5.17 (Continued)

The coefficient μ and the Q factor of the narrow-band filters are the two most important parameters of the proposed tuning method when the noise densities are estimated using narrow-band filters. Also the frequency difference between the desired notch frequency and the deviated notch frequency should not be too large or too small such that this tuning method can be applied. Figure 5.18 illustrates the system settling behavior for different updating coefficients. In these three cases, the system finally converges. It can be observed that the larger the value of μ is, the faster the converging process becomes and the smaller the value of μ is, the slower the converging process results is achieved. Figure 5.19 shows the system settling behavior with very large μ values. If μ is too large, the system will not converge or converge to a wrong value –2.5. The ideal tuning code is 0.25. Figure 5.20 shows the system settling process for different Q values but with the same μ equal to 1e-7. It can be seen that the larger the value of Q is, the faster the converging process becomes and the smaller the value of Q is, the slower of the converging process results. This is easy to understand because the percentage of leaked noise power from outside the band of the narrow-band digital filters is smaller for a larger Q value.

One limitation for the proposed method is that when the initial notch frequency was too far away from the ideal location as shown in Figure 5.8, it could not tell if the modulator is converged to the right point. Thus it is not possible to tune back to the final desired notch frequency if it has converged to a local minimum as shown in Figure 5.19. So this method can only apply when the initial notch frequency is not too far away from the ideal one. Figure 5.21 shows the system settling process for different frequency difference between ω_A and ω_B. When the difference is 1/12 or 1/24, the system converged. When the difference is equal to

1/48, the system converged to a wrong location. This is due to the fact that the noise energies at ω_A and ω_B are too small when compared to the noise outside the band of the narrow-band digital filters. When the difference is equal to 1/6, the system did not converge at all. At this time, point A and point B is beyond the notch region as illustrated in Figure 5.8.

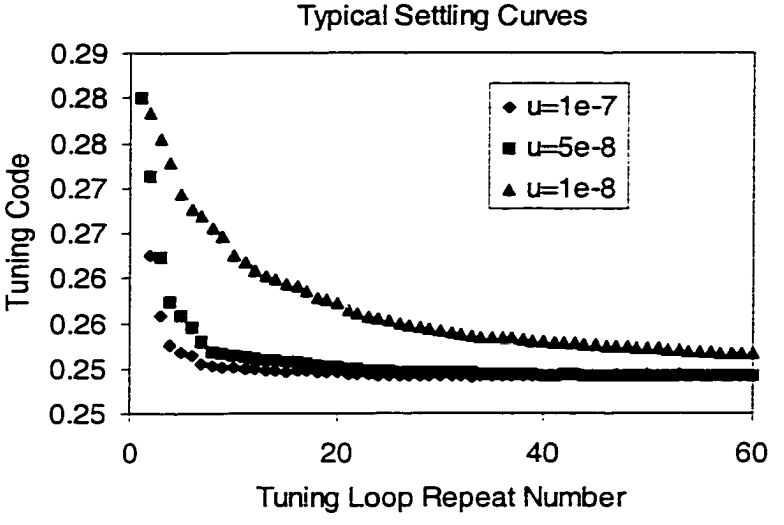


Figure 5.18 Settling curves versa different updating coefficient μ with Q=1000

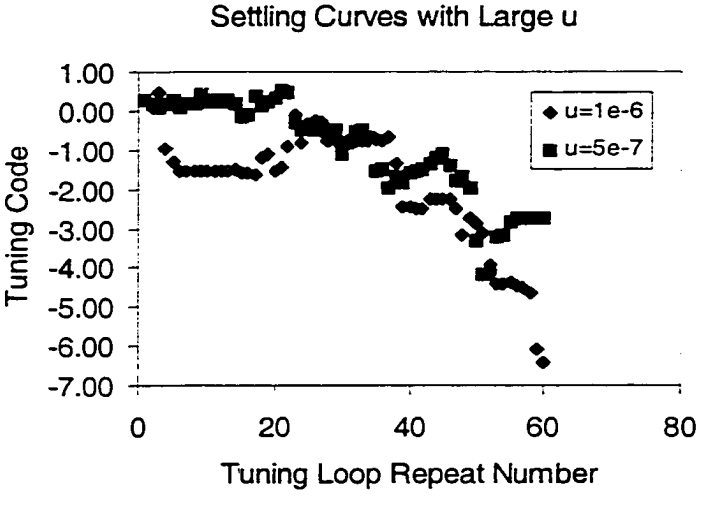


Figure 5.19 Settling curves versa large μ with Q=1000

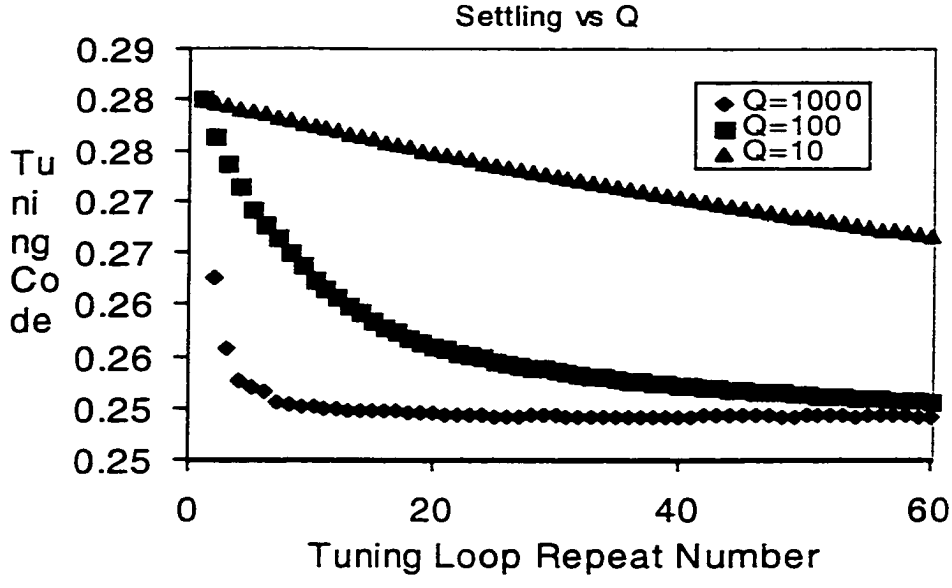


Figure 5.20 Settling curves versa different Q of narrow-band filters with μ=1e-7

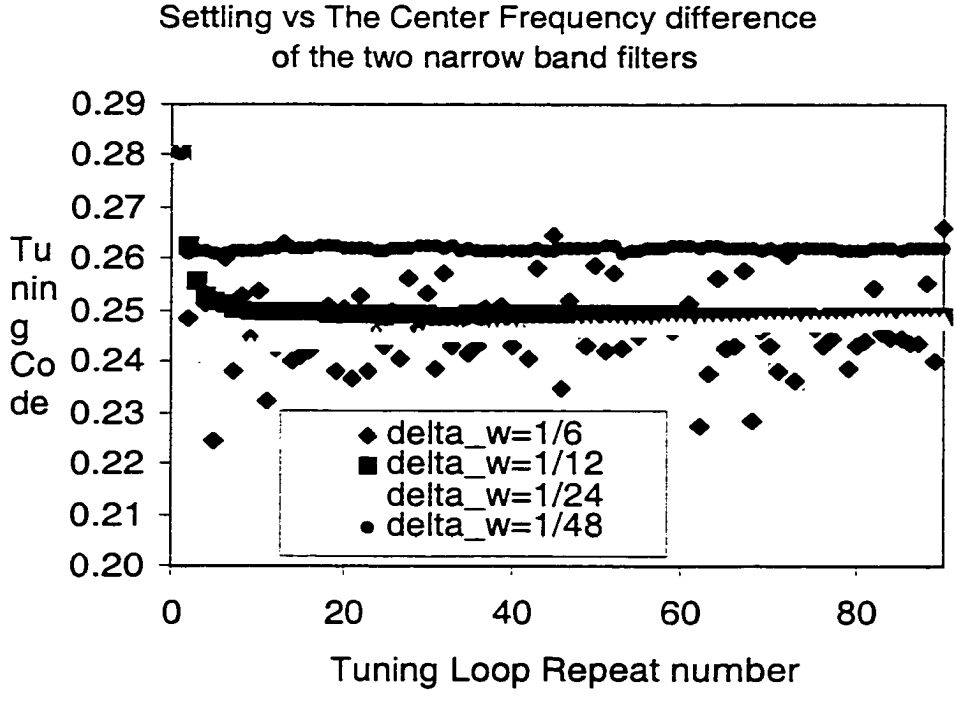


Figure 5.21 Settling curves versa the frequency difference between the shifted center frequency and the desired center frequency with Q=1000 and μ=1e-7

5.7 Summary

In this chapter, a direct background digital tuning technique is presented to tune the center frequency of CT BP ΣΔ modulator. It estimates the noise power densities of two points by doing DFT computations or by using two narrow band BP digital filters. The tuning code of the BP filter in the modulation is updated on the background according to the comparison between the two noise spectral densities at the modulator digital output without interrupting the normal modulator operation. This technique only requires extra DSP hardware and does not need any other extra ADCs or DACs. With slight modification on the updating circuits, this system is applicable to tune GmC, RC or LC type continuous-time sigma-delta modulators and even more, it is applicable to some discrete-time sigma-delta modulators to fine tune the final location of the notch frequency. In principle, the proposed tuning technique can also be applied to BP ΣΔ modulators with mixers in the loop and some bandpass filter system. To use this technique efficiently, proper μ and proper Q values and center frequencies for the two narrow-band BP digital filters must be chosen.

CHAPTER 6 A 1V 1MHZ CONTINUOUS-TIME ACTIVE RC LOW PASS AND BAND PASS FILTER

To demonstrate the proposed filter design in chapter 3 and the filter tuning techniques in chapter 4, a 1 V 1 MHz second-order band pass and low pass filter fabricated in a conventional 1.2 μm CMOS process is presented in this chapter. For a 5 kHz sine wave input signal, the filter achieves a THD of –60.2 dB for a peak-to-peak output voltage of 600 mV. The frequency tuning range is between 585 kHz and 1.325 MHz. The measured power consumption for the filter alone is about 0.52mW and for the entire system consumes about 1.6mW for a supply voltage of ±0.5 V.

6.1 General Design Consideration

The entire filter system shown in Figure 4.2 except the attenuator was implemented in the filter prototype. Simple resistor voltage divider was used as the off-chip attenuator. Due to the limited die area, an 8-bit counter was used as the m-counter. Both the f-counter and the Q-counter were 7-bit. Since the opamp has a unit gain of about 10MHz, the nominal center frequency of the main filter was designed to be at about 1 MHz. The cap array C_A's and C_B's were implemented as double poly capacitors and their values can be expressed as 3 pF + 0.05n pF and 0.1 pF + 0.1n pF, respectively, where n is an integer between 0 and $(2^7 - 1)$. For simplicity, all of the resistors were set to have the same value. The poly resistors must be chosen carefully. If the resistors are too large, they will occupy more area but consume less

power. If the resistors are too small, large biasing currents must be set and this will increase the sizes of the NMOS current sources for biasing the common mode input voltages of the opamps. Simulation results show that the oscillator is prone to stop oscillation when the sizes of the NMOS transistors become too small. Considering the above constraints, all the resistors used in the filter were designed to be about 20 kΩ in this design. To get reasonable output impedance and keep proper sizes for the NMOS current sources, V_x is chosen to be 150mV. Therefore, I_{B1} and I_{B3} are set to 35μ and I_{B2} is set to 17.5μ. The biasing transistors are large enough to have a small minimum saturation voltage. To simplify the entire design, a single off-chip resistor was used to generate the necessary biasing currents for testing.

To avoid the interference of digital circuit noise to the analog circuits, the analog signal path and the digital signal path are completely separated. Good layout matching techniques such as inter-digitized, common-centroid and utilizing unit cell are used to lay out the analog circuits. The main filter is separated from the oscillator by the reference filter.

6.2 Circuit Blocks Implementation

In this section, we describe the transistor level design of the building blocks used in the filter are presented. The filter was implemented in a conventional 1.2um CMOS process.

6.2.1 Low Voltage Opamp Design

One of the most common building blocks in analog circuit design is the opamp. Many analog systems require wide common mode input ranges. To achieve low supply voltages with rail-to-rail signal swings, opamp input stages with rail-to-rail input common-mode ranges have been developed [7] [8] [9] in standard CMOS process with a supply voltage in

the range of 1.2 V to 3 V. Supply voltage can go as low as 1 V if the input differential stage of the opamp is realized using bulk driven MOSFETs [10] or depletion devices available in some specialized BiCMOS process [11].

As the power supply voltage is reduced to less than 1.5V, the number of MOS transistors that can stack is reduced and the gate to source overdriven voltage must be minimized by increasing device sizes. If high gain or high output impedance (e.g., current sources and gain stages) is designed for low supply voltage, very large devices are often employed due to the long channel length and relatively small V_{DSsat}. This would degrade the frequency response. Since it is impossible to achieve high voltage gain with cascode structures for low supply voltage, cascading simple stages is the only way to obtain a gain comparable to a conventional cascode stage. However, these multiple stage designs often present some stability problems when used in a close loop system. Several judicious frequency compensation techniques have been developed to solve this problem [67] [68]. Replica amplifier concept [69] is another way that can be used to realize high gain amplifiers.

The opamp in this design was designed based on a simple two-stage architecture [44] as shown in Figure 6.1. A two-transistor output stage can get maximal output swing even at low supply voltage. Since the input and output quiescent voltages are set to different voltages, it is easy to optimize the input and output stages. The minimum supply voltage required for proper operation of the opamp is

$$Vmin = \mathbf{max}\ \{3V_{OV},\ V_T + 2V_{Dssat}\} \qquad (6.1)$$

The maximum input common-mode range is limited to $V_{DD} - 2V_{SDsat} - |V_{Tp}|$. The biasing current at the output stage was designed to be capable of driving the required resistive load with an output swing close to rail-to-rail (from V_{DSsat} to $V_{DD}-V_{SDsat}$).

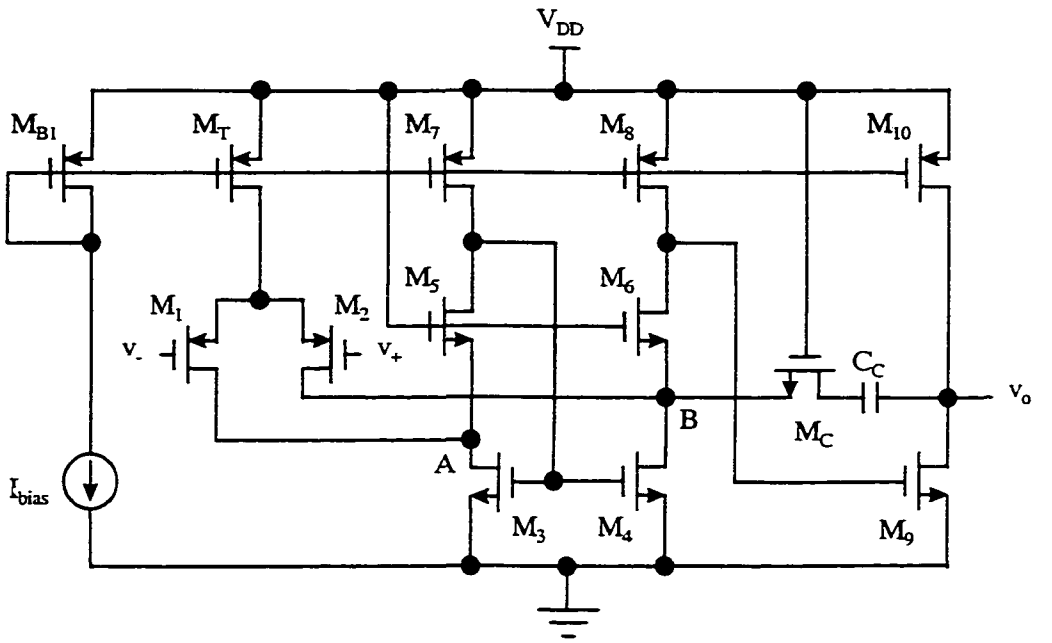


Figure 6.1 1V opamp design

Large transistors were used in the differential input stage such that a maximum input common-mode voltage of about 150 mV could be achieved for a single 1 V supply and a low input-referred noise can be obtained. Simple lead compensation is employed in this opamp. Increasing the size of transistor M9 can move the second pole further away from the unit gain opamp frequency and hence, increasing the phase margin. When designing the opamp layout, the smaller source/drain areas of M1/M2 and M5/M6 are connected to nodes A and B. By using the 1.2um AMI CMOS process model parameters, the simulated opamp performances are summarized in Table 6.1. A higher DC gain and higher unit-gain bandwidth can be achieved when a more advanced process technology is used. A self-cascode structure [26] can further increase the opamp DC gain to about 70-80dB.

Table 6.1 Opamp Simulated Performances

Technology	1.2μ CMOS
Power Supply	1 V
DC gain	> 60dB
Phase margin	> 58°
Unit gain bandwidth (20pF and 10kΩ)	> 9MHz
THD (Unit gain configuration, Vpp=200mV)	< 0.1%
PSRR (10Hz-100kHz)	> 50dB

6.2.2 Low Voltage Latched Comparator

A differential pair is often used as the input stage for a conventional comparator. However, it will have a limited input common-mode range for low supply voltage. To design the latched comparator used in the Q tuning loop, a current-mode comparator was designed as shown in Figure 6.2. It consists of an input folding mirror structure which is similar to the design described in [20] [70]. The input mirror structure is then followed by a latch stage. The minimum supply voltage required for proper operation of the folding mirror structure is $|V_{Tp}| + 2V_{Dssat}$. Wide input signal swing is achieved by connecting the comparator inputs (V_I and $-V_{bp}$) to two resistors, which convert the difference in voltages into current as i_1 that flows to the low impedance node A. The current i_2 is used as a reference for comparing with i_1. V_I and V_{bp} correspond to the in-phase output of the oscillator and the bandpass output of the reference filter shown in Figure 4.2. Since v_I and v_{bp} are actually 180° out of phase at ω_o and have the same quiescent voltage, i_1 and i_2 will be equal if v_I and v_{bp} have the same amplitude. Otherwise, i_1 and i_2 will be different and a logic signal is produced at the output after the signal, *latch*, (generated from v_Q) turns high.

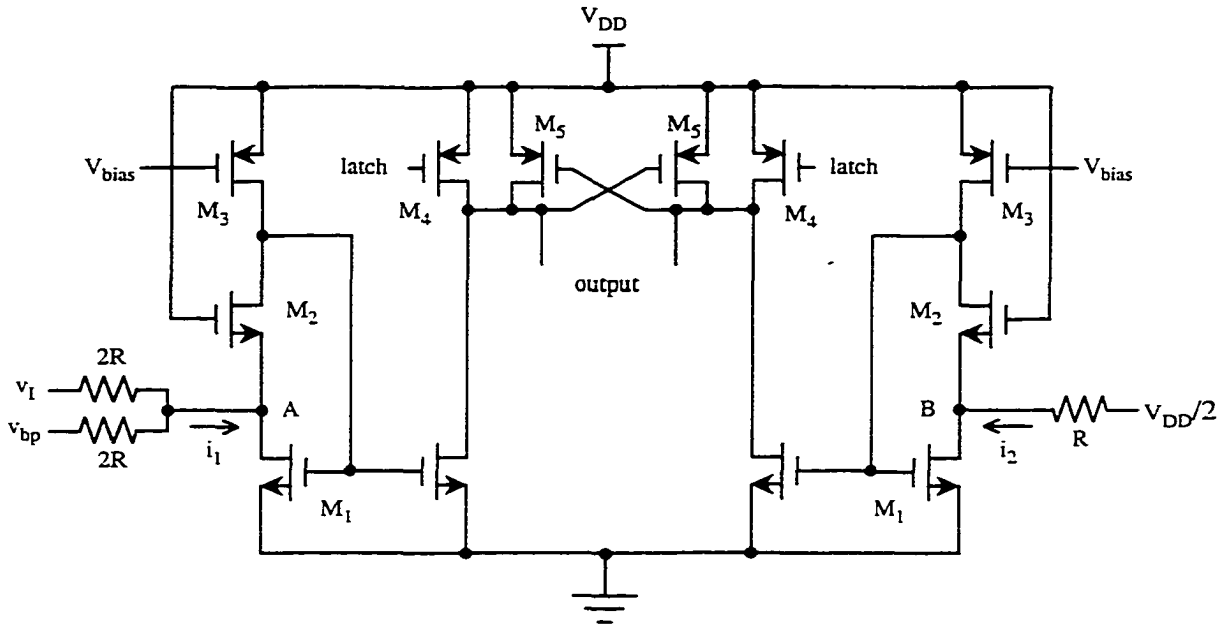


Figure 6.2 Proposed 1V current-mode comparator design

Simulation shows that the minimum difference in input voltage to produce a valid logic output is 0.15mV. It can operate up to a clock frequency of 2.5MHz. The minimum supply voltage is approximately given by

$$\text{Vmin} = \max\{V_T + 2V_{DSsat}, 3V_{SDsat}\} \qquad \textbf{(6.2)}$$

Although the offset of the comparator will result in errors in the Q factor, this error is usually less than the errors discussed in chapter 4 and is minimized by careful layout.

6.2.3 Low Voltage Process Tracked Biasing Circuit

Since the values of the resistors may change due to process variations or temperature change, the biasing current source I_1 in a BIOS is required to track with the changes in resistance. This can be achieved using the circuit shown in Figure 6.3[51].

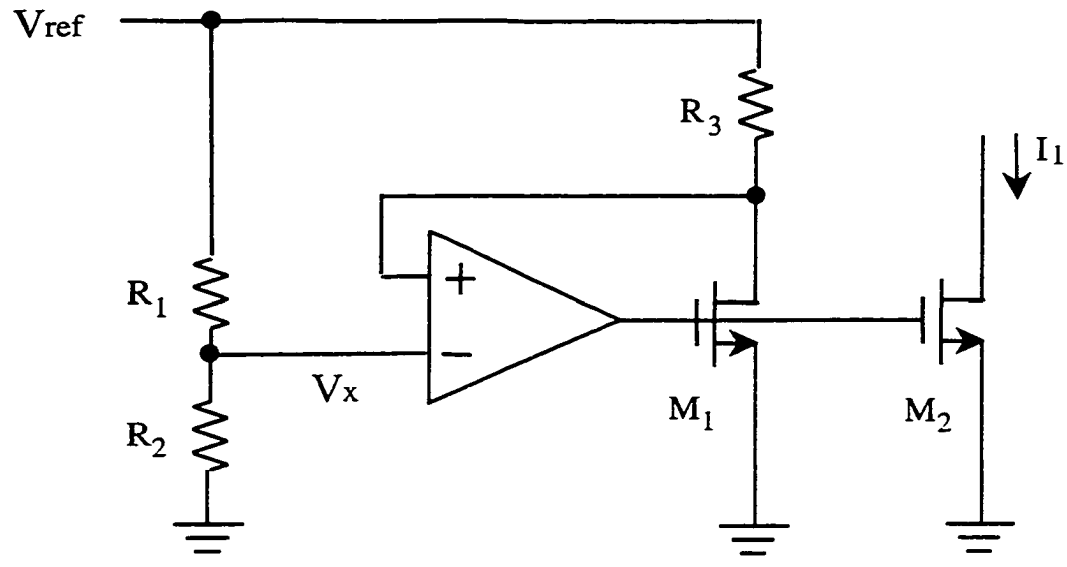


Figure 6.3 Biasing circuit for generating I_1

Assume that a reference voltage V_{ref} is available. Then a suitable v_x can be generated using a voltage divider. Due to the feedback loop that consists of the amplifier A and M_1, the drain current of M_1 as well as I_1 can be written as

$$I_1 = \frac{V_{ref} - V_x}{R_3} = \frac{V_{ref}\left(\frac{R_1}{R_1 + R_2}\right)}{R_3} \qquad \textbf{(6.3)}$$

and hence, I_1 will track with changes in resistance. The amplifier A can be realized using a simple differential stage similar to the first stage of the opamp shown in Figure 6.1. Furthermore, the drain voltages of M_1 and M_2 will be the same and equal to v_x even if they are in triode region. Therefore, the value of I_1 can be set robustly to the desired value and the minimum required supply voltage can be reduced to about $V_T + 3V_{DSsat}$.

6.3 Simulation Results

Some important simulation results about the BIOS structure, the oscillator and the filter are presented in this section.

6.3.1 BIOS structure

With $R_1=R_f=20k\Omega$, $W_1/L_1=218.4u/1.8u$ and C=10pF, the simulated performances for the BIOS circuit shown in Figure 3.1(d) are shown in Table 6.2.

Table 6.2 BIOS simulated Performance

Technology	1.2μ CMOS
Power Supply	1 V
-3dB frequency	700kHz
Input swing	800mV
Output swing	>800mV
THD (100kHz, Vpp=800mV)	< 0.14%

The simulated total power dissipation for the main filter is approximately equal to 850 μW. With ideal current sources, the simulated THD for 1-kHz sinusoid input was found to be less than –90 dB for a peak-to-peak output swing of 700 mV. The THDs at 100 kHz and 1 MHz were found to be about -81 dB and -50 dB, respectively, for a peak-to-peak output swing of 375 mV.

6.3.2 The matching between f_{osc} and ω_o

Similar to the conventional frequency-tuning scheme that uses a PLL, the proposed digital frequency-tuning accuracy is strongly dependent on a good match between the oscillating frequency f_{osc} and the center frequency of the filter ω_o. Figure 6.4 shows the Spice simulation results of f_{osc} and f_o ($\omega_o = 2\pi f_o$) for different control codes for PCA C_A.

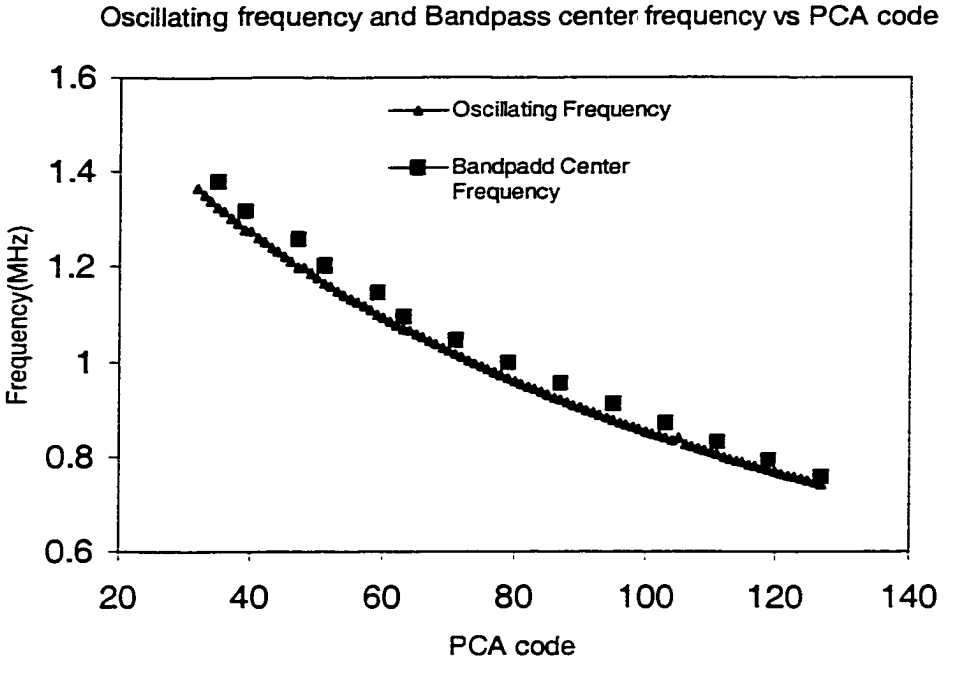


Figure 6.4 Simulation results of oscillating frequency and bandpass center frequency vs PCA code

It can be seen that f_{osc} is always smaller than f_o by an error of 2% to 5% due to different loading effects for the opamps in the oscillator and the filter. This will produce an error to the filter center frequency after tuning. To reduce this error, an offset can be added to the final tuning code. However, this offset must be properly chosen after considering different process variations.

6.3.3 Oscillating magnitude of the oscillator

To have a good matching between f_{osc} and f_o, the oscillating voltage range must be within the opamp output range. In the prototype filter design, a diode-connected transistor connected between the bandpass out and the positive input of opamp A is used to limit the oscillating amplitude. Figure 6.5 shows the simulated oscillating magnitude vs. different

oscillating frequencies. For the whole tuning range, the peak-to-peak oscillating magnitude falls in the range between 340mV and 700mV, which is well within the opamp's output voltage range. The oscillating magnitude is about 500mV at around 1MHz and this matches well with the measurement result as shown later in Figure 6.7.

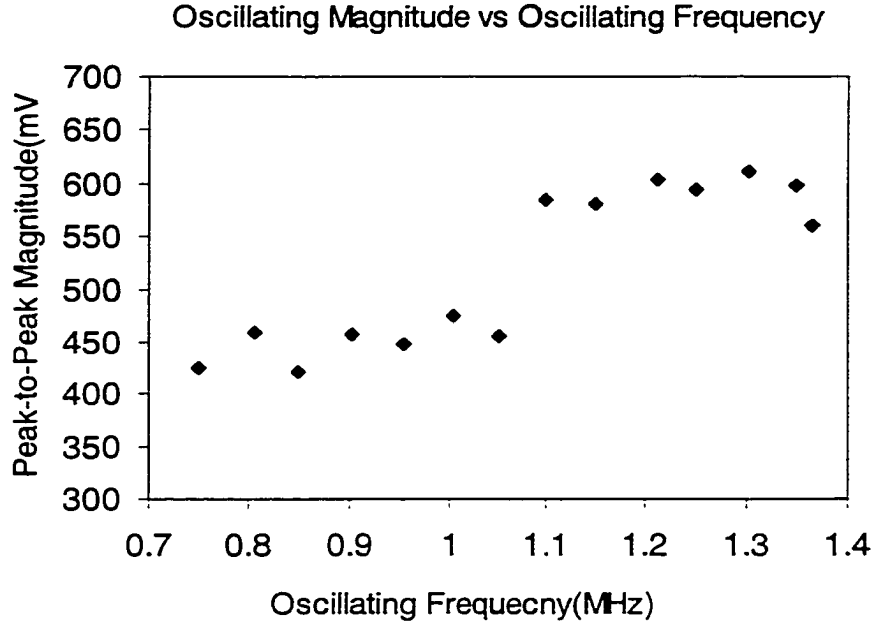


Figure 6.5 Simulation results of oscillating magnitude change with oscillating frequency

6.4 Measurement Results

The die photo of the entire filter system is shown in Figure 6.6. The entire filter system was tested with a ±0.5 V supplies. The filter alone consumed less than 0.52 mW and the entire system including all the biasing current, digital circuits and I/O pads dissipated less than 1.6mW (without counting the atteuator).

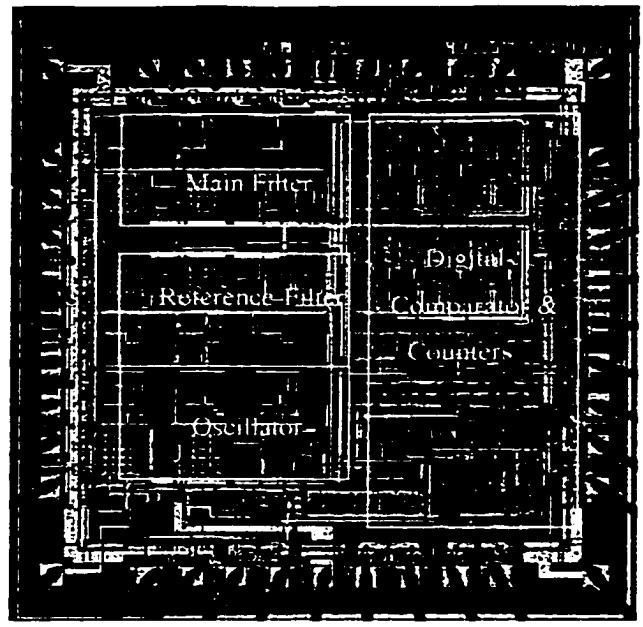


Figure 6.6 Filter Die photo

The opamp had an output swing between –0.4 V and +0.4 V for a supply voltage of ±0.5 V. The center frequency of the bandpass output can be tuned from 585 kHz to 1.325 MHz by setting B_f, which determines the oscillator's oscillating frequency f_{osc}. Figure 6.7 shows the two outputs of the oscillator at 1 MHz.

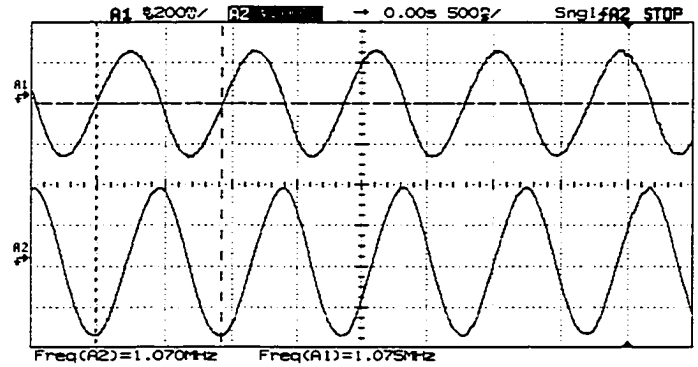


Figure 6.7 Measured oscillator outputs at f_{osc} = 1 MHz

Figure 6.8 shows the lowpass output responses with different ω_o's and Q factors. In this series of test, CQ is kept constant. Thus, smaller Q factors are achieved for lower center frequency. Figure 6.9 shows the measured and simulated bandpass output response with different Q factors. The dashed lines in Figure 6.9 are simulated ideal filter results. The desired center frequency was set at 1 MHz. The accuracy of the center frequencies after tuning was found to be within ± 2 % of the desired values for 5 dies. The testing results also show that larger errors will appear for other lower and higher center frequencies. The errors in center frequencies were mainly due to different off-chip loading on the oscillator and the filters as discussed in chapter 4 and section 6.2.2 and 6.2.3. The tuned Q factor was found to be always higher than the desired values by a factor of about 10 % to 15 %. This was mainly due to the undesired phase shift ($\approx 10^{\circ} - 20^{\circ}$) of the off-chip resistor attenuator. If the resistor attenuator was realized on-chip, it is expected the Q factor can be tuned to within 2 % accuracy as suggested from the HSPICE simulation results.

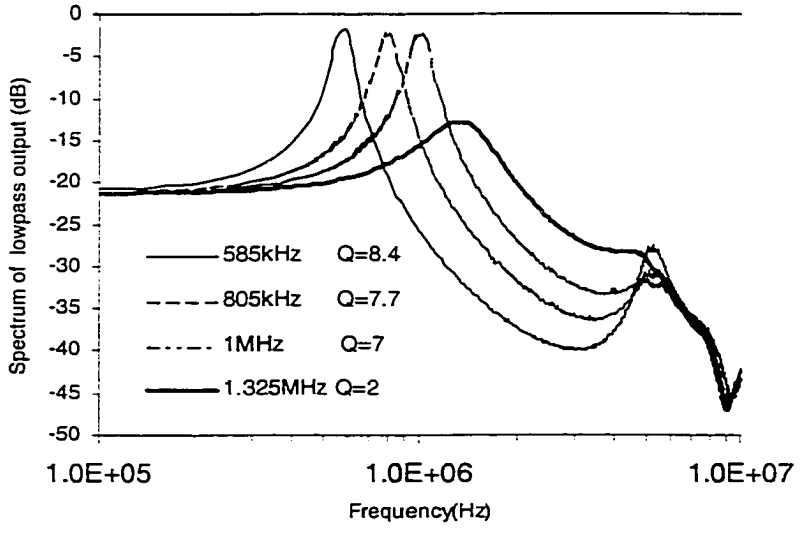


Figure 6.8 Measured lowpass output responses

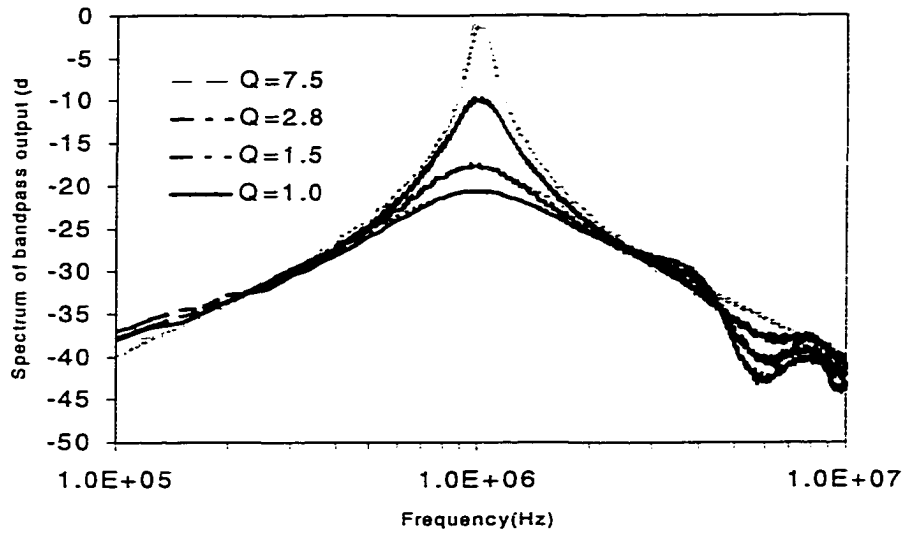


Figure 6.9 Ideal and measured bandpass output response

Figure 6.10 shows the measured THD performance for different peak-to-peak magnitudes at the low-pass output of the main filter for two different input frequencies (5 kHz and 100 kHz). Less than –56 dB of THD can be achieved for a peak-to-peak output voltage up to 635 mV.

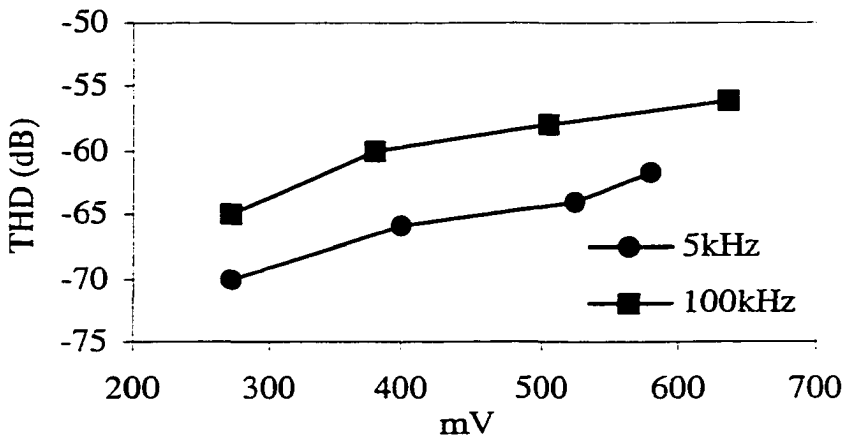


Figure 6.10 Measured THD vs. peak-to-peak output voltage

Figure 6.11 shows the magnitudes of the inter-modulation products. In this measurement, the center frequency of the filter was set to 1 MHz with a Q factor of 2. Two input signals at 990 kHz and 1010 kHz with equal peak-to-peak value of 160 mV were fed to the filter input. The intermoduation products were found to be about 48 dB lower than the two input signals. The linearity of the filter at high frequency is mainly limited by the slew rate limit and the finite gain bandwidth product of the low voltage opamps. Figure 6.12 shows the extrapolated third order intercept point. The input intercept point (IIP3) was found to be 13.5 dBm. The signal-to-noise ratio measured at the lowpass output was found to be 66.7 dB. A summary of the experimental results is given in Table 6.3.

Table 6.3 Summary of experimental results

Parameters	Measured Results
Technology	1.2 μm CMOS ($V_{tn} \approx 0.6$ V, $V_{tp} \approx -0.8$ V)
THD (f_{in} = 5kHz)	-60.2 dB @ V_{P-P} = 600 mV
IM3 @ Vin1 = Vin2 = 0.16 Vp-p	< -48 dB
IIP3	13.5 dBm
Frequency tuning range	0.585 MHz – 1.325 MH
Q tuning range	1 – 7.5 @ ω_o = 1 MHz
Output noise @ 1 kHz	120 nV/$\sqrt{Hz}$
SNR for a 1 MHz bandwidth	66.7 dB
PSRR (V_{DD})	31 dB @ 5 kHz 29 dB @ 100 kHz
PSRR (V_{SS})	38 dB @ 5 kHz 35 dB @ 100 kHz
Filter power dissipation	0.52 mW
Total power dissipation	1.6 mW
Supply voltage	±0.5 V
Active area	1.9×1.9 mm^2

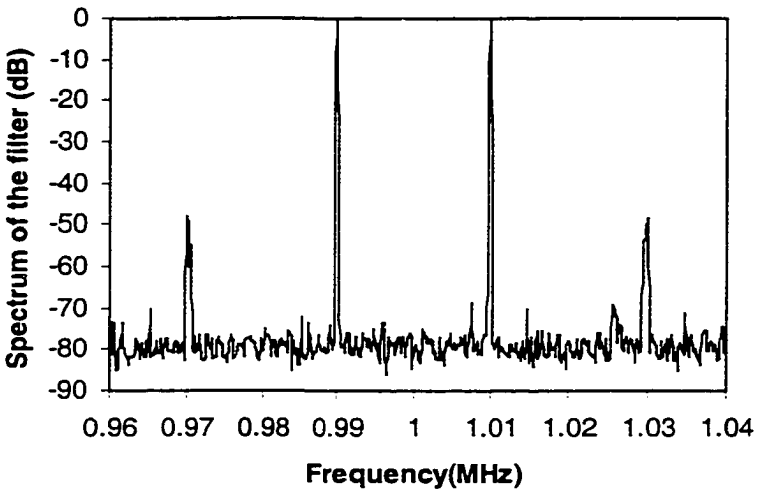


Figure 6.11 Measured two-tone intermodulation distortion for the filter

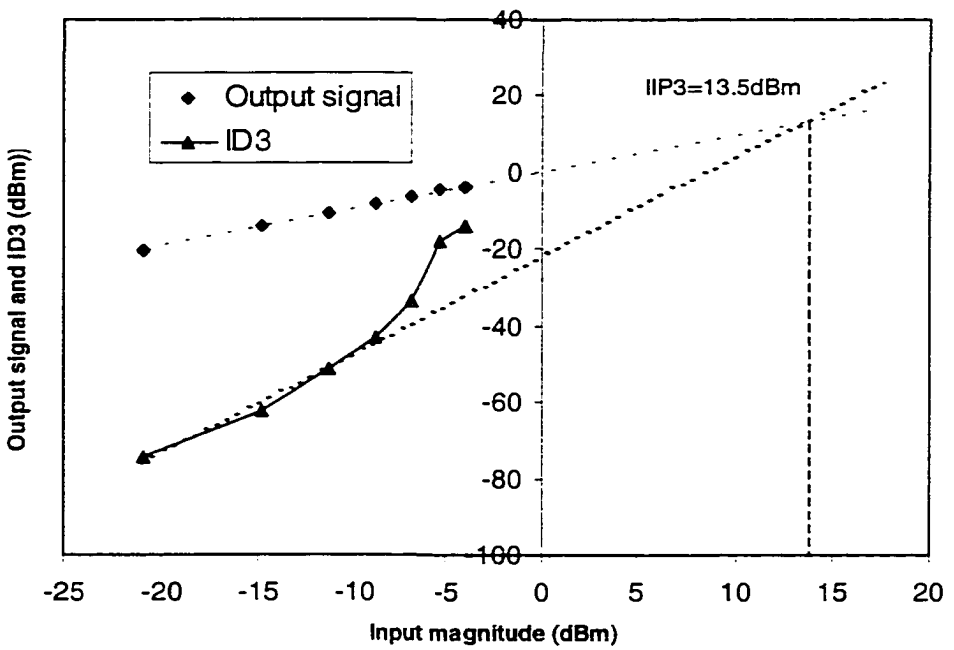


Figure 6.12 Extrapolated third-order intercept point

6.5 Summary

An integrated 1V 1MHz second-order filter with on-chip digital tuning has been implemented with the proposed low voltage design techniques. The center frequency of the proposed filter can be tuned from 585KHz to 1.325MHz and the Q factor is tunable between 1 and 6 at ω_o = 1.25MHz. The center frequency of the second order bandpass filter can be tuned within ±3%. The accuracy of tuned Q is in the range of 15%. The filter achieves THD ≤ -56dB with an output swing of 650mVpp. The third order inter-modulation distortion is lower than –40dB for a two tone signal with a peak-to-peak value of 300mV. The filter alone dissipates 0.52 mW, and the entire system including tuning circuits consumes 1.6 mW. This design demonstrate that low voltage low power continuous-time filter can be implemented in low cost standard CMOS process without using specialized process or on-chip voltage multiplier.

CHAPTER 7 A 1.2V FULLY DIFFERENTIAL SECOND-ORDER CONTINUOUS-TIME BAND PASS SIGMA-DELTA MODULATOR

A 1.2 V continuous-time bandpass sigma-delta modulator implemented in a conventional 1.5 μm CMOS process is presented in this chapter. It consists of a fully differential integrated-RC resonator, a returned-to-zero digital-to-analog pulse shape feedback loop and a one half-delayed-return-to-zero (HRZ) digital-to-analog pulse shape feedback loop. The modulator is tuned using the direct background digital tuning technique presented in chapter 5. For a sampling rate of 4 MHz, the maximum SNDR after tuning was measured to be 44.6 dB and the power dissipation was 2.1mW.

7.1 Introduction

The rapid development of wireless digital radio systems leads to a great effort to design high resolution and high-speed A/D converters. Lowpass and bandpass delta-sigma modulators are the preferred architecture for high-resolution A/D converters. Sigma-delta modulators can be implemented by designing the loop integrator or resonator either in discrete-time domain using switched-capacitor technique or in continuous-time domain using RC, transconductor-C, or LC filter techniques.

Recently, the popularity of continuous-time delta-sigma modulators is increasing due to some important advantages over the well-known discrete-time sigma-delta modulators for either high speed or low power applications. These advantages include higher sampling rate, lower thermal

noise, inherent anti-aliasing filter and reduced input sampling errors. However, there are also some problems associated in the design of continuous-time ΣΔ modulators. The first major problem is the excess loop delay, which is the delay between the sampling clock edge and the DAC output pulse as seen at the feedback point. It is significant because it changes the equivalence between the CT and DT transfer functions of the loop filter H(s) and H(z), respectively. If the excess loop delay is not properly optimized, it will increase in-band white noise, reduce maximum stable input amplitude and degrade DR. The second major problem in the implementation of continuous-time sigma-delta modulators is sensitivity to clock jitters. Timing errors due to clock jitter in the feedback loop increases the noise level in the signal band [59][60][61]. Another problem for some CT ΣΔ modulators is the tradeoff between stability and input dynamic range. Usually, large gain for the first integrator can cause instability problem. The other potential problem comes from the non-ideality and variations of circuit components such as integrators, resistors and capacitors such that the center frequency or the cutoff frequency of the CT filter in the modulator can vary significantly due to temperature and process variations. Therefore, tuning is required.

Generally, there are three kinds of feedback DACs that can be used in the design of CTΣΔ modulators: the non-return-to-zero (NRZ) DAC, the return-to-zero (RZ) DAC and the half-delay return-to-zero (HRZ) DAC. The NRZ DAC is driven directly by the quantizer output and hence, the NRZ DAC output is remained constant during a complete clock period. CTΣΔ modulators with NRZ feedback DAC suffer from harmonic distortion due to the asymmetric waveform of the DAC output signal. CTΣΔ modulators with return-to-zero (RZ) DACs can eliminate the correlation between the input signal and the amount of current feedback. This correlation is the main source of

harmonic distortion in NRZ DACs with asymmetric waveforms. If the DAC output is returned to zero at the beginning or at the end of each cycle, the pulse shape at the DAC output will be less signal dependent and, thus less harmonic distortion. The half delay return-to-zero (HRZ) DAC is similar to the RZ DAC except that the output of the HRZ DAC is delayed by one-half clock cycle. In practice, a multi-feedback scheme is often employed to design continuous time sigma-delta modulators such that the overall transfer function can become equivalent to its discrete time counterpart.

7.2 General Design Consideration

A fully differential second-order CT ΣΔ modulator is chosen to demonstrate the feasibility of the tuning algorithm discussed in chapter 5. The block diagram of the multi-feedback second-order CT ΣΔ [59] with return-to-zero (RZ) DAC and half-delayed-return-to-zero (HRZ) DAC is shown in Figure 7.1.

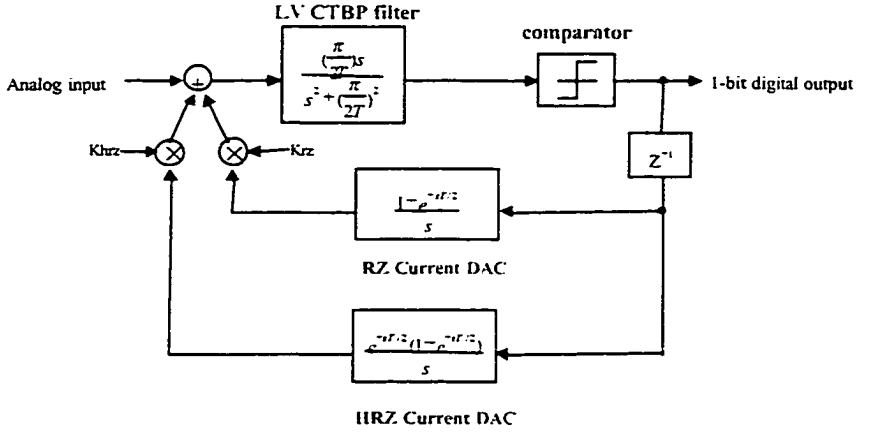


Figure 7.1 Diagram of a second-order multi-feedback (RZ and HRZ) CT ΣΔ modulator

One important type of continuous-time band pass ΣΔM is obtained by performing the substitution of z^{-1} to z^{-2} to the low-pass ΣΔ modulator that has a quantization noise notch right at dc. This produces a bandpass (BP) ΣΔ modulator with a noise notch right at fs/4. This method is adopted in this design.

$$H_{LP}(z)=\frac{z^{-1}}{1-z^{-1}} \longrightarrow H_{BP}(z)=\frac{z^{-2}}{1-z^{-2}} \tag{7.1}$$

Where $H_{LP}(z)$ and $H_{BP}(z)$ are the low pass filter and the bandpass filter inside the ΣΔ modulator, respectively. It is known that equivalence exists between CT ΣΔ modulators and DT ΣΔ modulators when the following condition holds [71].

$$Z^{-1}\{H(z)\} = L^{-1}\{h_{DAC}(s)H(s)\}|_{t=nTs} \tag{7.2}$$

or
$$H(z) = Z\{L^{-1}[h_{DAC}(s)\cdot H(s)]|_{t=nT}\} \tag{7.3}$$

where Z^{-1} and L^{-1} represent the inverse Z-transformation and the inverse Laplace transformation respectively. h_{DAC} is the impulse response of the DAC. This condition can be used to find the equivalent DT loop filter H(z) for a given CT loop filter transfer function H(s)[(6), 59]. Assume the transfer function of the CTBP filter is $H(s) = \frac{s\omega_0}{s^2+\omega_0^2}$. The equivalent Z-transforms for the RZ DAC and the HRZ DAC are given as follow:

$$H_{RZ}(z) = \frac{z^{-1}((1-\frac{1}{\sqrt{2}})-\frac{1}{\sqrt{2}}z^{-1})}{1+z^{-2}} \tag{7.4}$$

$$H_{HRZ}(z) = \frac{z^{-1}(\frac{1}{\sqrt{2}}-(1-\frac{1}{\sqrt{2}})z^{-1})}{1+z^{-2}} \tag{7.5}$$

Considering the digital delay (z^{-1}) in Figure 7.1, The combination of the RZ DAC and the HRZ DAC pulse feedback loops result in:

$$H_{2bp}(z) = k_{rz}\frac{z^{-1}((1-\frac{1}{\sqrt{2}})-\frac{1}{\sqrt{2}}z^{-1})}{1+z^{-2}} + K_{hrz}\frac{z^{-1}(\frac{1}{\sqrt{2}}-(1-\frac{1}{\sqrt{2}})z^{-1})}{1+z^{-2}}$$

$$= \frac{z^{-2}}{1+z^{-2}} \qquad (7.6)$$

where H2bp(z) represents the ideal discrete time bandpass filter in the modulator for

$$k_{rz} = -\frac{1}{\sqrt{2}} \text{ and } K_{hrz} = 1+\frac{1}{\sqrt{2}} \qquad (7.7)$$

Therefore, if the feedback coefficients for the DACs can be tuned to the above values, an ideal second-order DT transfer function is obtained. The above calculation does not account for the effects of the excess loop delay. In fact, the excess loop delay will change the above transfer function away from the desired one [61]. In addition, if only one feedback path is used and only one feedback coefficient is tuned, it is hard to make the actual realized discrete-time z-domain loop transfer function match the ideal transfer function even though the modulator's noise shaping performance can be optimized to some degree. Thus, two feedback paths including a return-to-zero DAC and half-delay return-to-zero DAC were employed in the prototype design as described by equations (7.4)-(7.7) and shown in Figure 7.1. The tuning of the feedback coefficients and the digital background tuning technique proposed in chapter 5 can be used together to achieve the best performance for a CTBP ΣΔ modulator.

The second-order differential CT ΣΔ modulator with RZ DAC and HRZ DAC was designed based on a top-level schematic shown in Figure 7.2.

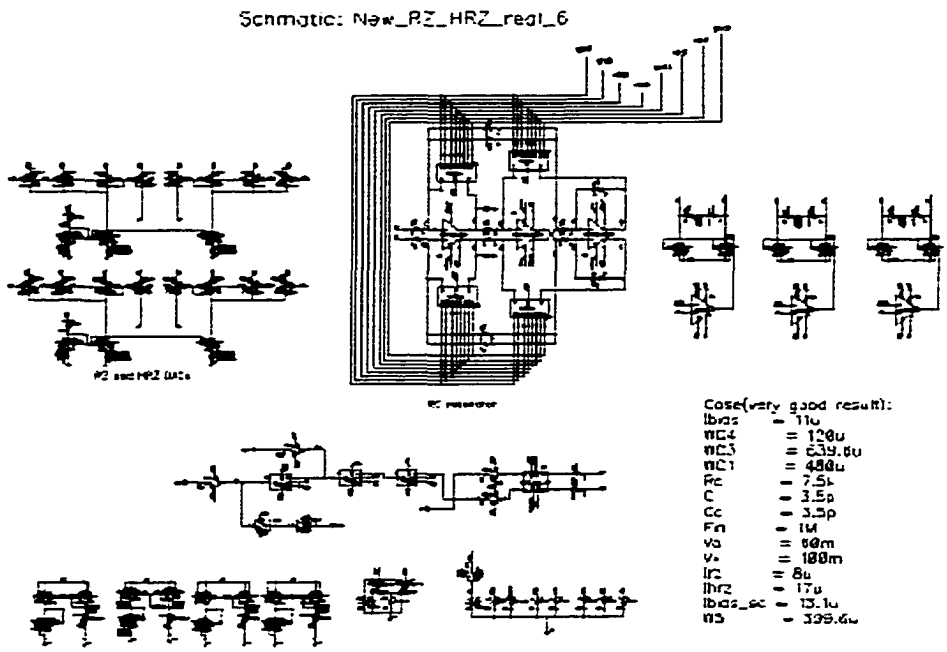


Figure 7.2 Schematic of the second-order (with RZ and HRZ DAC) CT ΣΔ modulator

It mainly consists of a fully differential active RC resonator, a comparator, a pair of half-delayed-return-to-zero DACs and a pair of return-to-zero DACs. Ideally, the Q factor of the resonator should be infinite to obtain an infinite deep noise notch. Due to some non-ideal factors such as non-idealities in the integrators, in practice, some Q enhancement circuits are often required to boost the Q factor of the resonator [59][60]. The feedback coefficients for the DACs are tuned by changing the reference currents of the RZ DACs and the HRZ DACs.

The first differential opamp of the resonator is the most important block that must be carefully designed because the non-linearities and non-idealities of the resonator will appear directly at the input. The minimum detectable input voltage U_{min} for the modulator is determined by the input

referred noise of the first opamp while the maximum detectable input voltage U_{max} is determined by the linearity of the system. Theoretical analysis can be done to derive the input referred noise. In this design, the total in-band (from 990kHz to 1010kHz) equivalent input noise voltage is obtained by simulating the resonator shown in Figure 7.5. It was found to be 26.79uV. Thus,

$$U_{min} = 26.79uV \tag{7.8}$$

By definition of SNR, the maximum detectable input signal is

$$U_{max} = U_{min} \times 10^{\frac{SNR}{20}} \tag{7.9}$$

If the desired SNR is 50dB, U_{max} is around 10mV while if the desired SNR is 70dB, U_{max} is around 85mV. HSPICE simulations show that the minimum detectable input voltage is between 1 and 2mV. In the above calculation, the noise in the coil, which was used to produce the differential inputs in experimental measurement, was not taken into account. Notice that the above SNR is limited by the circuit. It should be higher than the SNR the modulator can achieve such that the SNR due to the circuit will not limit the performance of the modulator.

To keep the modulator stable, the feedback current from the DACs must be chosen at least as large as the maximum input current. So the maximum feedback current can be calculated as

$$I_f \geq \frac{U_{max}}{R_{in}} \tag{7.10}$$

Since the bandwidth of interests is chosen as 20KHz, the over sampling ratio of the prototype is

$$OSR = \frac{f_s}{2B} = \frac{4MHz}{2 \cdot 20KHz} = 100 \tag{7.11}$$

7.3 Circuit Building Block Implementation

Since the 1.2V continuous time sigma-delta modulator prototype was designed for operating in low voltage supply, low voltage components such as resonator, comparator and current feedback DACs must be properly designed. In the following section, the design of low voltage differential opamp was first discussed and then the design of low voltage resonator and comparator were discussed.

7.3.1 Low Voltage Fully Differential Opamp

A two-stage CMOS fully differential opamp that can operate at 1 V supply [44] is shown in Figure 7.3.

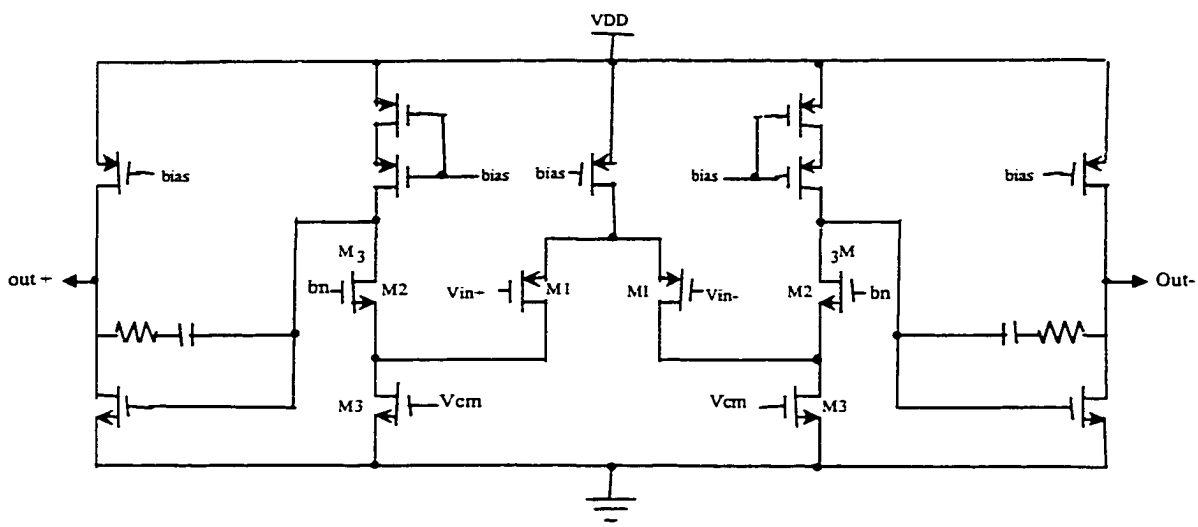


Figure 7.3 1V differential opamp

In order to improve the output impedance of the first stage or the overall gain of the amplifier, self-cascode structure described in chapter 2 was employed in this design. Additional current sources are added to the two inputs of the opamp to set the input and output common mode DC voltages independently as discussed in chapter 2. Figure 7.4 shows the common mode feedback circuit. The current i_1 is determined by the common mode output voltage and is compared with current i2, which is set by the desired common mode voltage ($V_{DD}/2$) and the resistor R. Any current difference between i1 and i2 is changed into a control voltage Vcm, which was used to adjust the V_{GS} of M3 in the fully differential amplifier to stabilize the output common mode voltage of the opamp.

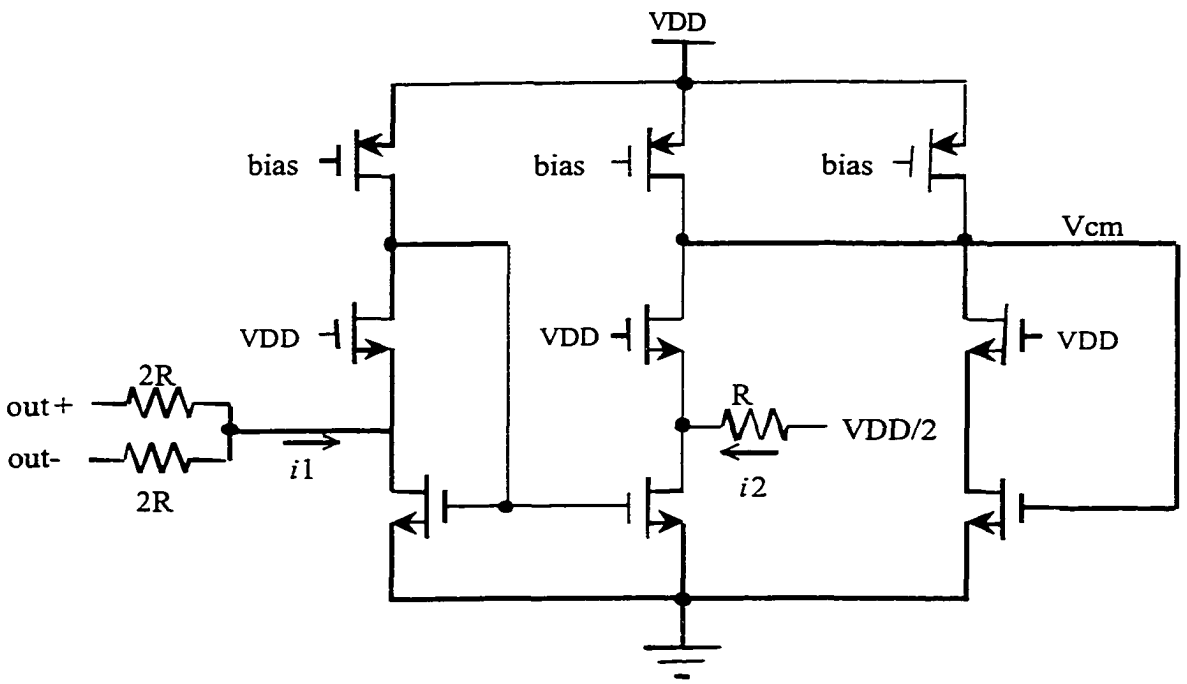


Figure 7.4 1V CMFB circuit

7.3.2 Low Voltage Active RC Resonator Design

Figure 7.5 shows the differential resonator. It is quite similar to the filter that is described in chapter 6 except that it is a fully differential design. In order to apply the low voltage technique proposed in chapter 2 to this design, an input common mode voltage controlling circuit was designed as shown in Figure 7.6, which will be used to adjust the two additional current sources. Two resistors connected to the two inputs of opamp were used to detect the input common voltage.

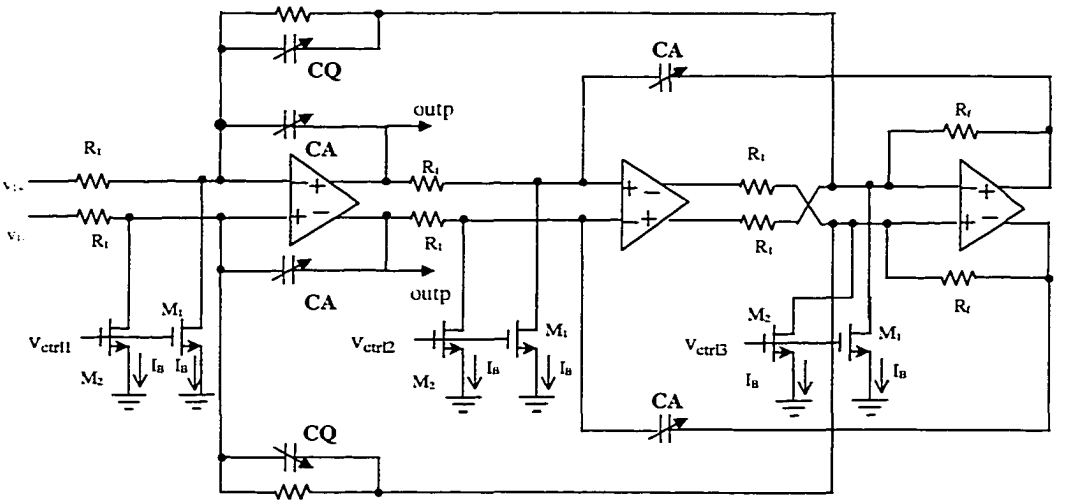


Figure 7.5 1V differential continuous-time active RC resonator

Ideally, an infinite Q should be achieved by removing the cap array CQ in the biquad filter as shown in Figure 7.5. However, simulation shows that the achievable Q is only around 50-100. In this design, programming cap array CQ is still used for tuning the Q factor. HSPICE simulations show that large Q can be achieved for the resonator when CQ value is adjusted carefully.

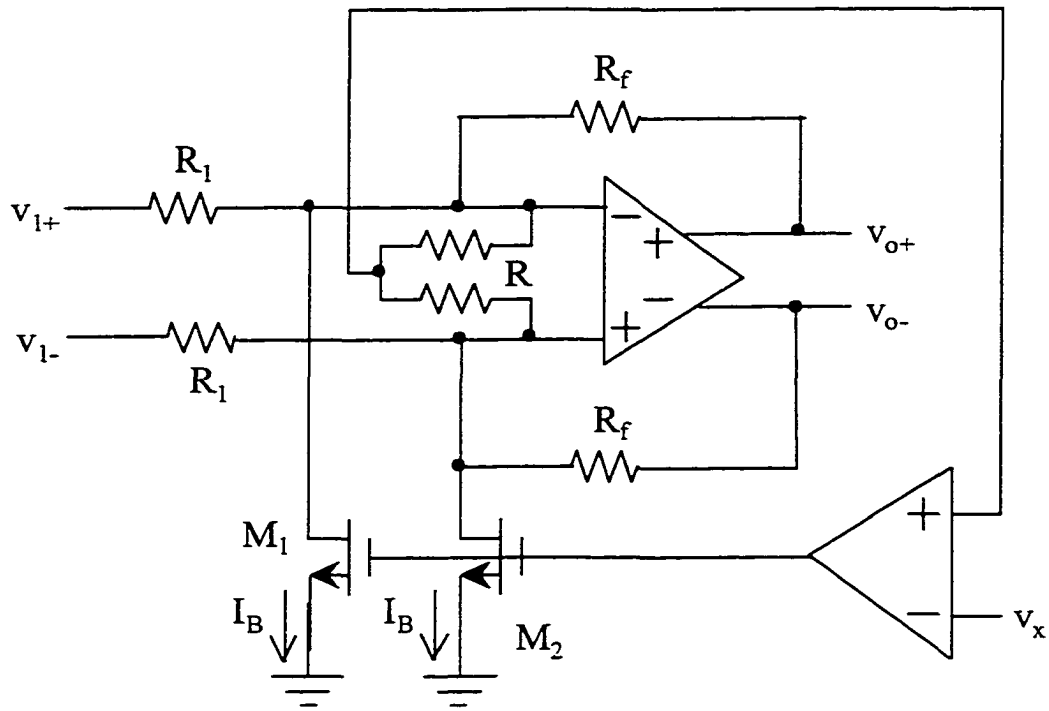


Figure 7.6 Biasing circuit to generate the additional current for the differential opamp

7.3.3 Low Voltage Latched Comparator Design

A 1V latched comparator with wide input common-mode range is proposed and is shown again in Figure 7.7. Since the input signals are connected to the resistors, a wide input signal swing can be achieved. In the modulator design, the two differential outputs from the resonator are connected to different side of the comparator for comparison while the two inputs being compared are connected in the same side and a reference input is added to the other side in chapter 6.

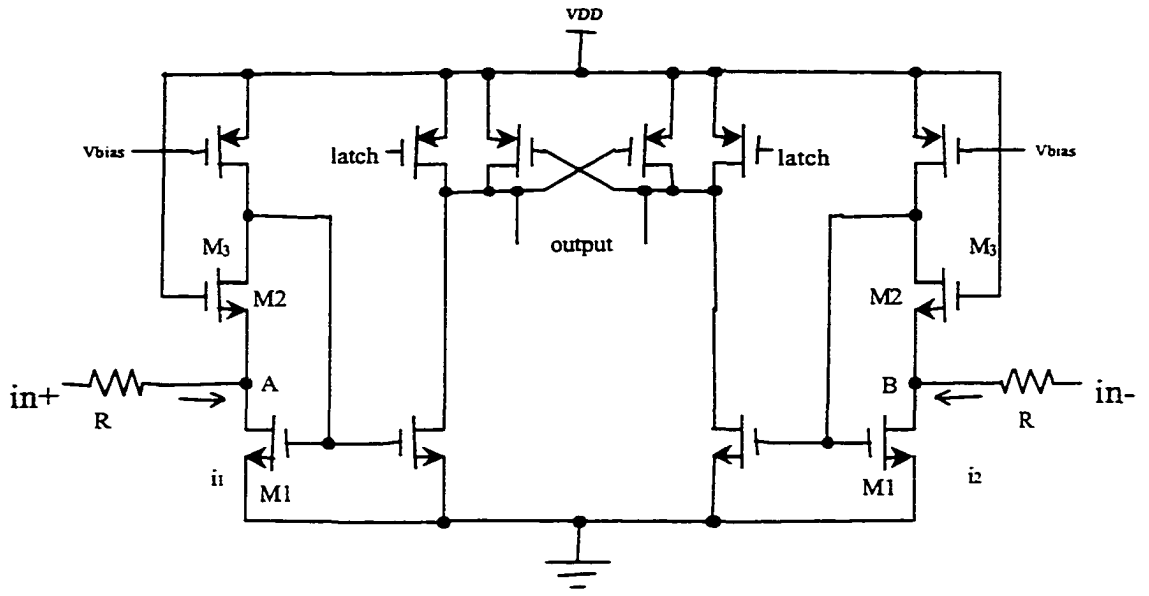
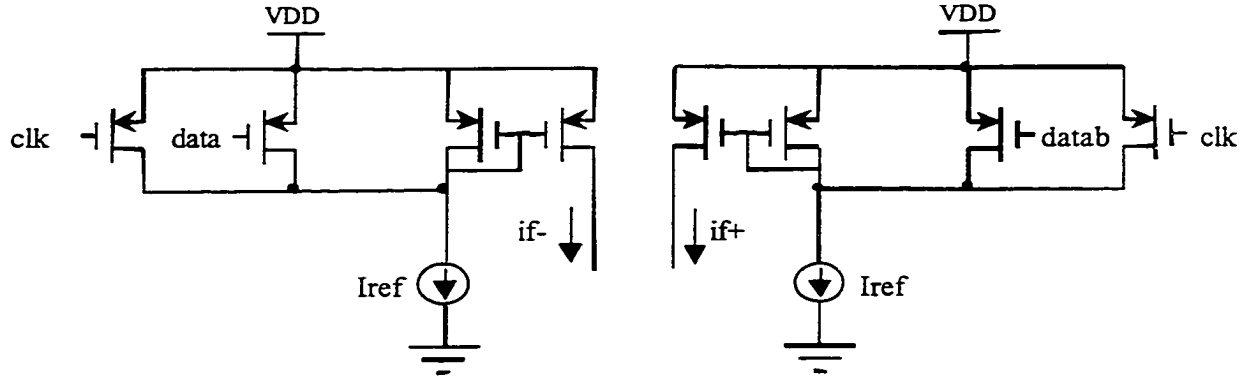


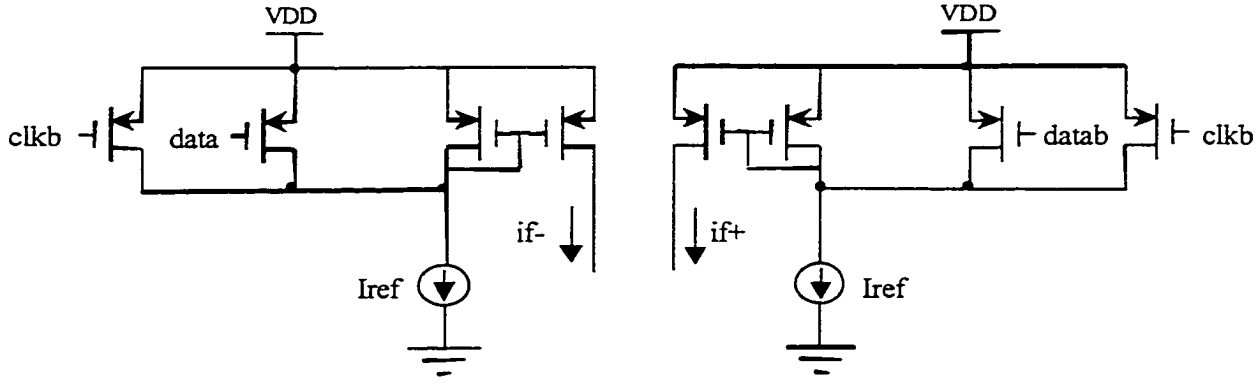
Figure 7.7 Low voltage current-mode latched comparator

7.3.4 Low Voltage Current DACs

Since return-to-zero type DACs can effectively prevent signal dependent errors that result from asymmetric rise and fall times, they are chosen for this design. The feedback DACs shown in Figure 7.8 that can operate at 1V, are used in the modulator. The outputs from the comparator are not connected directly to the current sources. Instead, they are connected to a pair of switches, which are used to bypass the currents from the reference current sources. This will avoid the noise caused by switching the current sources directly. As the input common mode voltage is close to ground (Vx is 100-150mV), the feedback currents must be designed to flow into the summing nodes. Switching the two nodes in which feedback current flows into can be used to change the sign of the feedback coefficient.



(a)



(b)

Figure 7.8 Feedback DACs (a) HRZ DAC (b) RZ DAC

7.4 Simulation Results

To achieve high Dynamic Range (DR), the excess loop delay should be less than 20% of the sampling period Ts [60][61]. In this design, simulations show that the excess loop delay is about 80-90ns, which is about 10% of the sampling period. Over 45dB of maximum SNR can be achieved for peak-to-peak output values of around 100mV. Simulation results also show that the magnitude of the input signal can not be too large otherwise it will overload the modulator. To achieve better performance, the magnitude of feedback current should be equal to or larger than the input current. A simulated output spectrum is shown in the Figure 7.9.

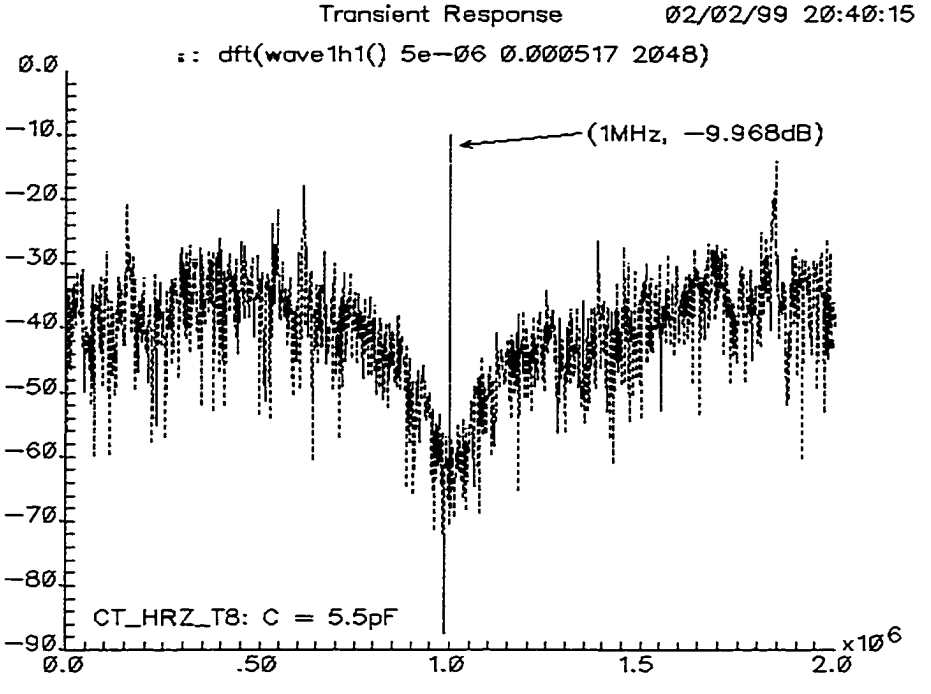


Figure 7.9 Typical FFT spectrum of the output bit stream with HSPICE

7.5 Measurement Results

The die photo of the sigma-delta modulator is shown in Figure 7.10. The modulator chip was tested with a ±0.6 V powers supply. An off-chip transformer was used to produce the two differential input signals. The digital tuning algorithm proposed in chapter 5 was applied to the modulator and was realized off-chip by first capturing the modulator output using a Tektronics logic analyzer and then calculate the tuning code using MATLAB. Afterwards, the tuning code is sent back to the modulator.

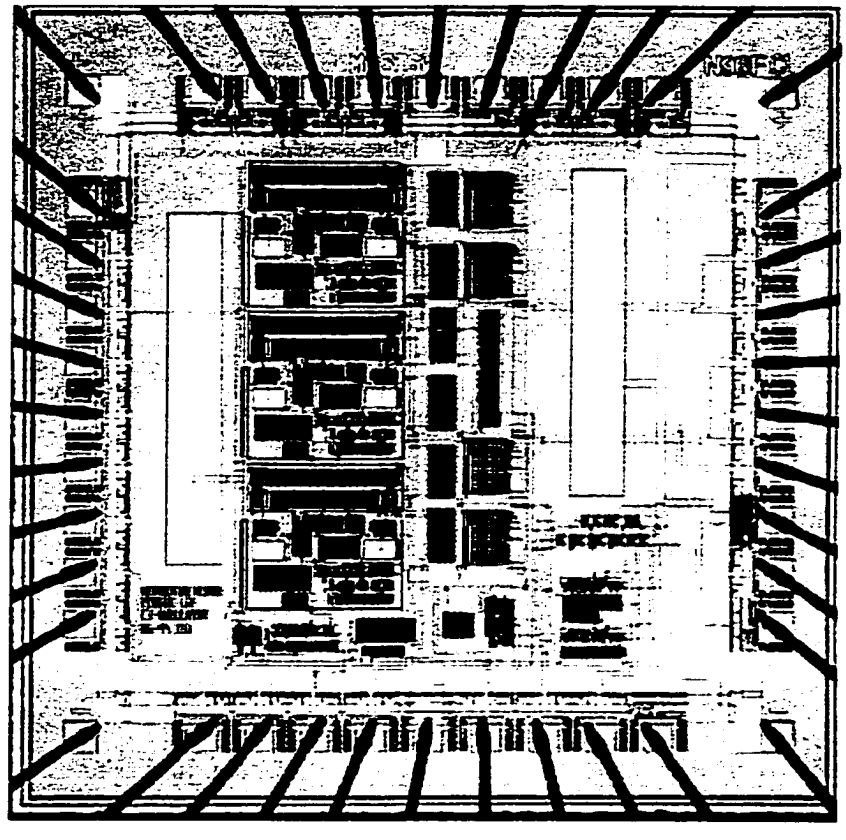


Figure 7.10 1.2V sigma-delta modulator die photo

Figure 7.11 shows the measured output spectrum using the HP 4145 spectrum analyzer when the notch frequency of the modulator was set to 1MHz. The input signal was at 1MHz, 170mV peak-to-peak voltage. The resolution bandwidth (Res BW) is set to 150Hz. All output data streams were also captured using a Logic Analyzer. 16384-point FFTs using Hanning window were performed on each of those bit streams. Figure 7.12 shows a MATLAB calculated output noise shaping spectrum for a –2dbm input amplitude at 1MHz. The sampling frequency is 4MHz. Figure 7.13 shows the measured SNR versus input signal amplitude for a single tone at 1MHz. The extrapolated DR is around 40dB(6.5bit). The maximum SNR is 44dB(7bit).

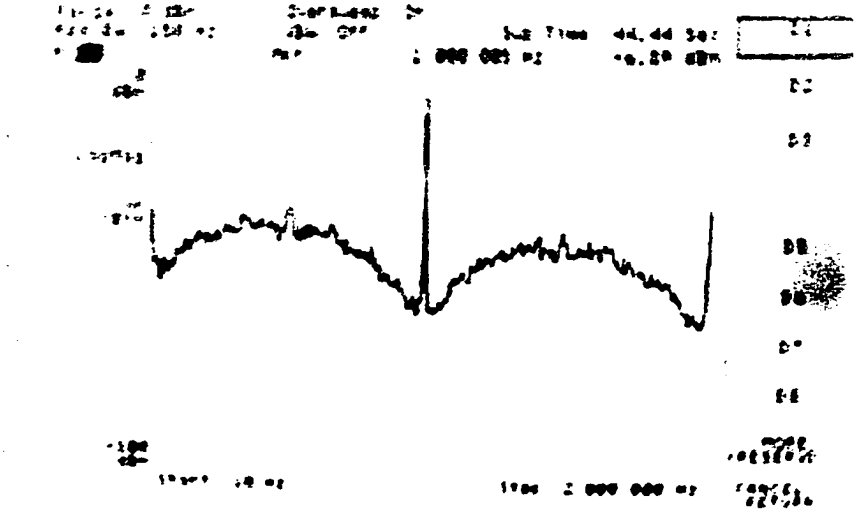
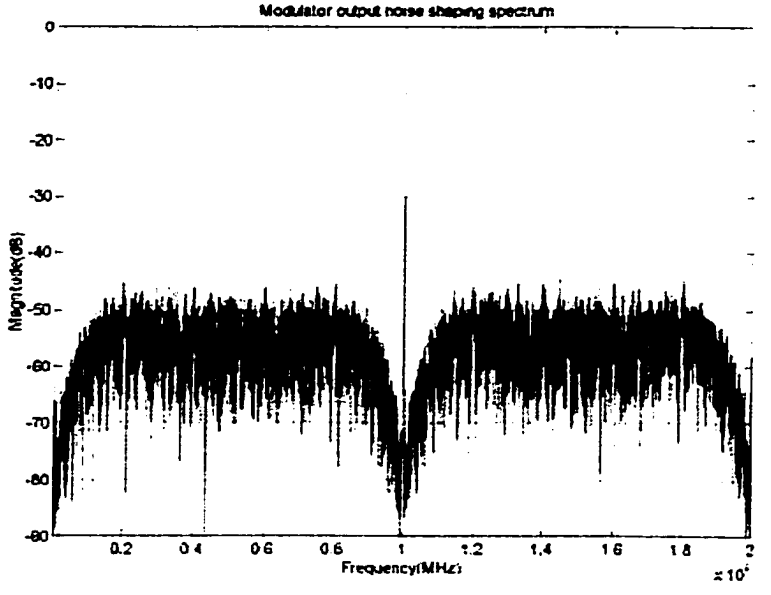
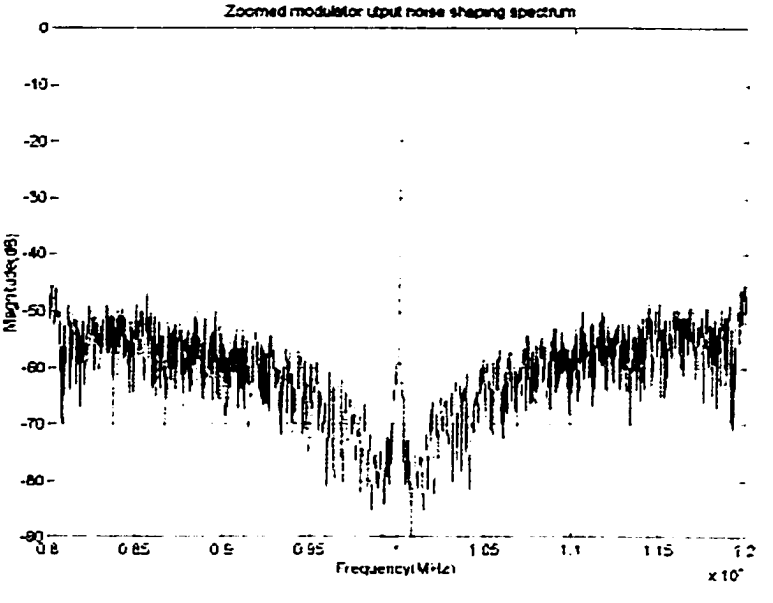


Figure 7.11 A typical noise-shaping spectrum measured using spectrum analyzer



(a)



(b)

Figure 7.12 MATLAB calculated output noise shaping spectrum

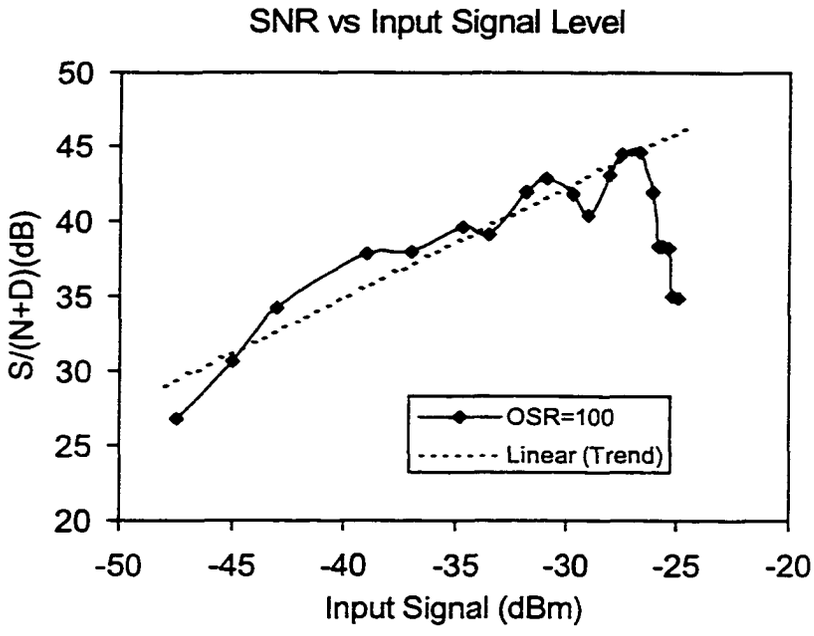


Figure 7.13 SNR versus input signal level

Figure 7.14 shows the output spectrum of the modulator before tuning when an input signal of about 1 MHz was applied. It can be observed that the notch frequency is at about 900 kHz. The desired location should be at 1 MHz. In this case, the measured SNR was 32.3 dB for a BW of 20 kHz with a peak-to-peak input signal magnitude of 360mV. To tune the modulator, the power spectral densities at 800 kHz and 1200 kHz were estimated using the method based on DFT. Each spectral density was calculated using 4096 output samples. Four numbers of calculated spectral densities were then averaged to produce the actual spectral density used for updating the tuning code. To simplify the testing operations, the simple updating equation (5.5) is used.

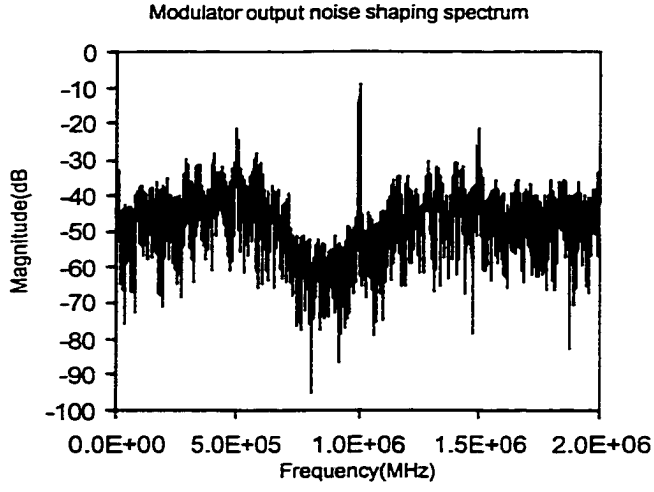


Figure 7.14 Output spectrum before tuning (SNR = 32.3 dB for a Vp-p of 360 mV)

After five iterations, the tuning code converged to the final value. In reality, the tuning code would fluctuate around the desired value for more iterations due to errors in estimating n_A and n_B. The value of $n_A - n_B$ was measured to be about -0.014390 before tuning. The output spectrum after tuning is shown in Figure 7.15, in which the tuned notch is around 1MHz. The corresponding value of $n_A - n_B$ was less than 0.000845. Table 7.1 shows the tuning codes and the corresponding measured values of $n_A - n_B$. For simplicity, only the four most significant bits D [4:7] were changed during testing. The measured SNR was 37.2 dB for a peak-to-peak input signal magnitude of 360mV after tuning. Higher tuning accuracy and quick convergence are expected if equation (5.1) is used. Similar testing results can be achieved with the noise estimating method based on two narrow band digital filters. Table 7.2 summaries the performance of the 1.2 V CTBP modulator.

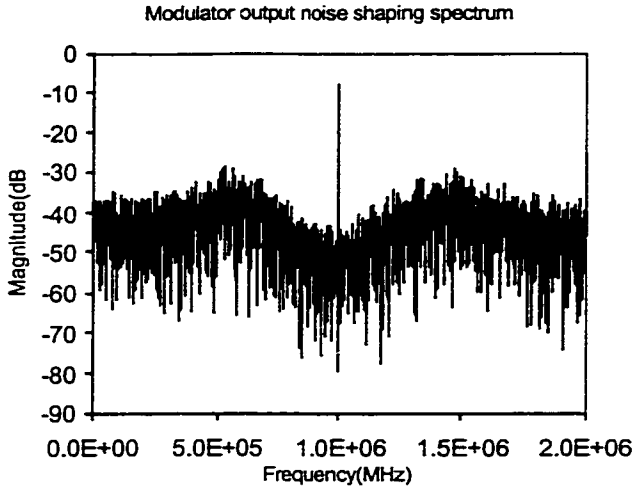


Figure 7.15 Output spectrum after tuning (SNR = 37.2 dB for a Vp-p of 360 mV)

Table 7.1 Values of $n_A - n_B$ for different tuning codes

Tuning code D[4:7]	$n_A - n_B$
1110	-0.014390
0110	-0.007196
1010	-0.012838
0010	-0.010301
1100	-0.004036
0100	+0.000845

Table 7.2 Performance summary of the 1.2V CTBP modulator

Technology	1.5 μm CMOS process
Supply voltage	± 0.6 V
Sampling frequency	4 MHz
Tuning range	0.9 MHz to 1.1 MHz
Dynamic Range	~ 40 dB
Maximum SNDR	~ 44.6 dB
Power consumption	2.1mW
Active Area	1.5 μm × 1.9 μm

7.6 Summary

To demonstrate the proposed tuning technique in chapter 5, a 1.2 V second order CTBP modulator was implemented in AMI 1.5um CMOS process. The measured DR is around 40dB(6.5bit) and the power consumption is 2.1mW. When the tuning technique was applied, the center frequency of the modulator could be tuned to 1 MHz in a few iterations from an initial center frequency between 0.9 MHz and 1.1 MHz. A maximum SNDR of 44.6 dB was achieved after tuning. These performances are comparable to the testing results of a 3V second-order Gm-C sigma-delta modulator presented in [59]. This work demonstrates the possibility of designing an ultra low voltage continuous-time BP sigma-delta modulator with tuning in a conventional CMOS process.

CHAPTER 8 CONCLUSIONS AND FUTURE WORK

8.1 Conclusion

The key motivation for studying low voltage analog circuit design is the high demand for battery-operated systems as well as lighter and faster electronic equipment using conventional CMOS process. Most previous works focus on the design of low voltage discrete time CMOS circuits. Only a few techniques had been proposed in the literature to meet the need of designing continuous-time analog circuits. Thus, this thesis focuses on the study of designing low voltage continuos-time circuit for a power supply voltage down to 1V.

This thesis describes a technique that can be used to design low voltage analog circuits for different applications such as low voltage continuous-time active RC filters and continuous-time sigma-delta modulators. In the proposed technique, some biasing current sources are added to the inverting or non-inverting opamp terminals such that the opamp input common-mode voltages can be biased close to one of the supply rails for allowing low voltage operations. For high linearity and high dynamic range applications such as tele-communication applications, active RC filters based on poly-silicon resistors and programmable capacitor arrays are often used. The proposed technique can be used to convert many high voltage active RC filters into their low voltage designs at the expense of slightly increasing noise. As a result, it may lead to increasing power consumption for a given SNR. The filter prototype achieves a high performance THD $\leq$ -56dB with an output swing of

650mVpp. The third order inter-modulation distortion is lower than –40dB for a 300mV two-tone signal at 0.9MHz and 1.1MHz. The measured DR for the 2^{nd} order sigma-delta modulator is around 40dB(6.5bit) for an OSR of 100. The peak SNR is 44dB(7bit). The performance is acceptable for a 2^{nd} order continuous-time sigma-delta modulator.

A digital frequency and Q tuning technique for low-voltage active RC biquad filters that uses programmable capacitor arrays (PCAs) was also proposed. The proposed technique does not require any peak detectors, which are difficult to implement at low-voltage. Instead, it uses a few analog comparators, a digital comparator and a few binary counters to adjust the PCAs to implement the tuning operation. The center frequency of the filter prototype can be tuned from 585KHz to 1.325MHz and the Q factor is tunable from 1 to 6 at ω_o = 1.25MHz. The center frequency of the second order bandpass filter can be tuned within $\pm$3%. The Q factor is within 15% after tuning. This is mainly limited by the phase shift of the off-chip attenuator. It can be tuned to within about 2% when on-chip atteuator is used.

The proposed low voltage design technique demonstrates promising linearity performance in the prototype filter and acceptable performance in the modulator prototype. Therefore, it is expected that it could be applied in many low voltage applications.

In the final part of this thesis, a tuning technique for tuning the notch frequency of a continuous-time $\Sigma\Delta$ modulator is presented. All the operations can be performed in pure digital domain without additional analog components. It first estimates the noise power densities of two frequencies. Then the tuning code of the BP filter is adjusted according to this information. Furthermore, the tuning algorithm can be applied even if the signal is presented to the modulator. The tuning algorithm is based on direct measuring the

characteristic of the modulator. This technique can be applied to many kinds of continuous-time ΣΔ modulators such as gm-C, L-C and RC modulators. MATLAB simulations as well as experimental results demonstrate the effectiveness of this algorithm. After the algorithm converges, large SNR improvement can be achieved. The tuning algorithm is most effective when the noise transfer function of the modulator is symmetrical at the center frequency of the bandpass filter.

8.2 Recommended Future Research

Certainly, there are a lot of generic low voltage circuit architectures and techniques to be exploited. The proposed biased opamp technique could be a good choice for designing low to medium frequency low voltage analog circuits. More works are needed to be done to further demonstrate the validity of the proposed low voltage technique before it can be applied in a practical system. Fully differential low voltage filters can be designed to achieve better performance. Higher cutoff frequency 1V filters can be designed with the proposed technique in a more advanced CMOS process. Furthermore, higher order low voltage continuous-time sigma-delta modulator could be designed to achieve a high SNR. Beside the above, the following aspects of research works can be studied:

- Design techniques for low voltage high frequency filters can be studied
- Further studies for low voltage high order and high frequency continuous-time sigma-delta modulator should be investigated
- For low supply voltage, the Q factor in a continuous-time filter is usually limited. Some Q boosted circuits need to develop for low voltage continuous-time filters

- A background calibrating and tuning technique may need to study such that it applies to both symmetrical and asymmetrical spectrum
- The direct tuning technique can be further studied for tuning continuous-time filters

APPENDIX: MATLAB CODE TO SIMULATE THE PROPOSED TUNING TECHNIQUE

```
%Matlab code used to simulate the proposed tuning system with two narrow-band filters
%to estimate the noise power density
%Some sub-codes are from the Delta Sigma Toolbox by Richard Schreier [72] of Oregon
%State University
%by Huanzhang Huang 10/05/00

clear;
clc;
addpath d:\sigmadelta_toolbox\release;
format long;
fprintf('\t\t\t ********************************************** \n');
fprintf('\t\t\t Direct Digital Tuning For Bandpass Modulator \n');
fprintf('\t\t\t     With Two Narrow Bandpass Filters \n');
fprintf('\t\t\t     by Huanzhang Huang Oct. 15, 2000 \n');
fprintf('\t\t\t ********************************************** \n');
N=8192*2*2;
f0 = 1/4; R=32;

%Updating coefficient for the complicated updating scheme
ucof=1e-7;

%Updating increment for the simple updating scheme
delta=2e-3;

%The initial u value
%c(1)=1/4+1/128;
c(1)=0.28; %The initial normalized center frequency
NADC=0;
NBDC=0;
loopnum=30;

for k=1:loopnum,
  fprintf(' \n');
  fprintf(' \n');
  fprintf('****************** ****************************** \n');
  fprintf('This is tuning loop \n');
  k
```

```
%c(k)=c(k-1)+ucof*(NADC-NBDC);
  %H = synthesizeNTF(8,R,1,[],f0);
  ntf = synthesizeNTF(8,R,1,[],c(k));
  fB = ceil(N/(2*R));
  %f=round(f0*N + 1/2*fB);
  f=(f0+1/512/4)*N;
  %f=round(f0*N+1/23*fB);
  u = 0.1*sin(2*pi*f/N*[0:N-1]);   % sine-wave input
  v = simulateDSM(u,ntf); % the bit stream from sigma-delta modulator
  echo off;

  %figure(1); clf;
  %t = 0:500;
  %stairs(t, u(t+1),'r');
  %axis([0 40 -1.2 1.2]);
  %figure(2); clf;
  %stairs(t, u(t+1),'r');
  %hold on;
  %stairs(t,v(t+1),'g');
  %axis([0 500 -1.2 1.2]);
  %xlabel('Sample Number');
  %ylabel('u, v');
  %title('Modulator Input & Output');

  spec = fft(v.*hann(N))/(N/4);
  echo off;
  figure(3); clf;
  plot(linspace(0,0.5,N/2), dbv(spec(1:N/2)))
  f1 = round((f0-0.25/R)*N);
  f2 = round((f0+0.25/R)*N);
  snr = calculateSNR(spec(f1:f2),f-f1+1);
  text(0.32,-110, sprintf('SNR = %4.1f dB\n(OSR=%d)',snr,R));
  axis([0 0.5 -160 0]);
  grid on;
  xlabel('Normalized Frequency')
  ylabel('dBFS')
  title('Output Spectrum');

  %Two Discrete Time Bandpass Filtes

  kbw1=0.001;
  kbw2=0.001;
  kw1=2-1/6;
  kw2=2+1/6;
  %syms z;
```

```
  %nom=-kbw*(1+1/z)*(1-1/z);
  %denom=2*(1-(2-kbw-kw*kw)/z+(1-kbw)/(z^2));
  %hz=nom/denom;
  %hn=iztrans(hz)
  b1=[200 0 -200];
  b2=[200 0 -200];
  a1=[4+2*kbw1+kw1^2 -8+2*kw1^2 4-2*kbw1+kw1^2];
  a2=[4+2*kbw2+kw2^2 -8+2*kw2^2 4-2*kbw2+kw2^2];
  %notch1=v-u;
  x=filter(b1,a1,v);
  y=filter(b2,a2,v);
  notch1=v-x;
  pp(1:N)=1;
  z1=filter(b1,a1,pp);
  z2=filter(b2,a2,pp);

  spec1 = fft(x.*hann(N))/(N/4);
  spec2 = fft(y.*hann(N))/(N/4);
  spec3 = fft(z1.*hann(N))/(N/4);
  spec4 = fft(z2.*hann(N))/(N/4);
  spec5 = fft(notch1.*hann(N))/(N/4);


  % BP filter spectrum
  figure(4); clf;
  plot(linspace(0,0.5,N/2), dbv(spec(1:N/2)),'k')
  hold on;
  plot(linspace(0,0.5,N/2), dbv(spec3(1:N/2)),'r')
  hold on;
  plot(linspace(0,0.5,N/2), dbv(spec4(1:N/2)),'b')
  axis([0 0.5 -180 50]);
grid on;
xlabel('Normalized Frequency')
  ylabel('Magnitude')


  figure(5); clf;
  %spec = fft(x.*hann(N));
  %plot(dbv(spec(1:N)))
  echo off;
  plot(linspace(0,0.5,N/2), dbv(spec1(1:N/2)), 'r')
  axis([0 0.5 -160 50]);
grid on;
xlabel('Normalized Frequency')
  ylabel('Magnitude')
```

```
  figure(6); clf;
  plot(linspace(0,0.5,N/2), dbv(spec2(1:N/2)),'b')
  axis([0 0.5 -160 50]);
grid on;
xlabel('Normalized Frequency')
  ylabel('Magnitude')


  %*****************X^2*******************

  M=2^10;
  %first sub loop
  for i=1:round(N/M),
  na(i)=0;nb(i)=0;
  for j=1+(i-1)*M:i*M,
  na(i)=na(i)+x(j)^2/M;
  nb(i)=nb(i)+y(j)^2/M;
      end
  %na(i)=na(i)-max(x)^2/M;
  %nb(i)=nb(i)-max(y)^2/M;
  end

  figure(7); clf;
  i=1:round(N/M);
plot(i, na*1, 'r', i, nb*1, 'bo-')
xlabel('Computation Number')
  ylabel('Estimated Noise Power')

%Second sub-loop
NADC=0;
  NBDC=0;
  p1=round(N/M);
  for l=1:p1,
  NADC=NADC+na(l)/p1;
    NBDC=NBDC+nb(l)/p1;
  end

  fprintf('Simulation Complete Successfully!!!\n\n');

%if (abs(NADC-NBDC)< 2500)
%  break
%end
```

```
  %Complicated updating scheme

  c(k+1)=c(k)-ucof*(NADC-NBDC);

  %Simple updating scheme

  % c(k+1)=c(k)-delta*(NADC-NBDC)/abs(NADC-NBDC);


end

%Drawing the settling curve
figure(8); clf;
    i=1:loopnum;
  plot(i, c(i), 'r^')
xlabel('Tuning Loop Running Number')
ylabel('Tuning Code')
title ('Tuning Settling Curve');
```

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